Resonant Clocking

How to save more energy in today's ICs ??

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Need for Speed and Need to be GREEN

- An average Google search is reported to require ~ 0.3 watt-hours.
- Datacenters need to be fast and very energy efficient for a sustainable growth.
- Requires massive number of high speed processors.
- The clock network has an activity of ~1.

Clock networks account for 25% to 35% of computing today



Common Techniques for Energy Saving in ICs

- Clock and Power Gating
- Multi-V_T
- Multiple Voltage Domains
- Dynamic Voltage Scaling (DVS)
 EDA Companies support these techniques

All these are done but just not enough!

Clock still hurts though it's the heart of the system



Clock Methodologies



Courtesy: Synopsis Inc.

The mesh network is good for skew management but itself has a big capacitance which consumes power

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Pendulum and Oscillation



Pendulums require a small nudge and it can oscillate forever. But friction and drag is the barrier to the perpetual system

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LC Oscillator





Parasitic resistance of this circuit is similar to the friction resistance of the pendulum

Can we use this circuit to save energy without major overhaul of the design flow??



The Answer is "YES"



- **Resonant clock mesh** marries the benefits of a clock mesh with the ultralow power consumption of a tank circuit
- The inductors that are built on the chip, in parallel with the capacitance of the clock grid, produce a natural oscillator to drive the clock grid ... with hardly any power consumption.



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- No clock skew means much less engineering time and resources are required and the SoC will perform faster. Clock meshes are much more immune to OCV so vendors benefit from higher manufacturing yields (and hence lower parts cost).
- ARM926 was used to implement the concept and it resulted in ~25% 35% decrement in overall chip power.



RCM Design Flow

However, ~5% more area consumption occurs

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Resonant Clocking Circuits



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UCLA 9

Contd....



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Resonant Transmission Line



!! Thank You !!

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