UCLA

An Introduction of Clock Gating Implementation in Architecture/Microarchitecture

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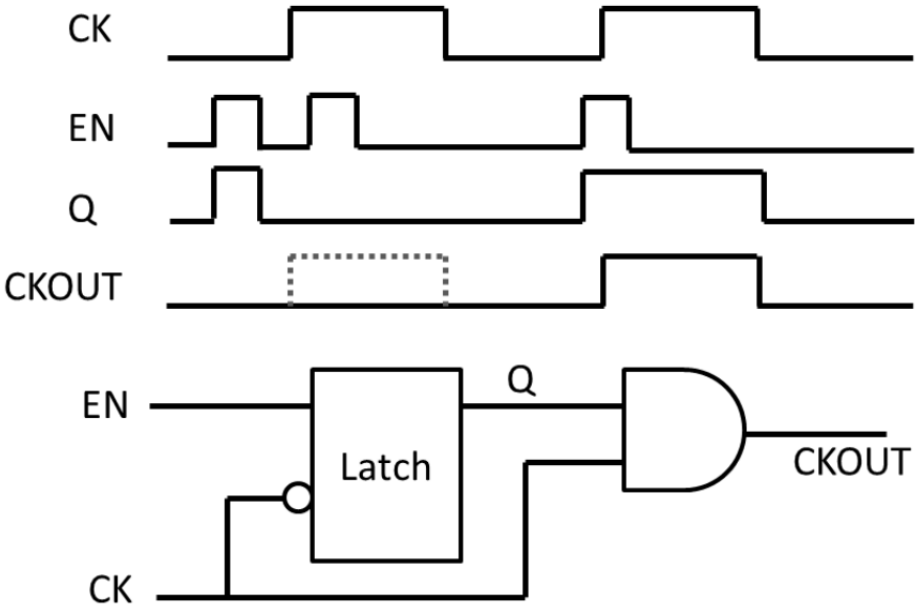
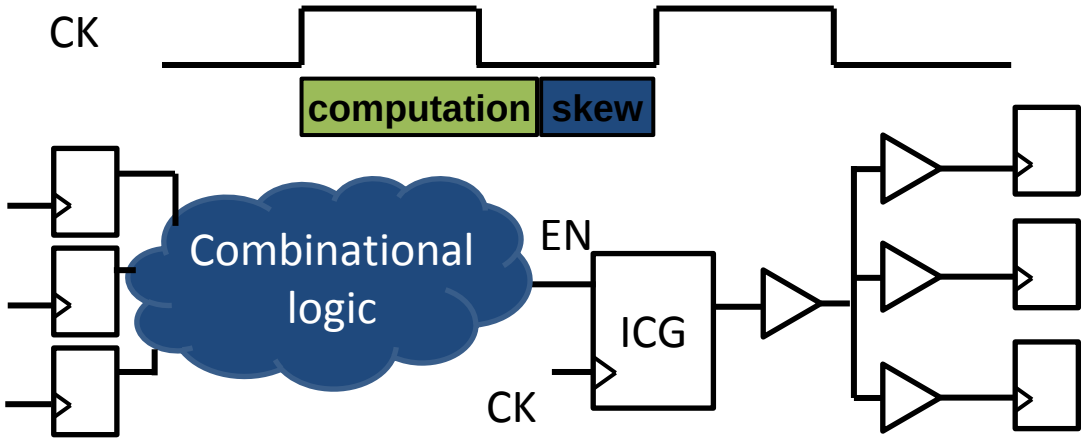
Clock Gating Cell



- Latch-based design
- FF-like timing behavior
- Zero clock gating latency

Timing Verification



- FF-like timing constraints for easy timing verification
- Skew may be too big for sub-cycle clock gating latency

Example in ARM CortexA9

Gated blocks

The Cortex-A9 processor or each processor in a CortexA9 MPCore design supports dynamic high level clock gating of:

- the integer core
- the system control block.
- the data engine, if implemented.

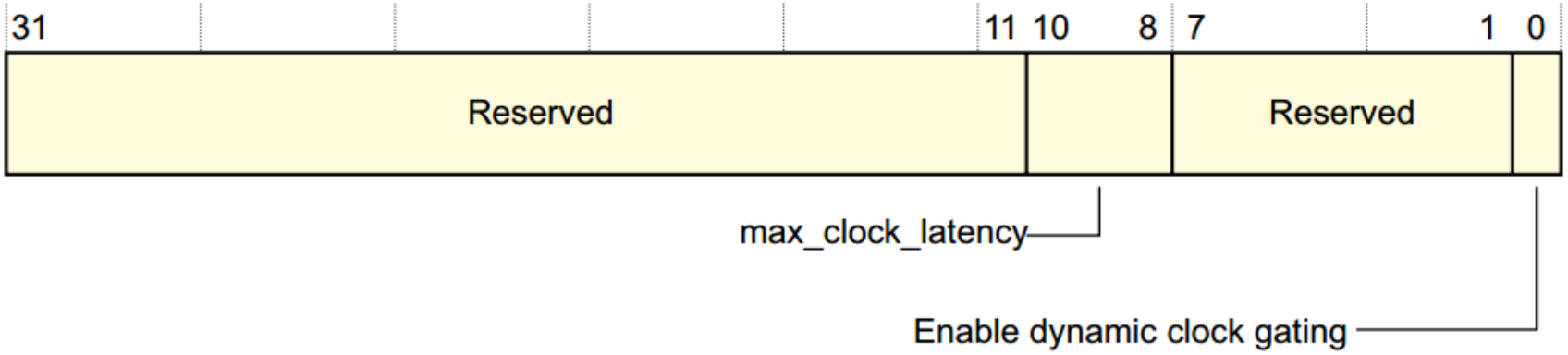
Power Control Register

The Power Control Register controls dynamic high level clock gating. This register contains fields that are common to these blocks:

- the enable bit for clock gating
- the max_clk_latency bits.

Cortex-A9: http://infocenter.arm.com/help/topic/com.arm.doc.ddi0388i/DDI0388I_cortex_a9_r4p1_trm.pdf

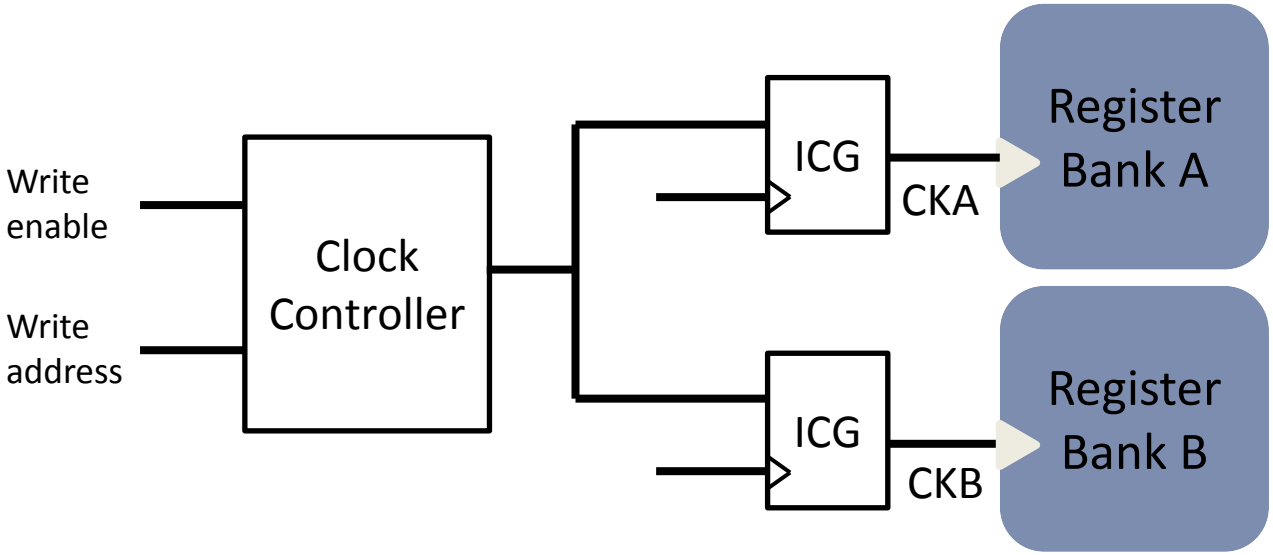
Example in ARM CortexA9



[10:8]	max_clk_latency	Samples the value present on the **MAXCLKLATENCY** pins on exit from reset. This value reflects an implementation-specific parameter. ARM strongly recommends that the software does not modify it. The max_clk_latency bits determine the length of the delay between when one of these blocks has its clock cut and the time when it can receive new active signals. If the value determined by max_clk_latency is lower than the real delay, the block that had its clock cut can receive active signals even though it does not have a clock. This can cause the device to malfunction. If the value determined by max_clk_latency is higher than the real delay, the master block waits extra cycles before sending its signals to the block that had its clock cut. This can have some performance impact. When the value is correctly set, the block that had its clock cut receives active signals on the first clock edge of the wake-up. This gives optimum performance.

Cortex-A9: http://infocenter.arm.com/help/topic/com.arm.doc.ddi0388i/DDI0388I_cortex_a9_r4p1_trm.pdf

Example of Register File Banking



- Banking register file based on write access and address
- Write address becomes available only one cycle before the actual register write operation
- Sub-cycle latency requirement