Local Interconnect

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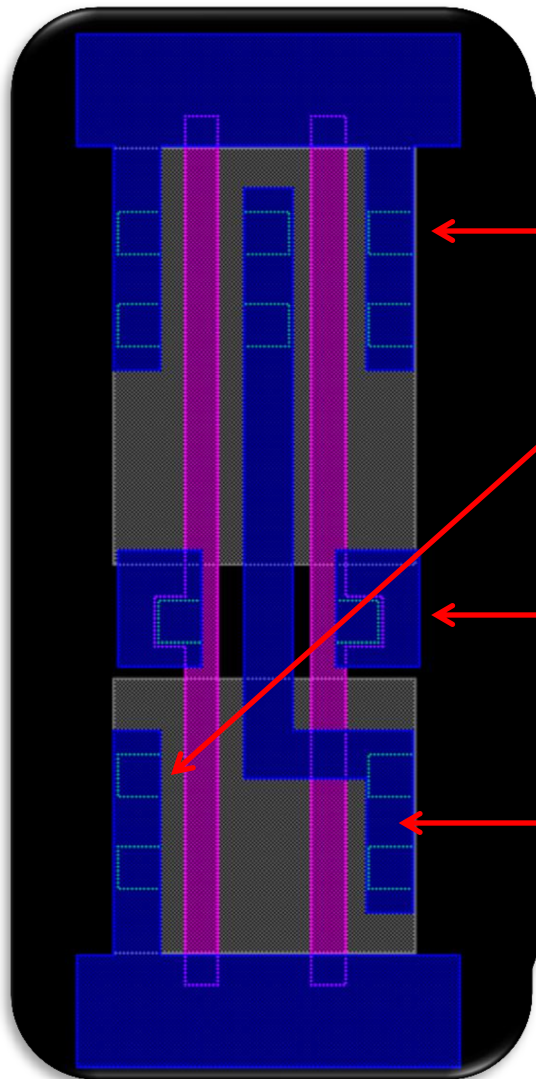
Conventional Standard Cell



Power/Ground connections

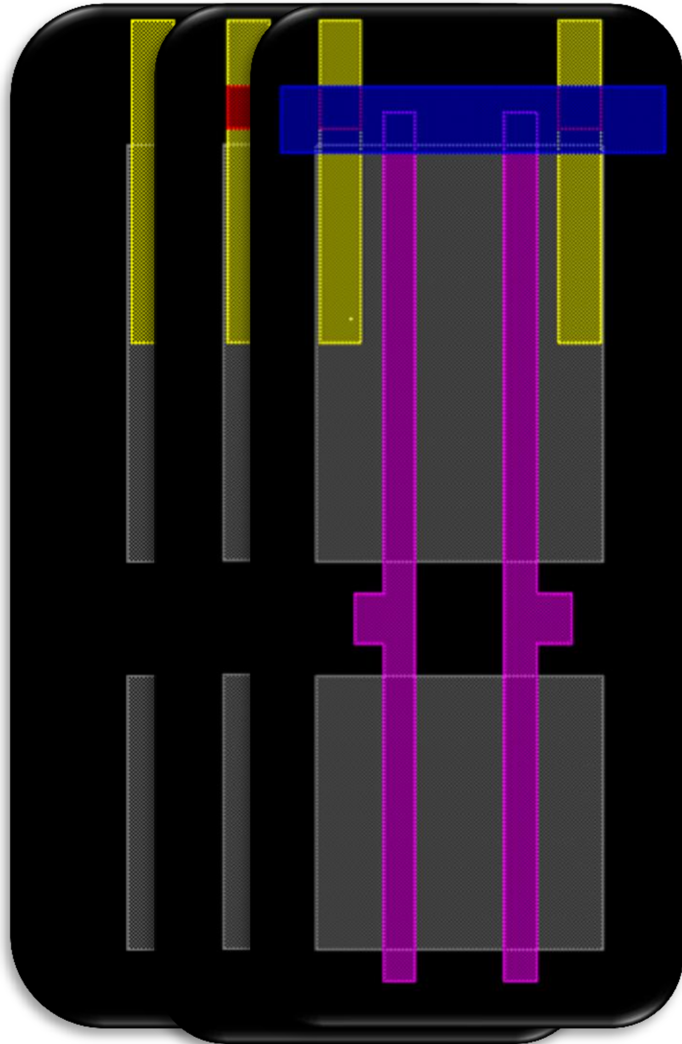
I/O connections

Local routing

Issues

- Printing contacts lithographically challenging
- Metal 1 very complicated (DPL conflicts)
- Limits scaling of standard cells

Standard Cell using local interconnect



- Spreads the complexity of metal 1 and contact layers to three layers: LI, V0 and M1
- Side benefit: Reduces channel strain caused by contacts
- Similarly other uses of contact also replaced by LI layer

Commercial 22nm Cell Layout

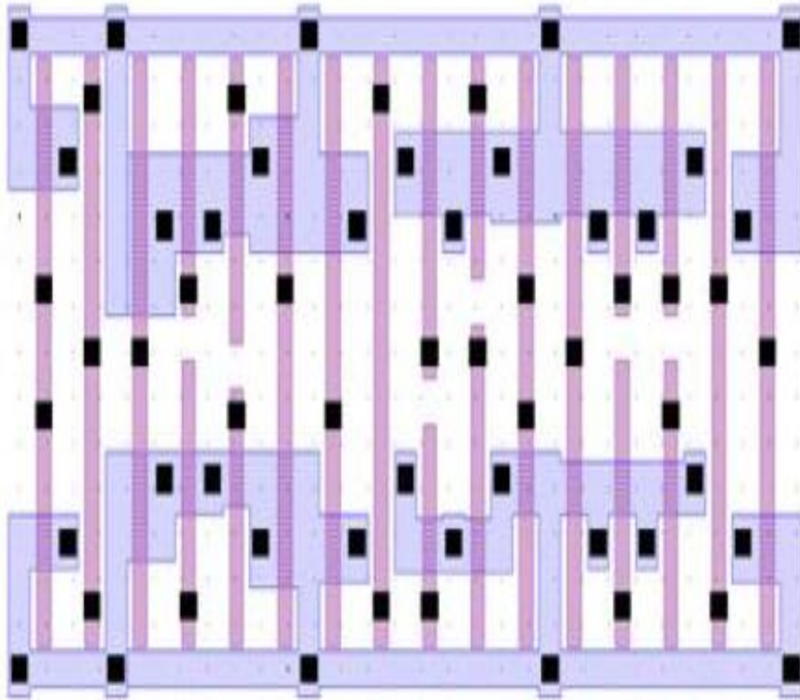


Fig.2a. Conventional Layout

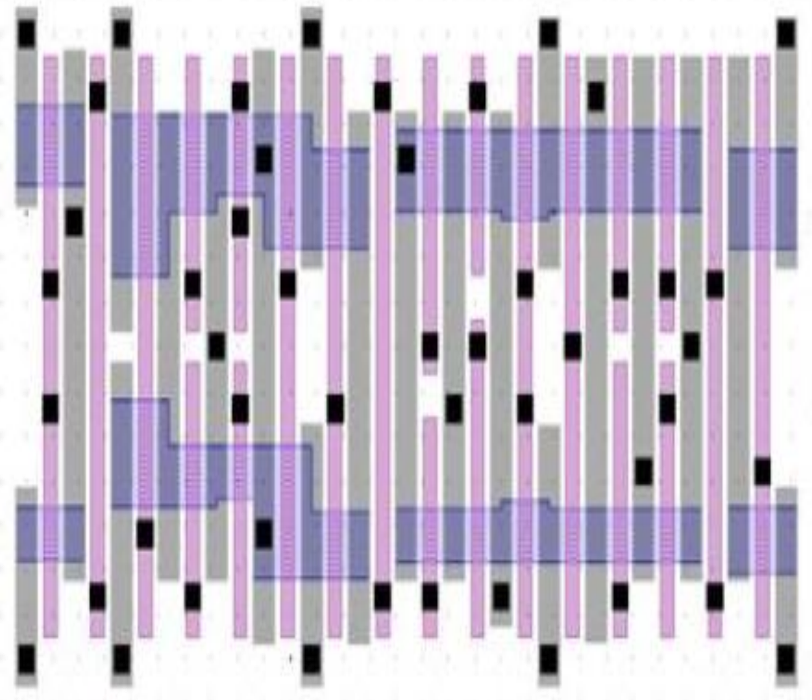
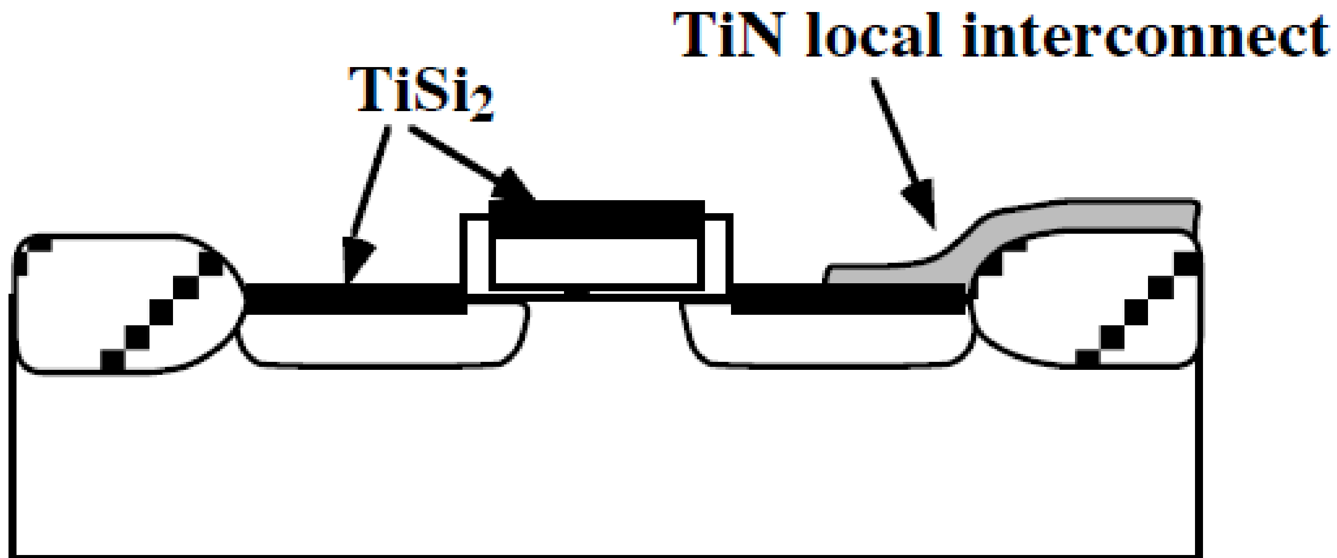


Fig.2b. Layout with Local Interconnect.

Source: Smayling et. al., SPIE 2010

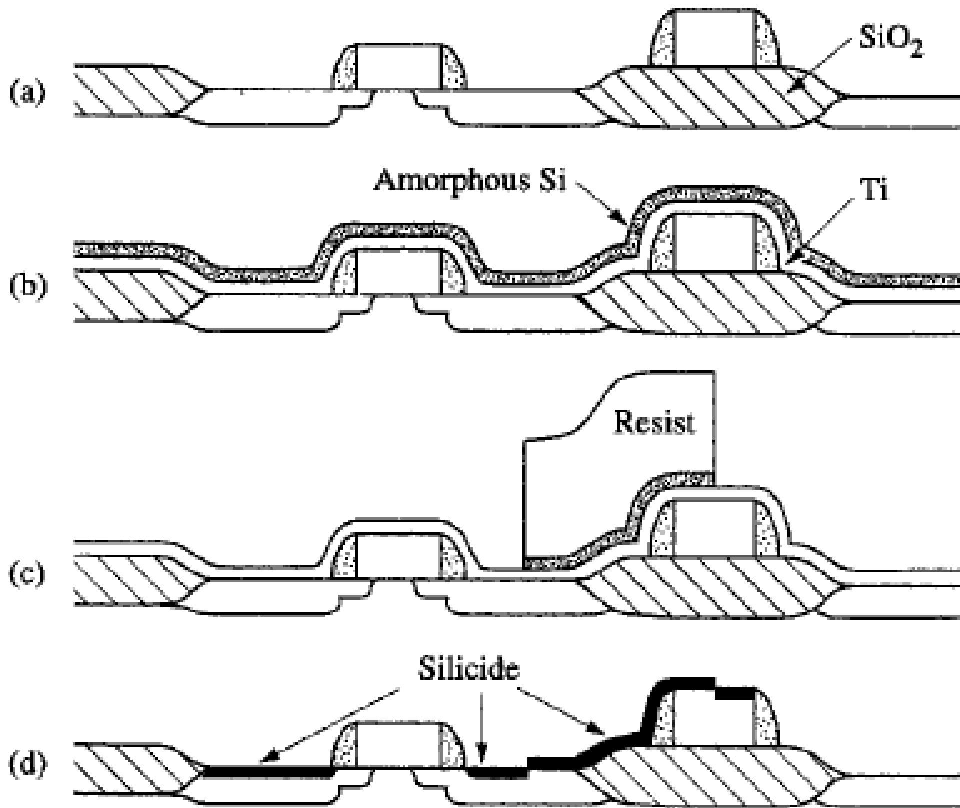
BEOL stack with local interconnect

- First proposed by TI in 1987 to improve SRAM density
- Requires an additional mask layer
- 10-20% density improvement was reported
- Salicide process was used for creating LI using TiN



Source: Saraswat, EE311 Lecture Notes

LI Manufacturing Steps



Source: Mann et. al., J. IBM, 1995

Devices Formed

Ti and Si deposited on formed devices

Local Interconnect Mask Exposed

Annealing to create silicide ($TiSi_2$)