Calibration of Setup and Hold Time for Latches and Flip-flops(II)

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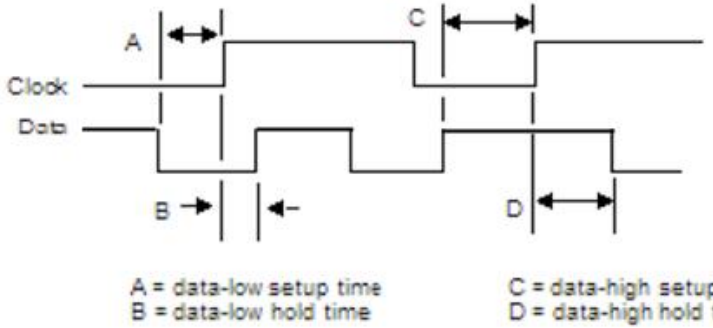
Outline

1. Definition of setup and hold time
2. Purpose for the constraints
3. Latches transient response example
4. Flip-Flops transient response example
5. References

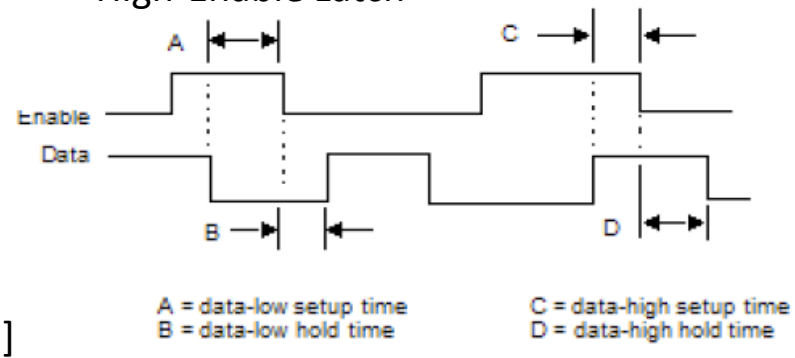
Definition of Setup and Hold Time(1/2)

Setup and Hold Times Specification for Rising-Edge-Triggered Flip-Flop

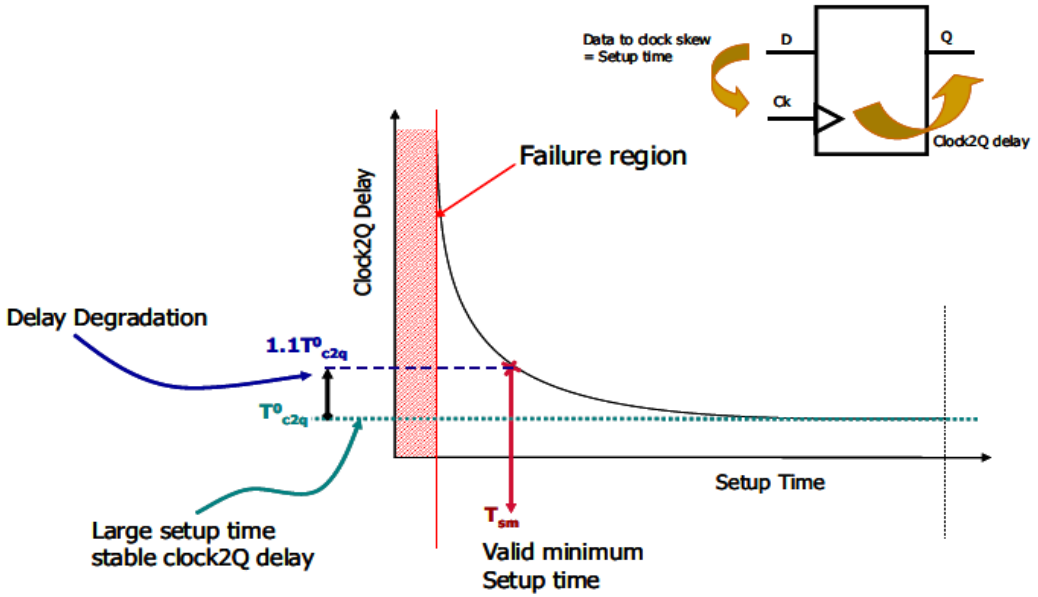


[1]

Setup and Hold Sepcification for High-Enable Latch



As the data setup time decrease and move toward the boundary of failure region, the clk-Q daley will increase.
When it reach beyond the boundary, it will not be able to flip the Q signal to follow the D signal.

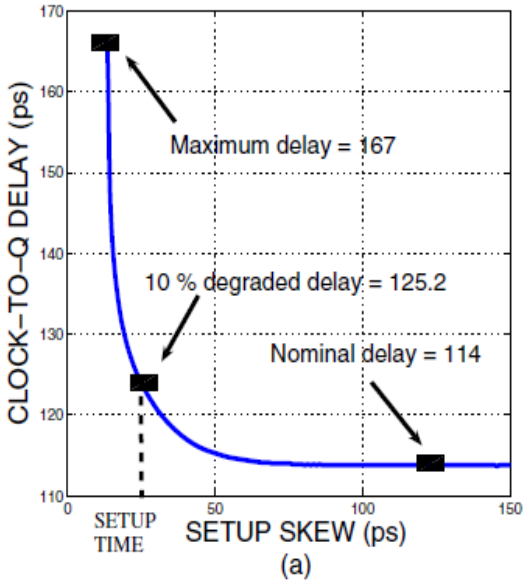


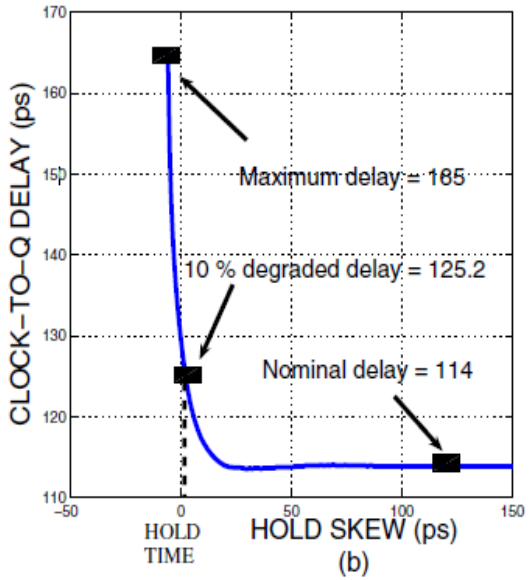
[2]

Setup and hold constraints(1/2)

The industrial methodology to calibrate setup and hold time is done by calibrating the nominal Clk-Q delay and search for the setup/hold time that gives the 1.1xnominal delay.
The binary search is usually applied.

[3]



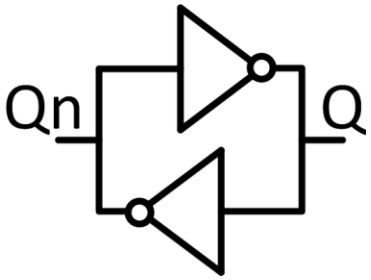


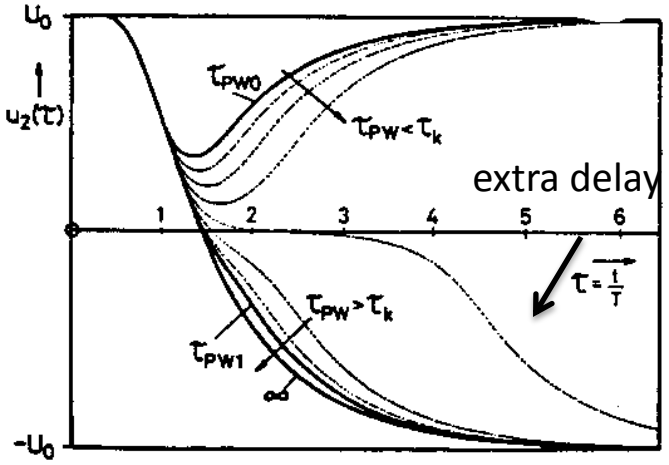
- In most lib file, calibrated for different sets of
  - Slope of CLK signal
  - Slope of Data signal

```
index_1("0.4, 0.57, 0.84"); /* Data transition Time*/
index_2("0.4, 0.57, 0.84"); /* Clock transition Time*/
values( /* 0.4 0.57 0.84 */ \
/* 0.4 */ "0.063, 0.093, 0.112", \
/* 0.57 */ "0.526, 0.644, 0.824", \
/* 0.84 */ "0.720, 0.839, 0.930");
...
```

[4]

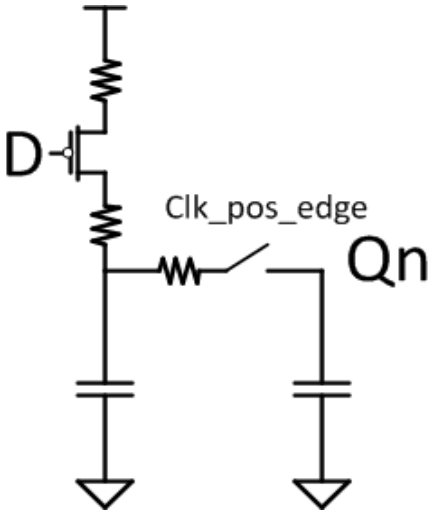
Purpose of the constraints(1/2)



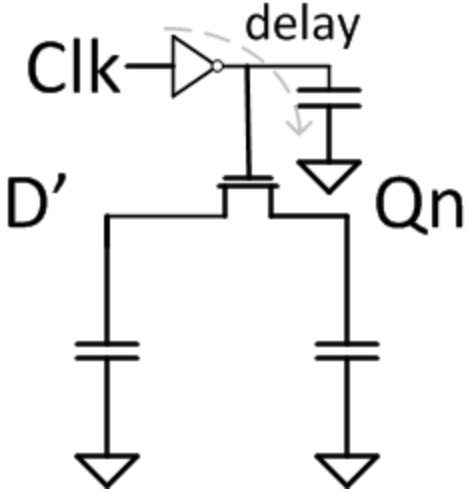


[5]

Setup time example



Hold time example

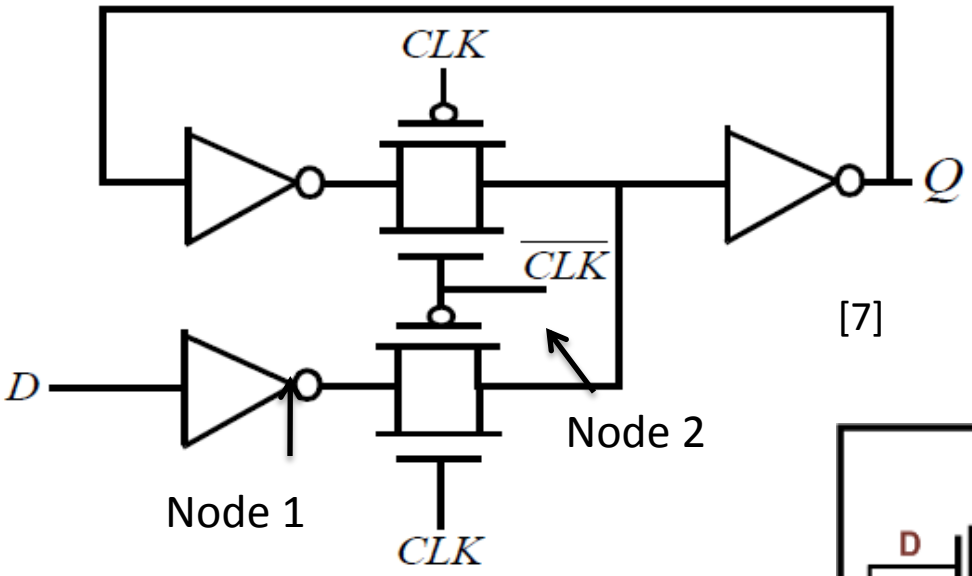


A delay of a gate is a function of the input slop

If there is a slope in controlling signal, then for some CMOS circuits both NMOS and PMOS might be turn on and increase the required time of charging and discharging

Purpose of the constraints(2/2)

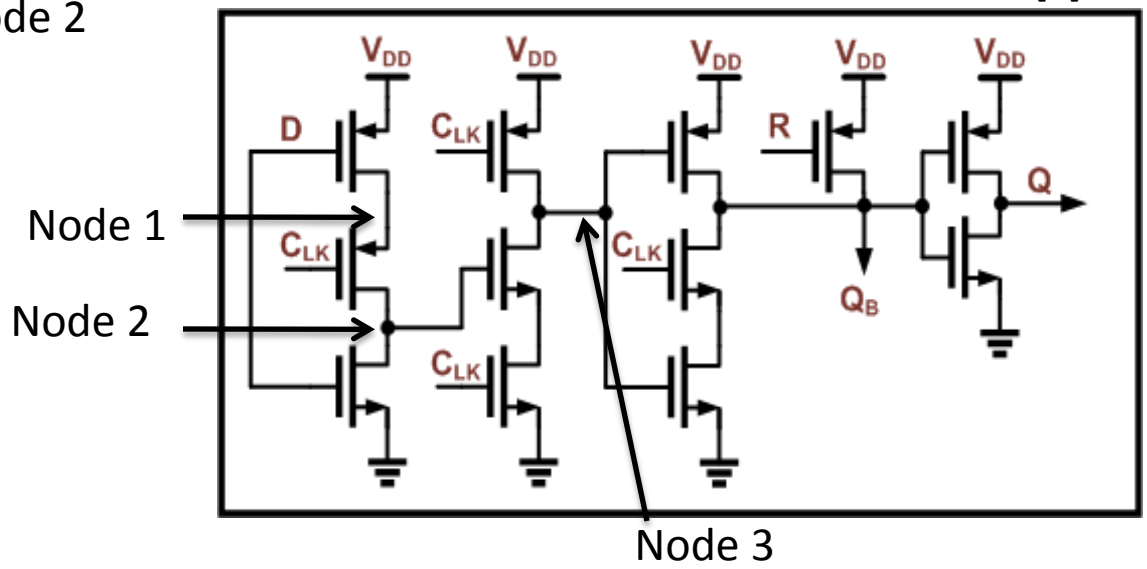
Latch design example



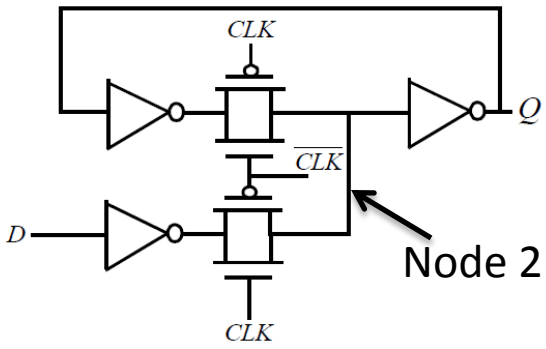
[7]

D Flip-Flop design example

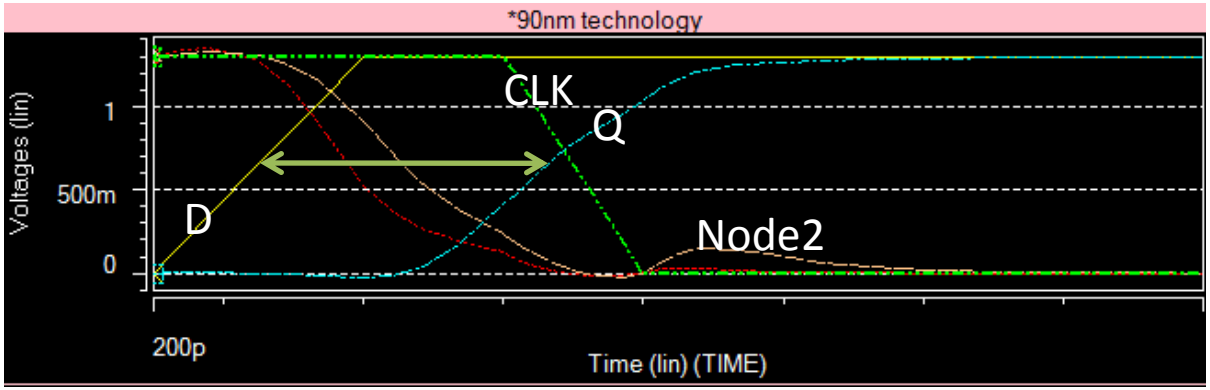
[8]

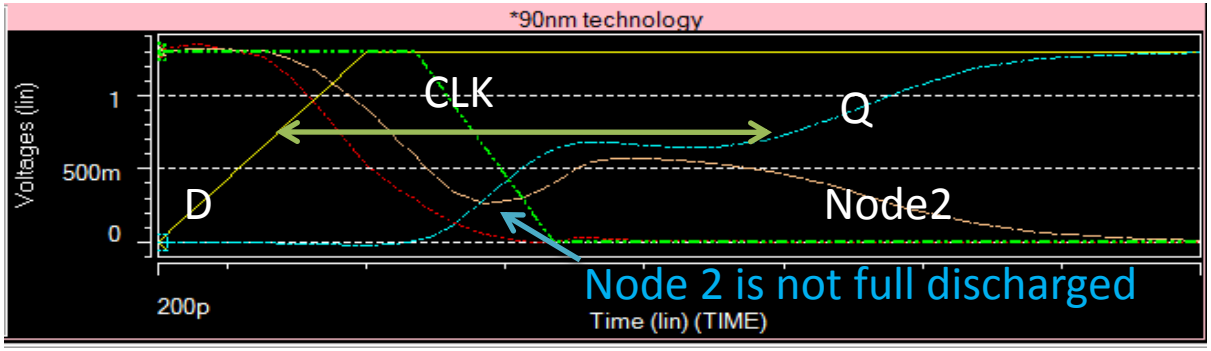


Latches transient response

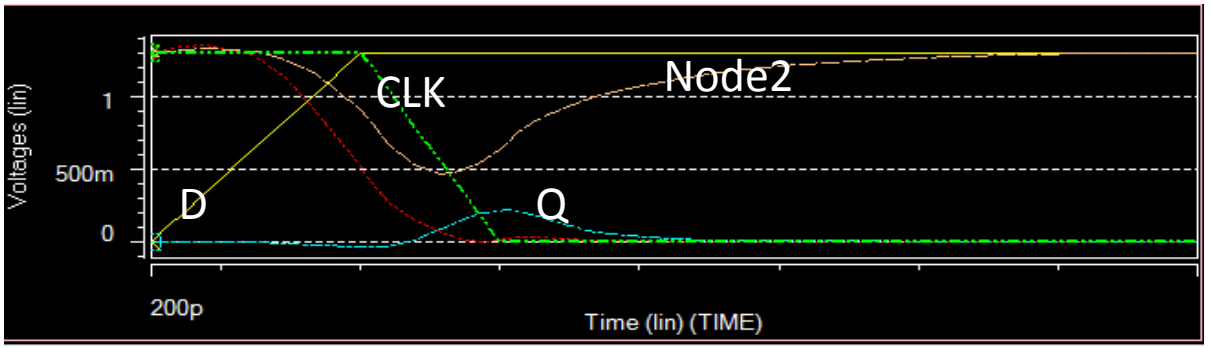


The internal nodes are not yet full discharge before the enable signal goes < vt

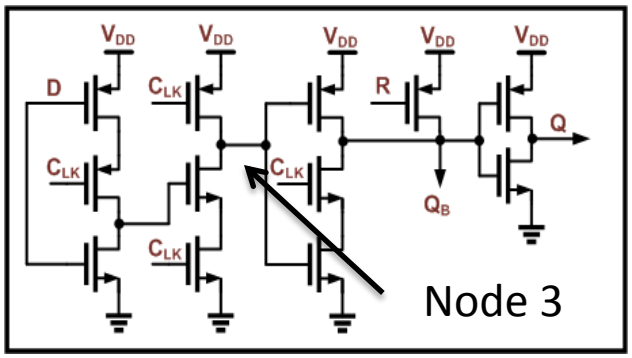


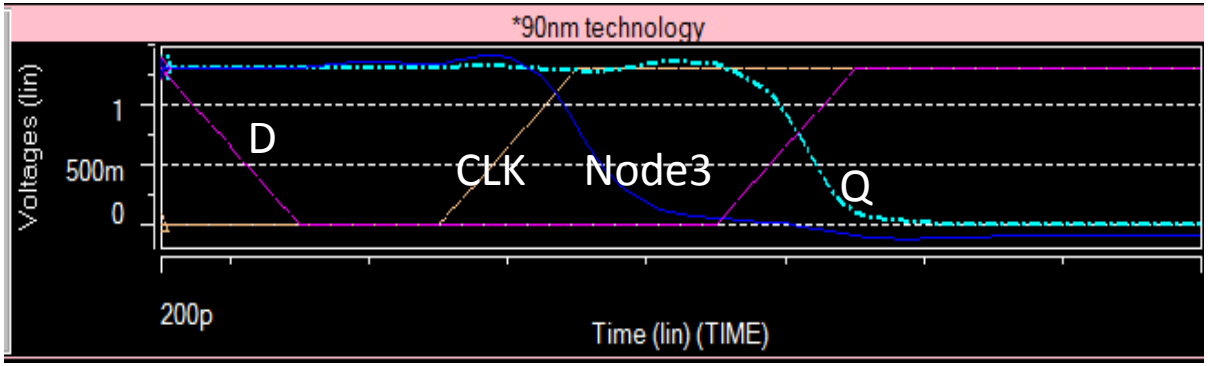


The internal node fail to compete with Q and the result is flipped back

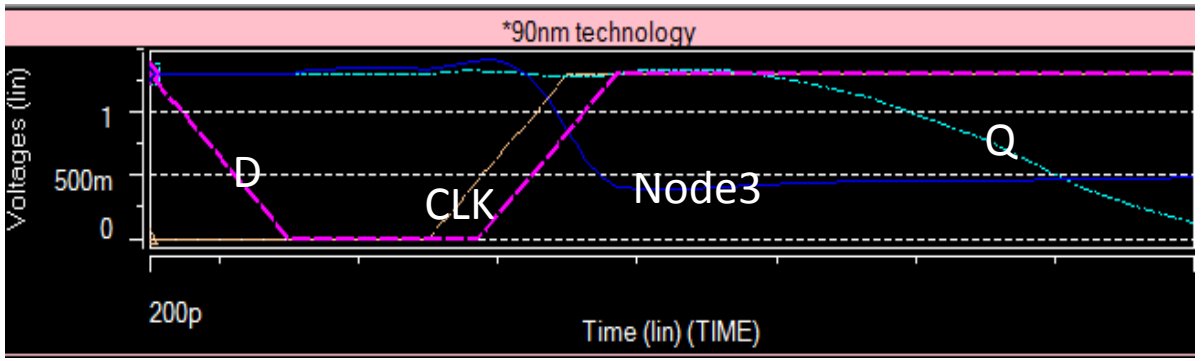


D Flip-Flop transient response

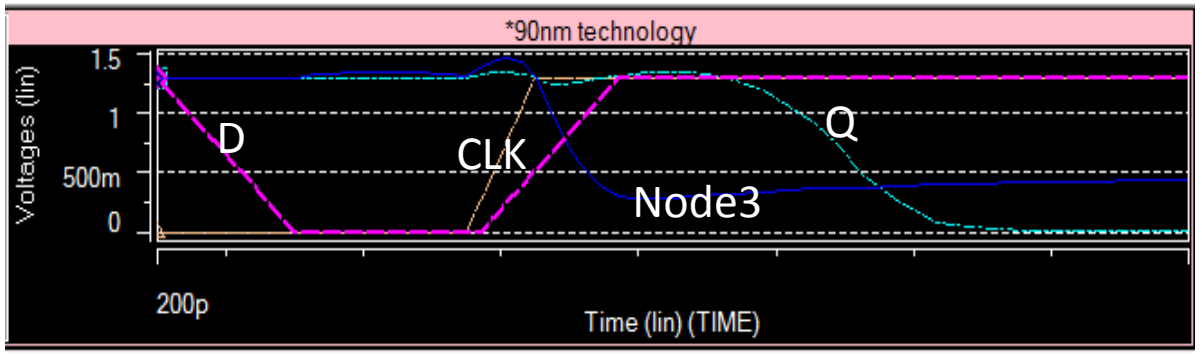




Hold time Violation:
the Node 3 was raised due to the arriving new data



Clock slope effect:
Same hold time, but steeper Clk will yield a small Clk-Q delay



Reference

[1] W. Roethig, “Library Characterization and Modeling for 130 nm and 90 nm SOC Design,” *Proceedings of the IEEE International SOC Conference*, pp. 383–386, September 2003.

[2] S. Sundareswaran,“Statistical Characterization For Timing Sign-Off: From Silicon to Design and Back to Silicon,” Doctorial thesis of the University of Texas at Austin, 2009

[3] Salman, E.; Dasdan, A.; Taraporevala, F.; Kucukcakar, K.; Friedman, E.G.; , "Pessimism reduction in static timing analysis using interdependent setup and hold times,"*Quality Electronic Design, 2006. ISQED '06. 7th International Symposium on* , vol., no., pp.6 pp.-164, 27-29 March 2006

[4] J. Bhasker and Rakesh Chadha, “Static Timing Analysis for Nanometer Designs: A Practical Approach. Springer,” first edition, April 2009.

[5] K. Yang, “Clocking Methodology and Flip-Flops,” EE215B lecture note, Winter 2010

[6] Srivastava, S.; Roychowdhury, J.; , "Rapid and Accurate Latch Characterization via Direct Newton Solution of Setup/Hold Times," *Design, Automation & Test in Europe Conference & Exhibition, 2007. DATE '07* , vol., no., pp.1-6, 16-20 April 2007

[7] Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic´, “Digital Integrated Circuit”, Secnod Edition, 2002

[8] Wikipedia, “Flip-flop (electronics)” http://en.wikipedia.org/wiki/Flip-flop_(electronics)