UCLA

SPIE'11 Review

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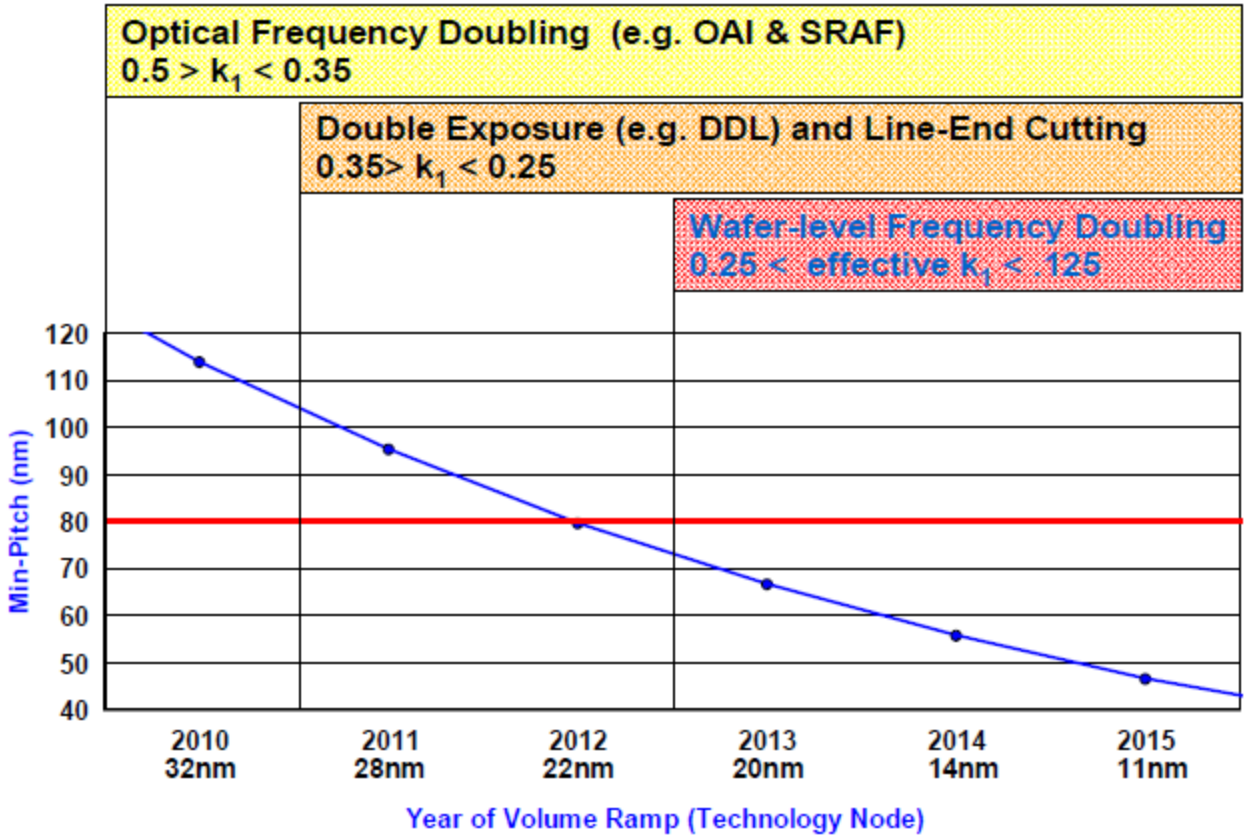
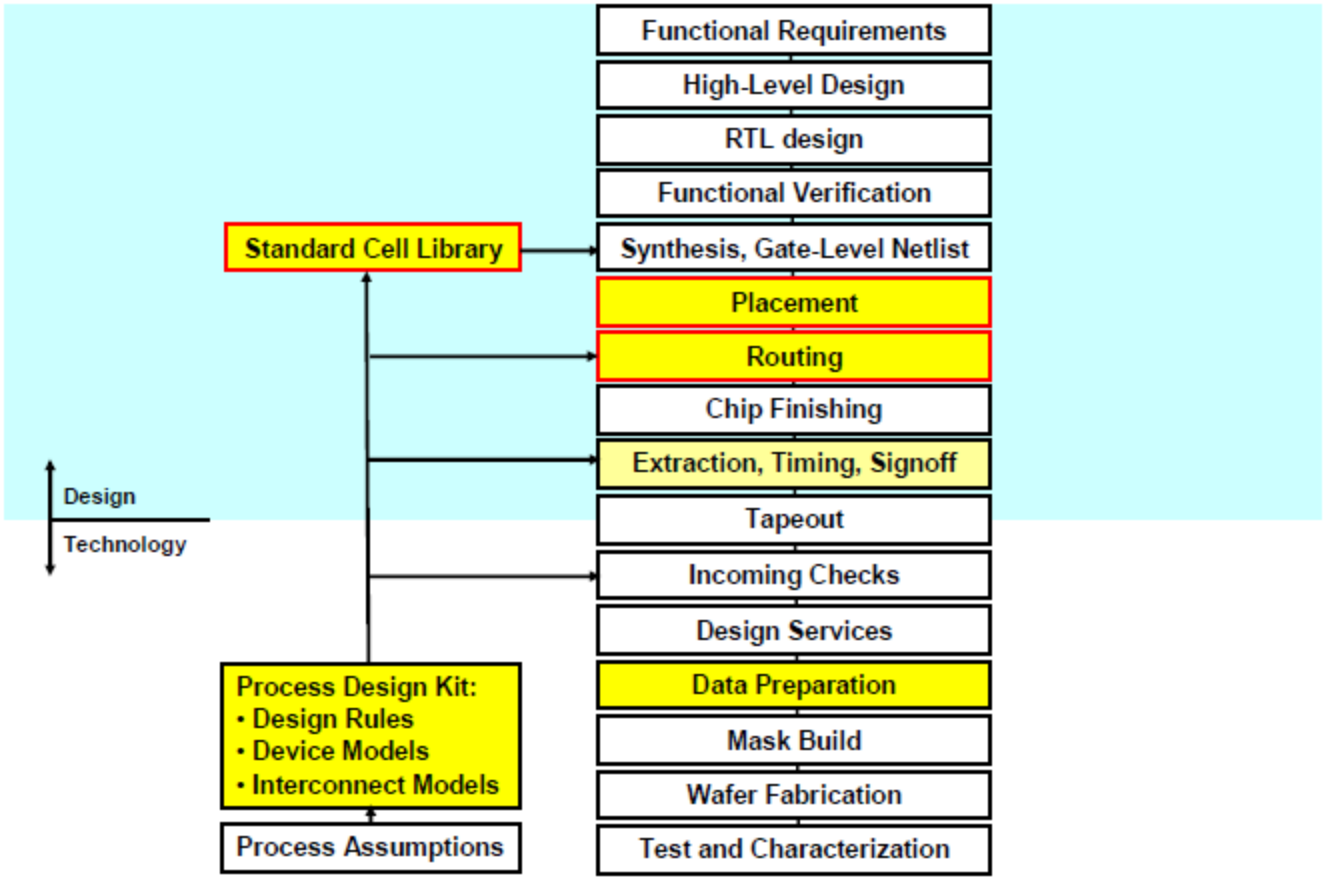
Decomposition-Aware Standard Cell Design Flows to Enable DPT *(IBM)*

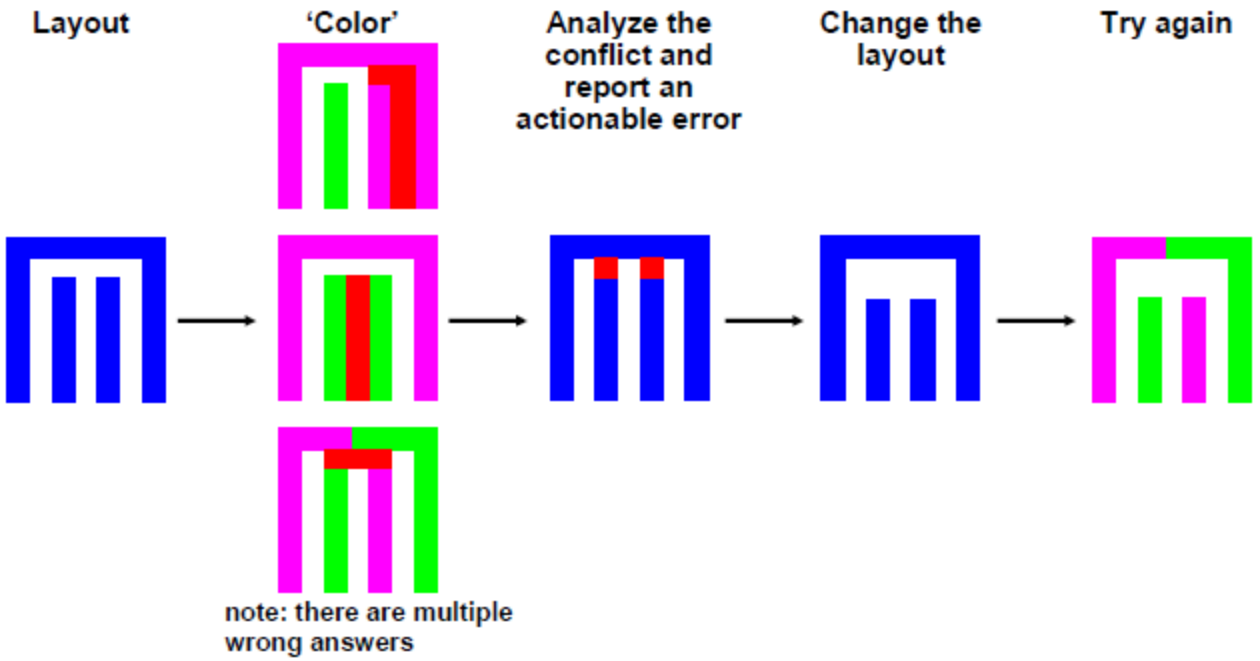


- DPT unavoidable below 80nm pitch

Design-Flow Components Affected by DPT

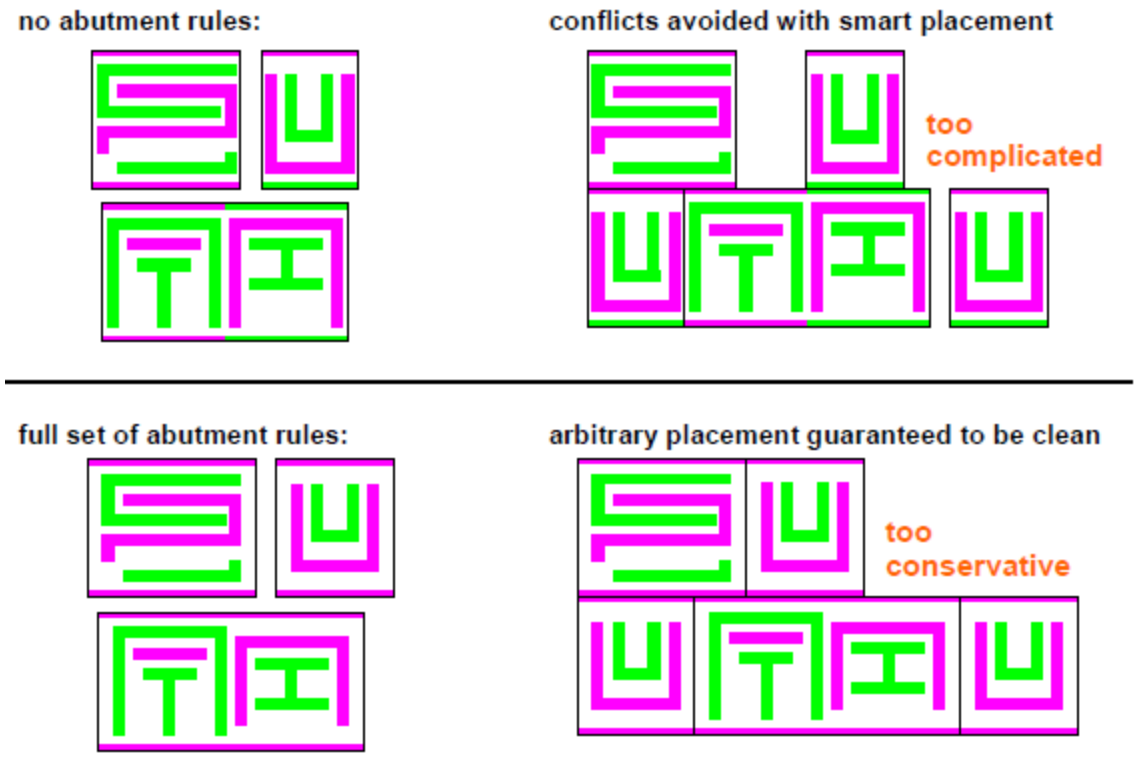


DP Decomposition and Issues



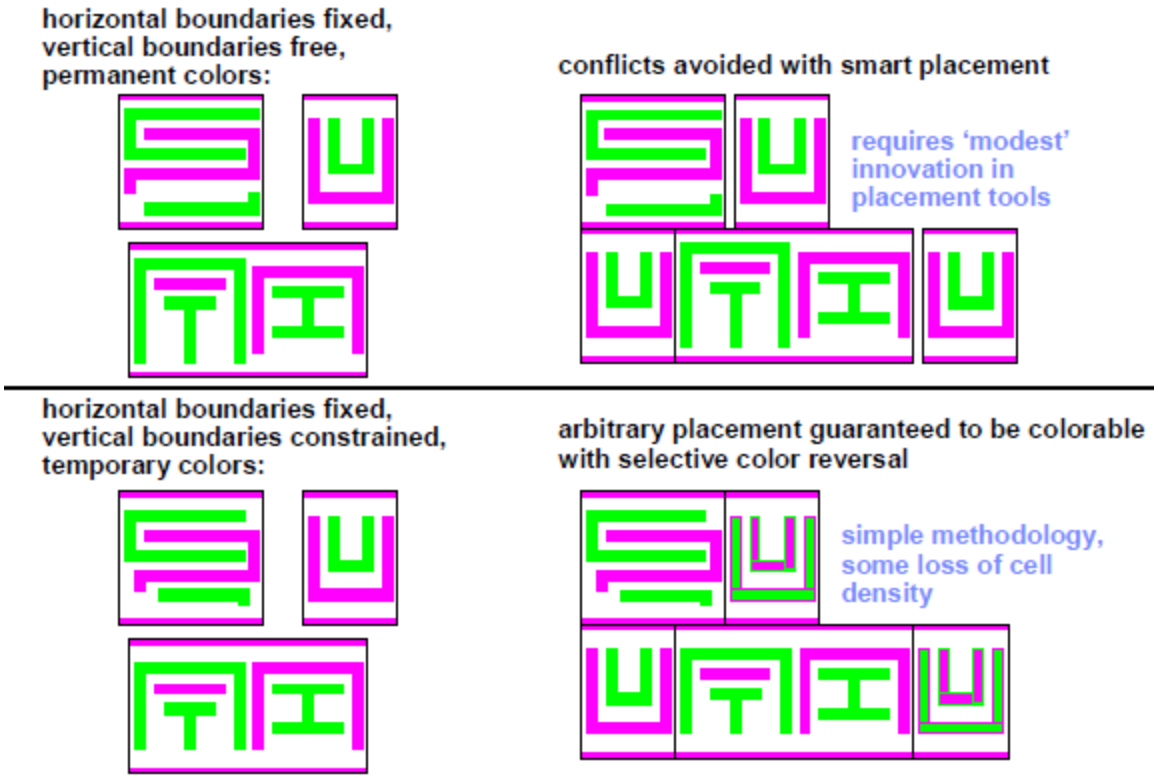
- Need DP decomposition that will eliminate layout legalization inefficiency
  - Decomposition for easy-to-fix conflicts (work in progress)

DP Placement – Extreme approaches



15% area overhead with 50% logic-cell util

DP Placement – Hybrid Approaches

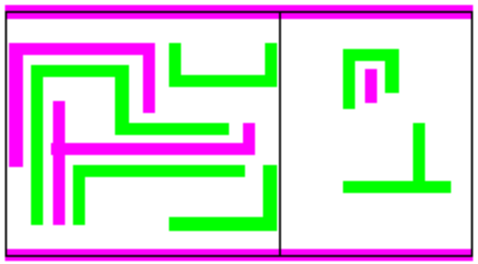


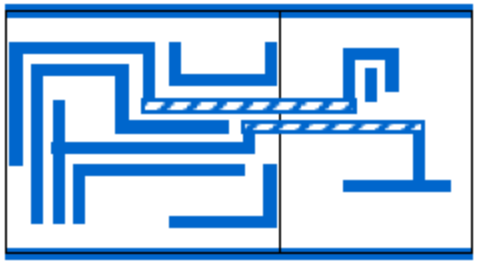
As low as 2-3% area overhead

Some infeasible cells, need large cell-height

1. Only worry about conflicts at vertical boundary, by either filler cells or flipping color (if possible)
2. Power pre-assigned, cell right forced to one color, flippable color w.r.t. power
   - Post-placement coloring or have two versions for each cell and placer chooses

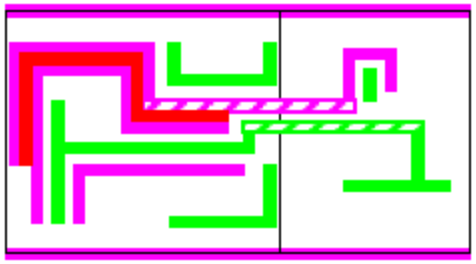
DP Routing

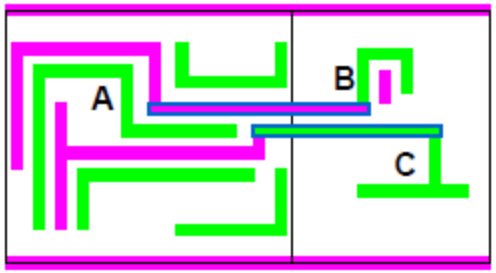


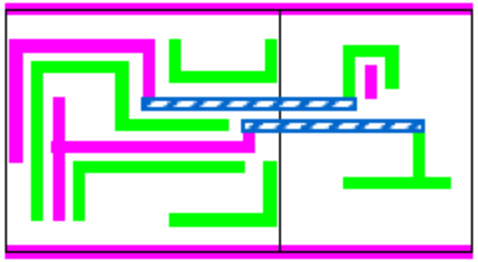


1) re-color after routing:

introduces errors in previously clean cells

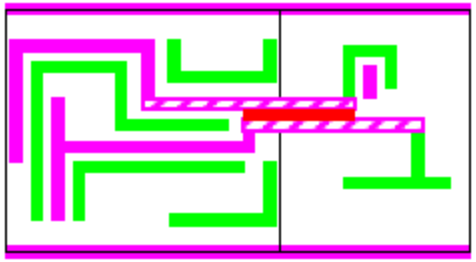


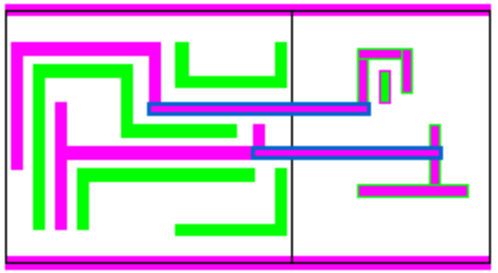




2) rigidly anchor router-colors to cell-level colors:

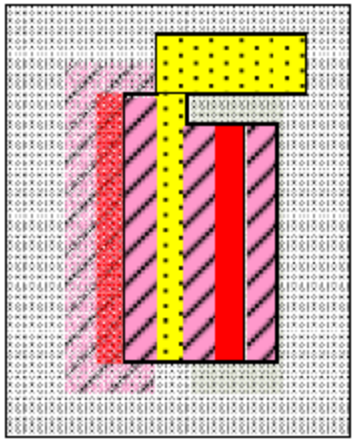
over constrains the routing challenge

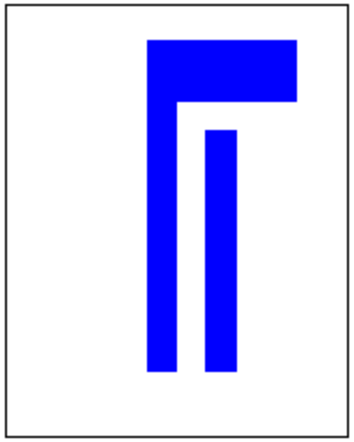




- Typical iterative optimization involving cycles of coloring, checking, locally re-routing, re-coloring, and re-checking.
- *"To avoid additional routing complexity from DPT, initial design flows will prevent routers from sharing wiring levels that are used predominantly in the cell level design." (also with globalfoundries)*
  - Eliminates DPT specific cell-to-router issues
  - May not be a long term solution

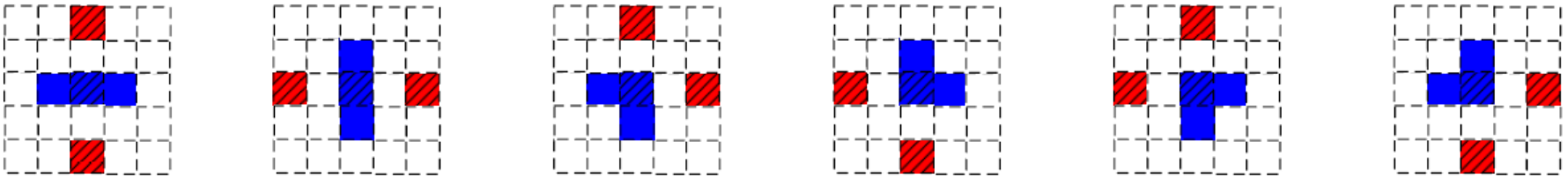
SADP Friendly Detailed Routing *(Mentor)*





- RMT bits
- Routing variable (R):
  - 1 → already occupied and routing blockage grids
- Mandrel-blocked variable (M):
  - 1 → conflicting on mandrel
- Trim-blocked variable (T):
  - 1 → conflicting on trim

Some Details



- Protective grid: trim grids that can provide assist spacer if filled with mandrel
- Bare grid: **occupied** trim grid is bare if its protective grids are “don’t cares”
  - Assign to trim or mandrel?
- Calculate hesitation parameters for each grid (likelihood)
- Heuristic to find path with best cost for each net (min WL, WL on each mask)

Table 2: Performance comparison between SADP-blind approach and SADP-DR

Design	Area (μm^2)	Nets	Router	Wirelength (nm)	SADP statistics (nm)				Runtime ($sec.$)	Ratio	
					M	PT	BT	Failure		BT	time
d1	410.292	672	blind-DR	8352	5344	984	1448	576	30.2	0.33	1.59
			SADP-DR	8416	3584	4320	512	96	48.3		
d2	5581.594	10891	blind-DR	43713	21729	5632	10208	61444	1523.88	0.3	1.65
			SADP-DR	44512	20416	20544	3552	1024	2517.9		

Double Patterning Compliant Logic Design *(Globalfoundries, cadence, AM)*

Litho-Etch-Litho-Etch		
Begin	TiN Metal Hardmask	
2	Scanner	ASML 1950i NXT
7	Scanner	ASML 1950i NXT
End	Queued for Via litho	

Sidewall Spacer SADP		
Begin	TiN Metal Hardmask	
2	Scanner	ASML 1900i
4	Spacer Dep	PE-ALD on SOC
8	Scanner	ASML 1900i
End	Queued for Via litho	

- 1900i cheaper less overlay accuracy
- 1950i slightly better throughput → almost same cost
- Spacer deposition → $14-$22 more per 12” wafer for 4 metal layers
  - Need 0.5%-1% less die area for same overall cost