Calibration of Setup and Hold time for Latches and Flip-flops

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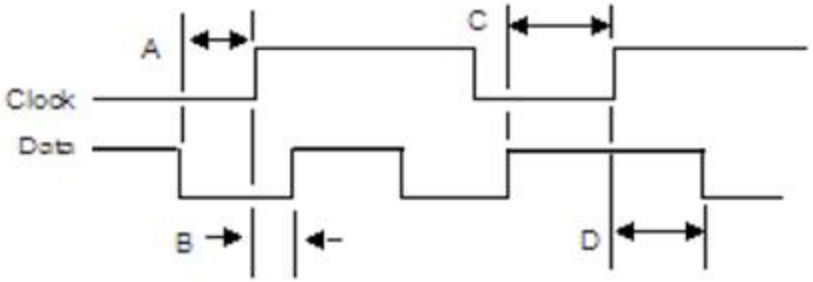
Outline:

1. Definition of setup and hold time
2. Measurement methodology
3. Library file formulation
4. Library characterization tools
5. Reference

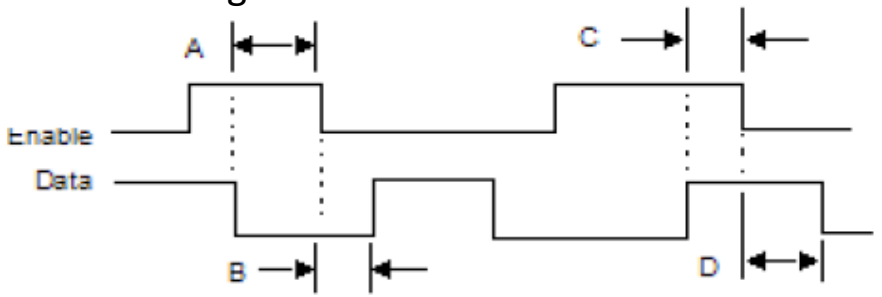
Definition of Setup and Hold Time

Setup and Hold Times Specification for Rising-Edge-Triggered Flip-Flop



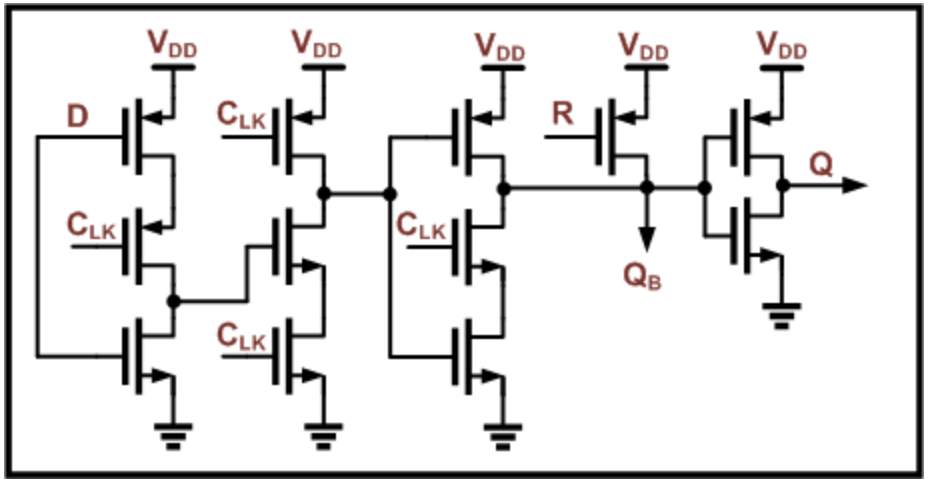
A = data-low setup time
B = data-low hold time
C = data-high setup time
D = data-high hold time

Setup and Hold Sepcification for High-Enable Latch



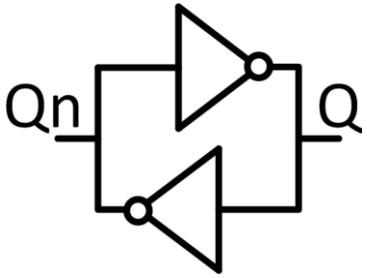
A = data-low setup time
B = data-low hold time
C = data-high setup time
D = data-high hold time

[1]

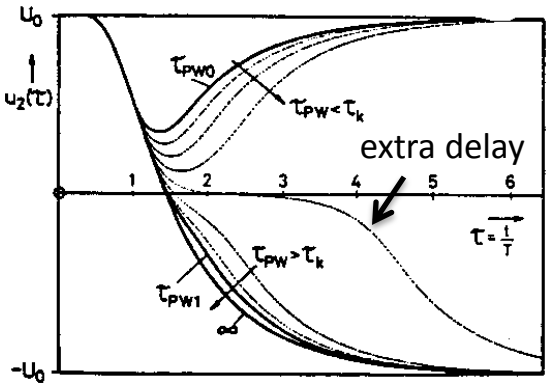


Conventional TSPC Flip-Flop Design [2]

When Violating the Setup or Hold Constraint :

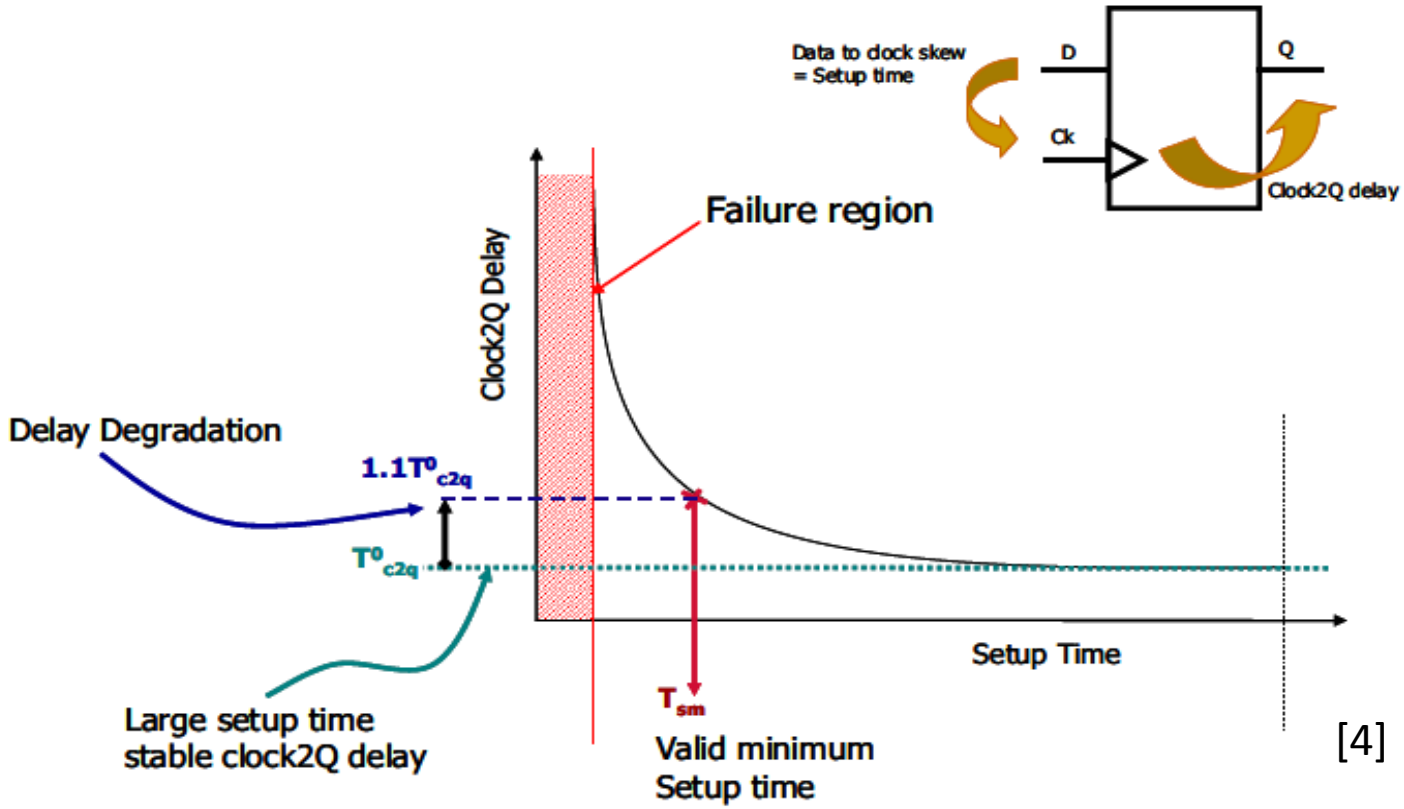


Voltage Keeper



Will cause Clock-Q delay to increase or even flip the Output [3]

Measurement Methodology(1/3)

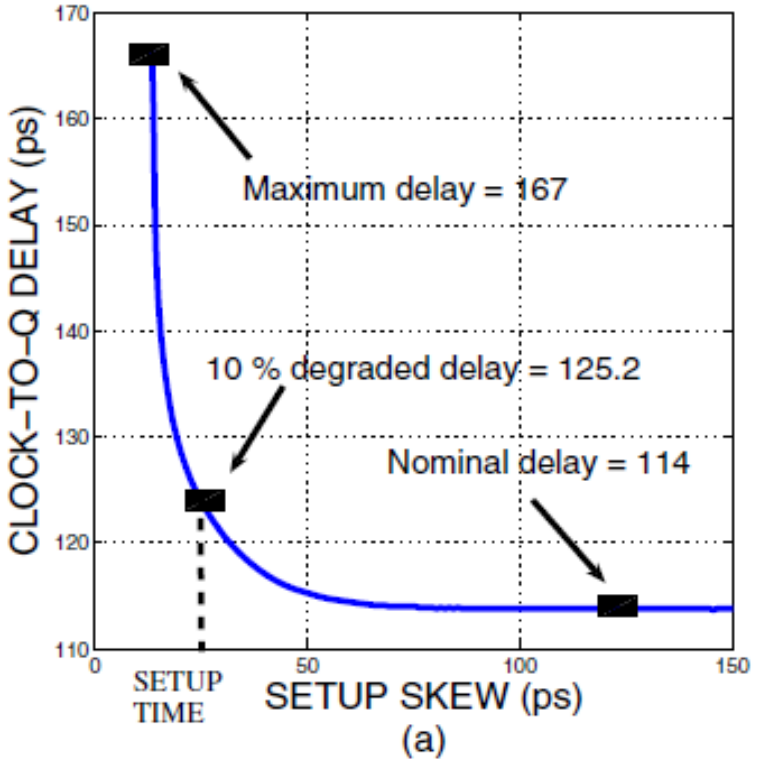


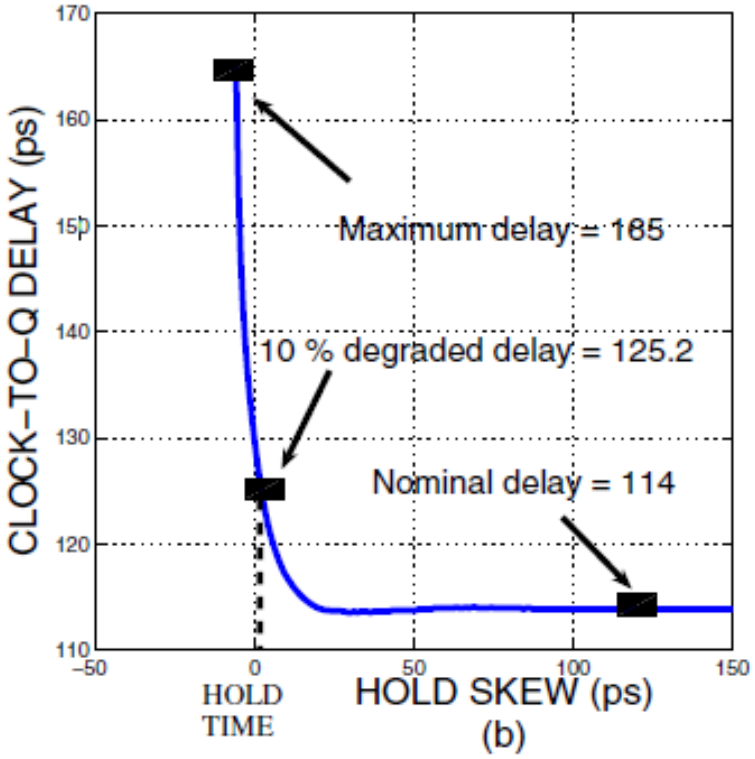
[4]

Approaches for setup and hold time determination: [4]

1. Minimizing T_setup +T_hold with some given delay allowance
2. Minimizing T_setup + T_clk2Q [5] -> Maximize the Perfomance
3. (Industrial approach) 5-10% degradation in the minimal possible T_clk2Q delay

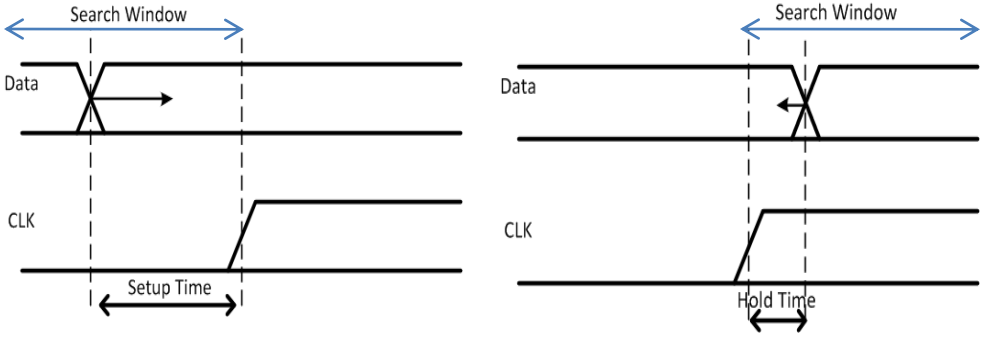
Measurement Methodology(2/3)





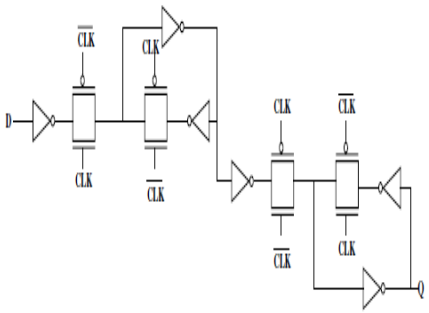
[7]

Measurement Methodology(3/3)

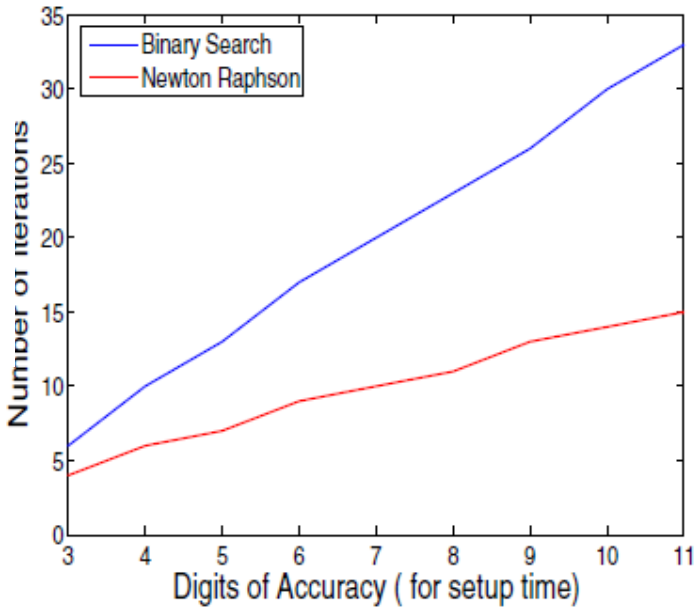


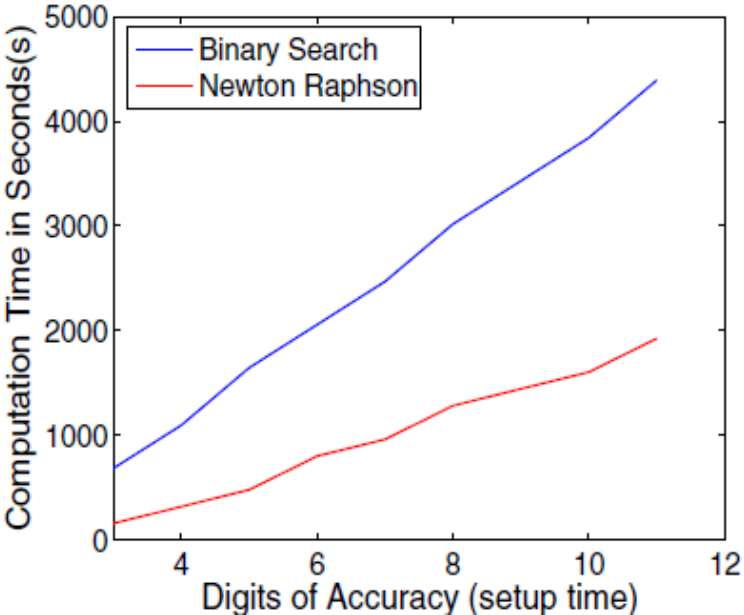
Searching methodologies for critical skew for the onset of metastability

1. Binary search (Mostly applied) : mouths of runtime for enterprise libraries[5]
2. Using Newton-Raphson method to solve Differential Equations of Metastability[6]
   4x ~ 10x faster



A Transmission Gate Based Positive-edge triggered master-slave register





Library File Formulation

To be calibrated:
setup_rising, setup_falling,
hold_rising, or hold_falling

```
pin (D) {
direction : input;
. . .
timing () {
related_pin : "CK";
timing_type : "setup_rising";
rise_constraint ("setuphold_template_3x3") {
index_1("0.4, 0.57, 0.84"); /* Data transition Time*/
index_2("0.4, 0.57, 0.84"); /* Clock transition Time*/
values( /* 0.4 0.57 0.84 */ \
/* 0.4 */ "0.063, 0.093, 0.112", \
/* 0.57 */ "0.526, 0.644, 0.824", \
/* 0.84 */ "0.720, 0.839, 0.930");
…
```

[10]

The table requires the 9 searching processes for different sets of indices

Setup time constraints for output rising case

Library Characterization Tools

LibDev *Specific* Software (~2008)[9]

Company	Layout	Characterization	Optimization	Verification
Altos Design Automation		Liberate		
Cadence		SignalStorm		
Fenix Design Automation				Crossfire
Legend Design Technology		CharFlo-Memory		
Library Technologies		LibChar	CellOpt, LowSkew	
Magma Design Automation		SiliconSmart		
Nangate	Library Creator	Library Creator, Library Characterizer	Library Creator	Library Creator, Liberty Analyzer
Prolific	ProGenesis			
Radix Tools		xlicdsm		Std. cell library characterization.
Sagantec	SiClone, SiFix		SiFix, DFM-Fix	
SIMUCAD Design Automation		AccuCell		
Synopsys	Cadabra	Liberty NCX	Circuit Explorer	Liberty parser, Liberty screener, Library Compiler
VeriPool		GSpice (free)		
Z Circuit		ZChar		Library Analyzer
Zenasis Technologies			ZenTime-CT	

Reference(1/2)

[1] W. Roethig, “Library Characterization and Modeling for 130 nm and 90 nm SOC Design,” *Proceedings of the IEEE International SOC Conference*, pp. 383–386, September 2003.

[2] Wikipedia, “Flip-flop (electronics)” http://en.wikipedia.org/wiki/Flip-flop_(electronics)

[3] K. Yang, “Clocking Methodology and Flip-Flops,” EE215B lecture note, Winter 2010

[4] S. Sundareswaran,“Statistical Characterization For Timing Sign-Off: From Silicon to Design and Back to Silicon,” Doctorial thesis of the University of Texas at Austin, 2009

[5] V. Stojanovic and V.G. Oklobdzija, “Comparative Analysis of Master- Slave Latches and Flip-Flops for High-Performance and Low-Power Systems,” *IEEE Journal of Solid-State Circuits,* Vol. 34, No. 4, pp. 536–548, April 1999.

[6] Srivastava, S.; Roychowdhury, J.; , "Rapid and Accurate Latch Characterization via Direct Newton Solution of Setup/Hold Times," *Design, Automation & Test in Europe Conference & Exhibition, 2007. DATE '07* , vol., no., pp.1-6, 16-20 April 2007

[7] Salman, E.; Dasdan, A.; Taraporevala, F.; Kucukcakar, K.; Friedman, E.G.; , "Pessimism reduction in static timing analysis using interdependent setup and hold times,"*Quality Electronic Design, 2006. ISQED '06. 7th International Symposium on* , vol., no., pp.6 pp.-164, 27-29 March 2006

[8] Srivastava, S.; Roychowdhury, J.; , "Independent and Interdependent Latch Setup/Hold Time Characterization via Newton–Raphson Solution and Euler Curve Tracking of State-Transition Equations," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* , vol.27, no.5, pp.817-830, May 2008

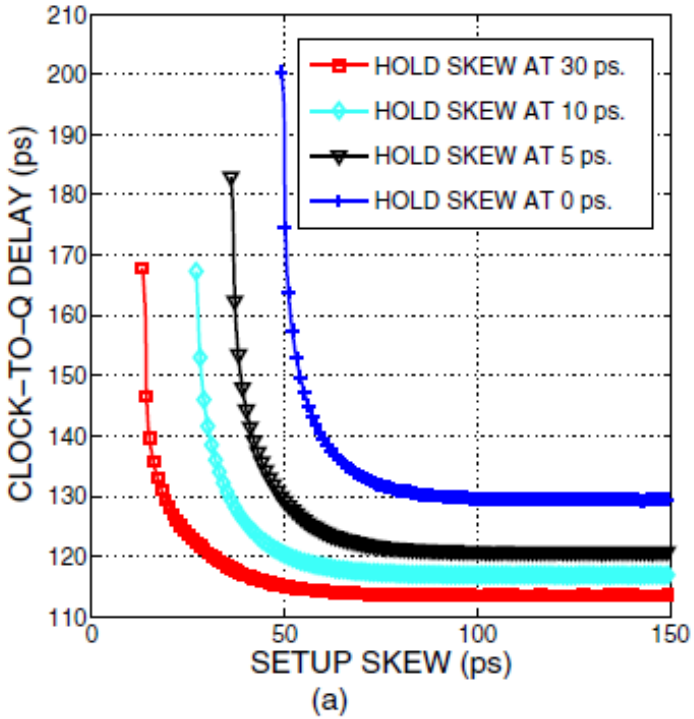
Reference(2/2)

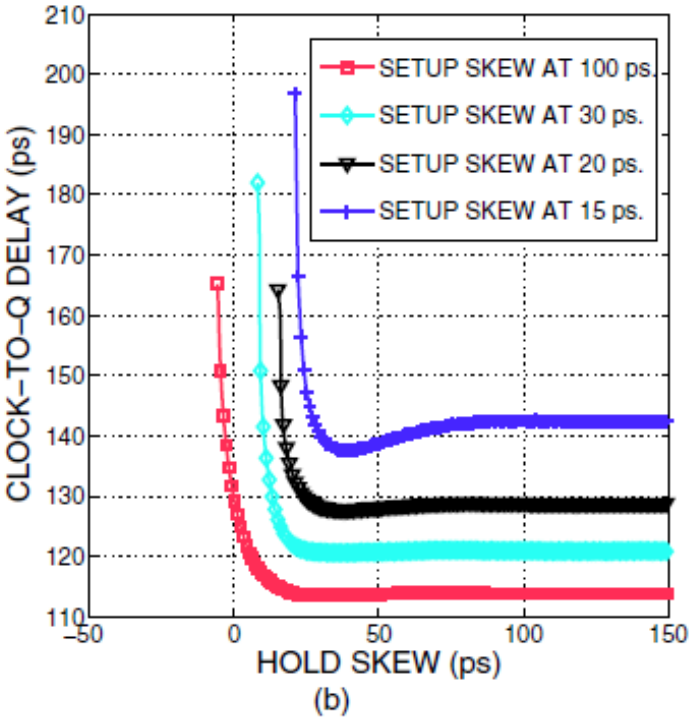
[9] Review of Library Develop tools in the personal website of Oleg S. SEVALNEV : http://olegsevalnev.tripod.com/

[10] J. Bhasker and Rakesh Chadha, “Static Timing Analysis for Nanometer Designs: A Practical Approach. Springer,” first edition, April 2009.

Related Study

- Setup and Hold Time interdependence Modeling in Static Timing Analysis [7][8]





Require more SPICE simulation