UCLA

Thermal Issues for 3D ICs

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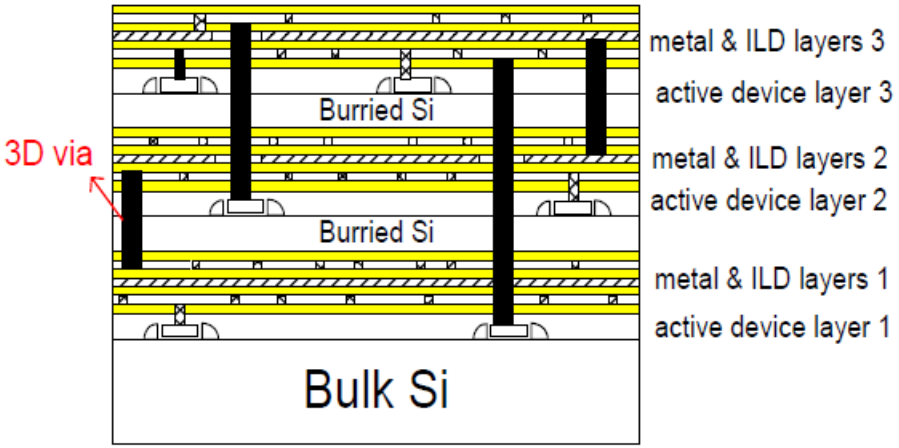
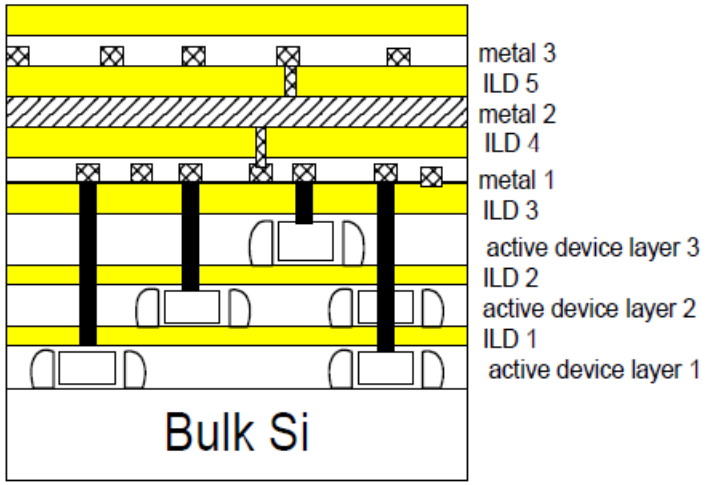
Outline

- 3D IC
- Thermal Analysis
- Heat Removal in 3D ICs
- Thermal Mitigation Methods

Three-Dimensional ICs



Face-to-Back Wafer-Bonding



Multi-layers Burried Structure

Wafer-bonding technology connects active device layers after processing each active device layer separately
while MLBS sequentially processes layers of active devices (transistors) before processing all the metal routing layers.

Thermal Analysis

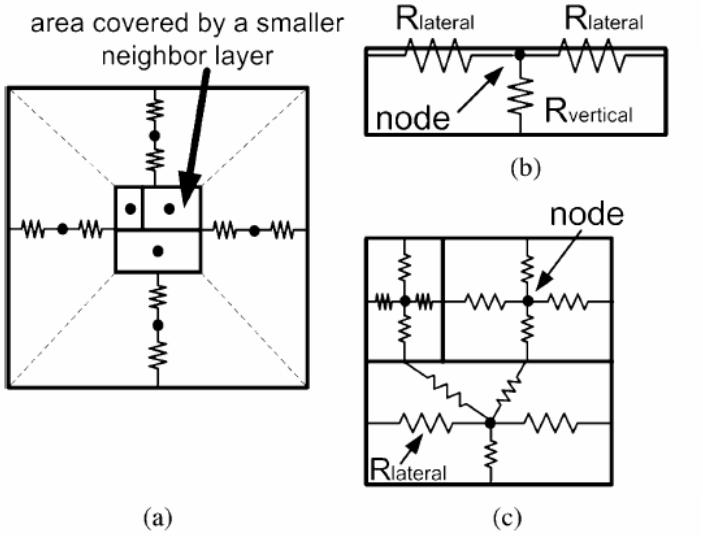
- Analogies between
  thermal parameters & electrical parameters

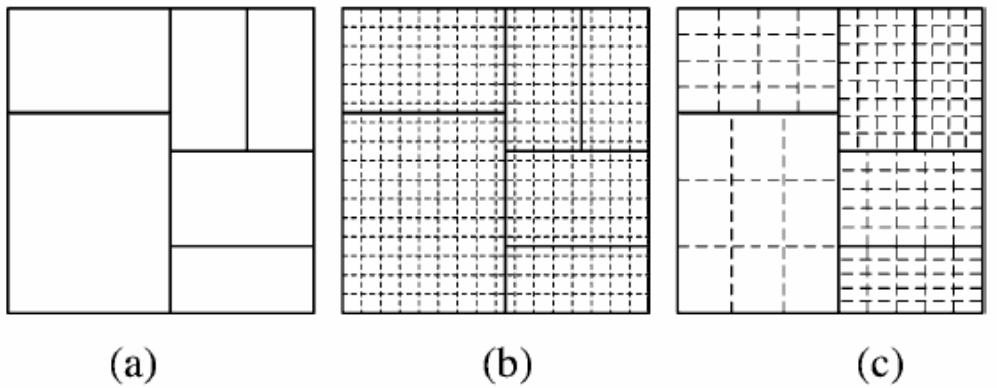
Thermal Parameter	Circuit Parameter
Temperature (T)	Voltage (V)
Heat Flow	Current (I)
Thermal Conductivity	Electrical Conductivity (σ)

- Thermal Analysis :
  Solve Partial Differential Equations (PDEs)

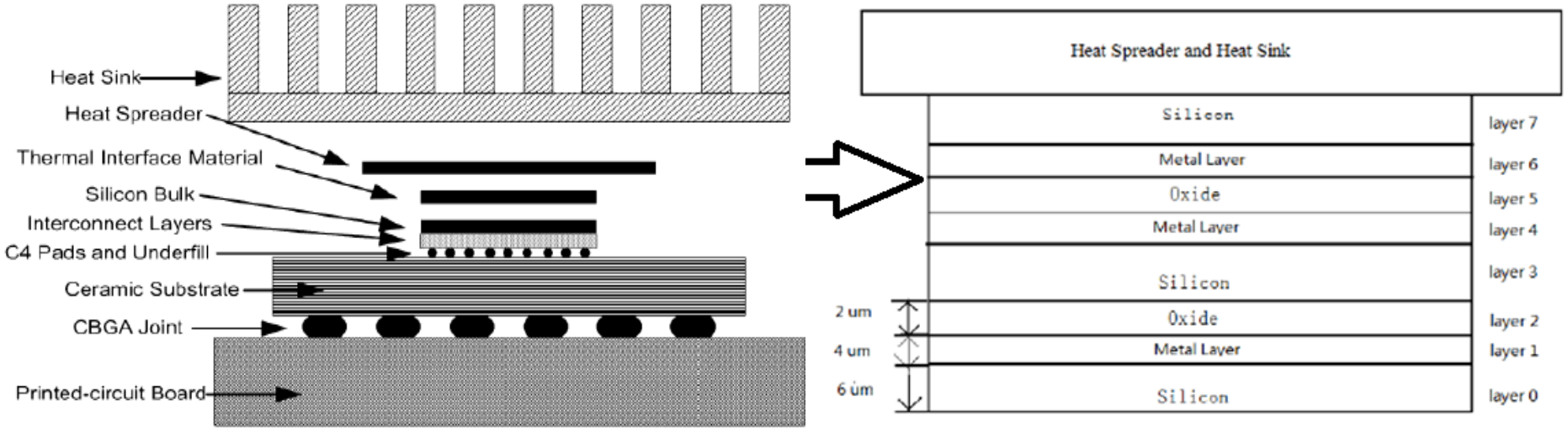
Thermal Analysis

- Thermal Modeling
- Block-based vs. Grid-based





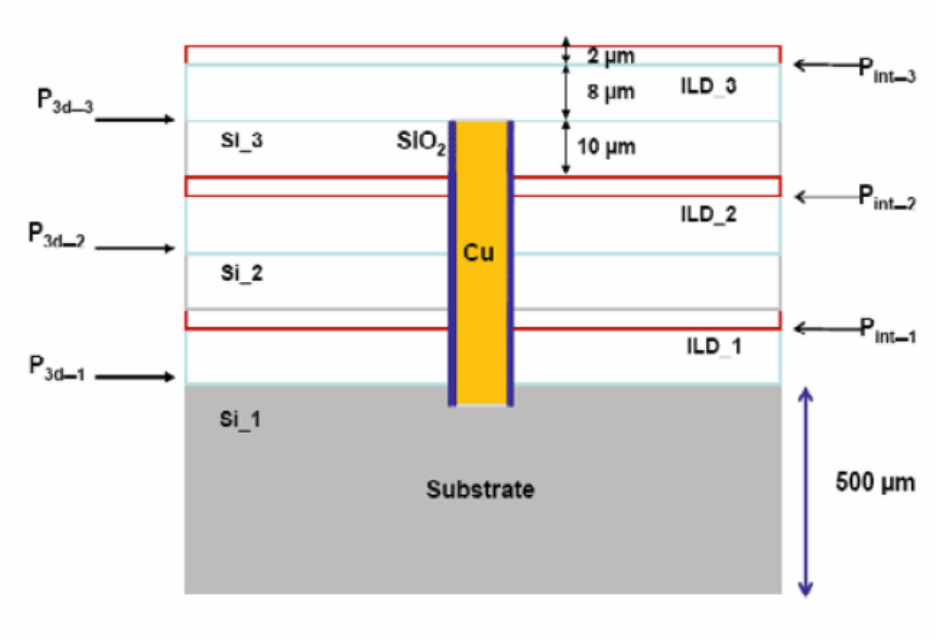
Heat Removal in 3D ICs



	Al	Oxide	Si
Thermal Conductivity (W/cm/K)	230	1.3	151
Density (g/cm^3)	2.7	2.2	2.65
Specific heat (J/kg/K)	900	740	710

Thermal Mitigation Methods

Thermal Through-Silicon Vias



Micro-fluid Channels (MFCs)

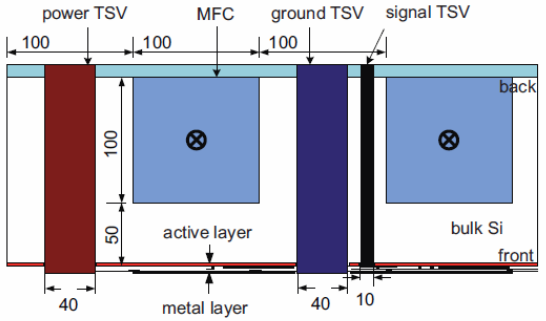


Fig. 3. Side view of a die layer in a stacked chip. The die is flipped over and the active layer is facing down. Shapes are drawn to scale. Unit is μm.

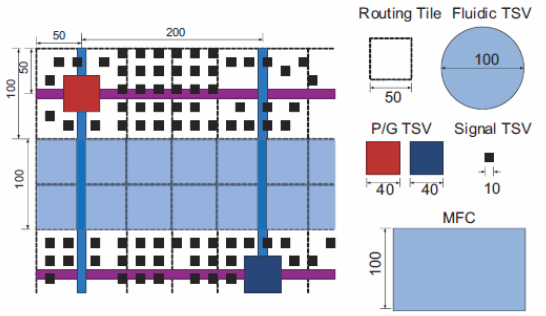


Fig. 4. Top view of the routing tile objects on routing grid. Objects are drawn to scale.

Reference

[1] Yuh-Fang Tsai, Yuan Xie, N. Vijaykrishnan, and Mary Jane Irwin, “Three-Dimensional Cache Design Exploration Using 3DCacti,”ICCD 05

[2] Wei Huang, Shougata Ghosh, Siva Velusamy, Karthik Sankaranarayanan, Kevin Skadron and Mircea R. Stan, “ HotSpot: ACompact Thermal Modeling Methodology for Early-Stage VLSI Design,” IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 14, NO. 5, MAY 2006

[3] Young-Joon Lee, Goel, R., Sung Kyu Lim, “Multi-functional interconnect co-optimization for fast and reliable 3D stacked ICs,” ICCAD, pp 645 – 651, 2009