

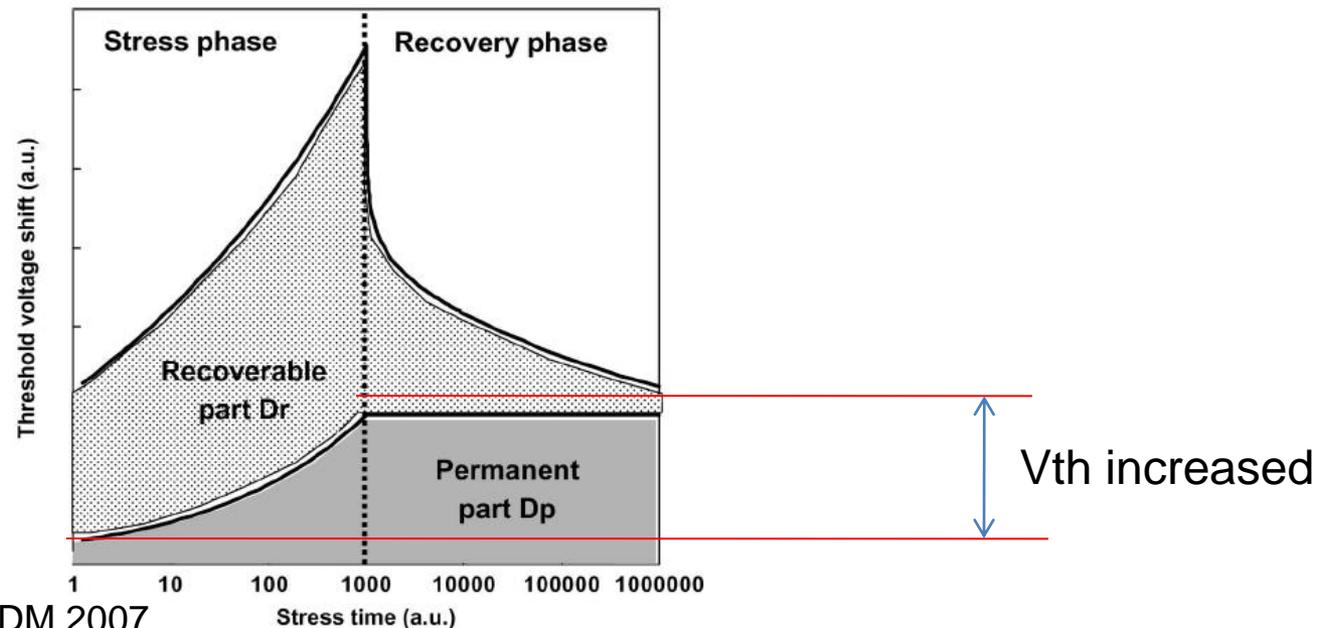
# *Introduction on NBTI*

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# What is NBTI ?

- NBTI : Negative Bias Temperature Instability
- $V_{th}$  varies on PMOS device
  - $V_{th}$  increase with negative bias,  $V_{gs} = -V_{dd}$
  - But recover with zero bias,  $V_{gs} = 0$

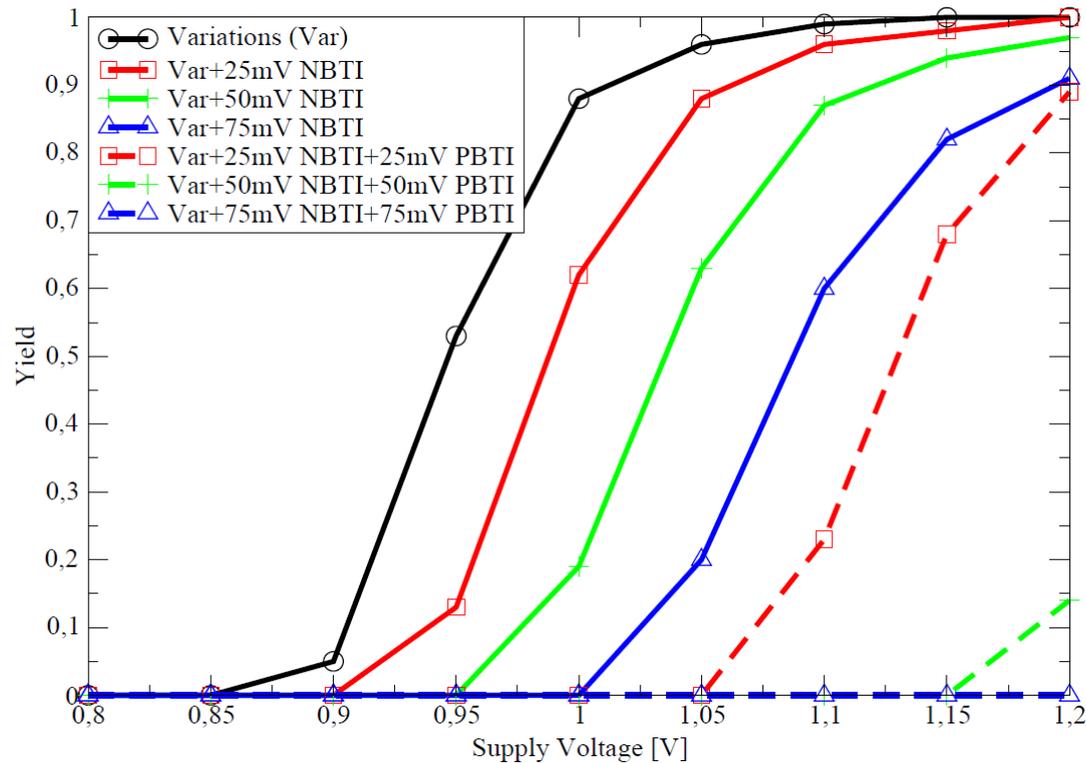


Source : Vincent Huard, IEDM 2007

# NBTI impact

- Wang, VLSI 2010
  - 7% to 10% frequency degradation on benchmark circuits
- Mangalagiri, ICCAD 2008
  - 5% to 10% delay degradation in FPGA due to NBTI (PTM model)
  - 1% delay degradation for process with hi-Vt and thick oxide.
- Neeraj, IEDM 2005
  - Degradation depends on configuration and application.
  - $V_{\text{error}} > 7 \text{ mV}$  (maximum allowed error=7.8mV) for a 64 bit DAC.
- J.C. Lin, IEDM 2006
  - SRAM read margin decrease as a result of NBTI stress.
  - Limit NBTI impact using a less “read margin” dominant design.

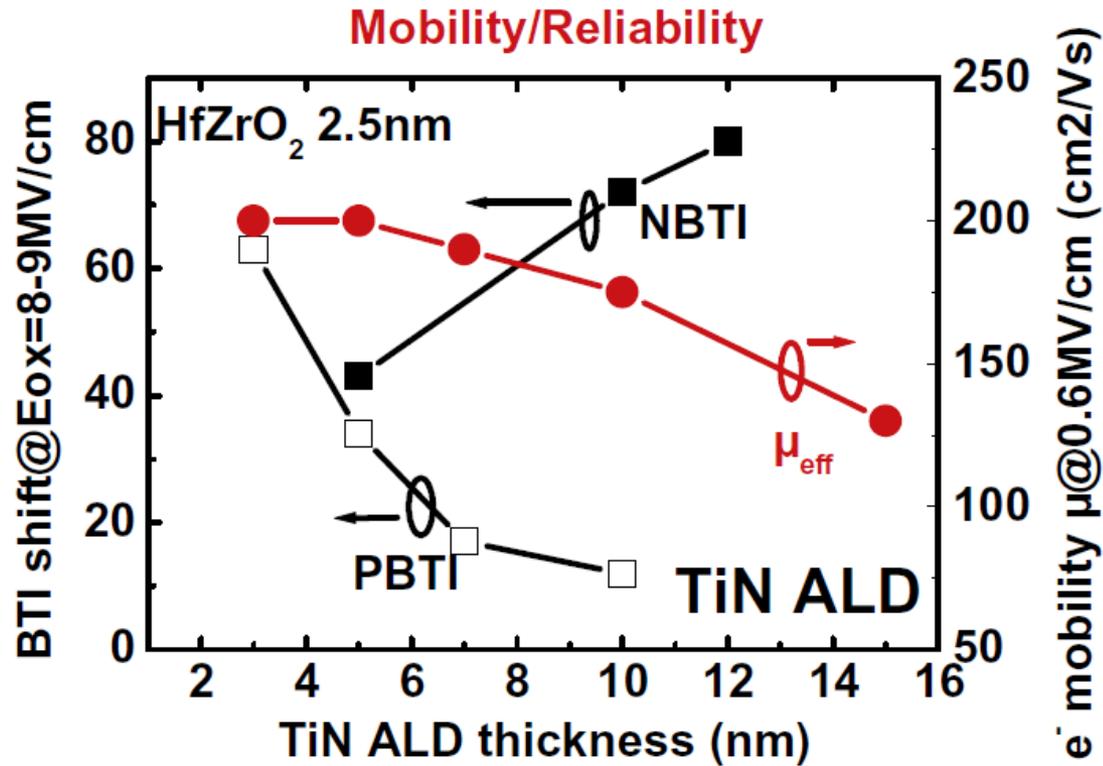
# Impact on SRAM



Drapatz, *Journal Advances in Radio Science*, 2009

- NBTI shows noticeable impact on SRAM yield
- Yield loss is huge considering NBTI + PBTI

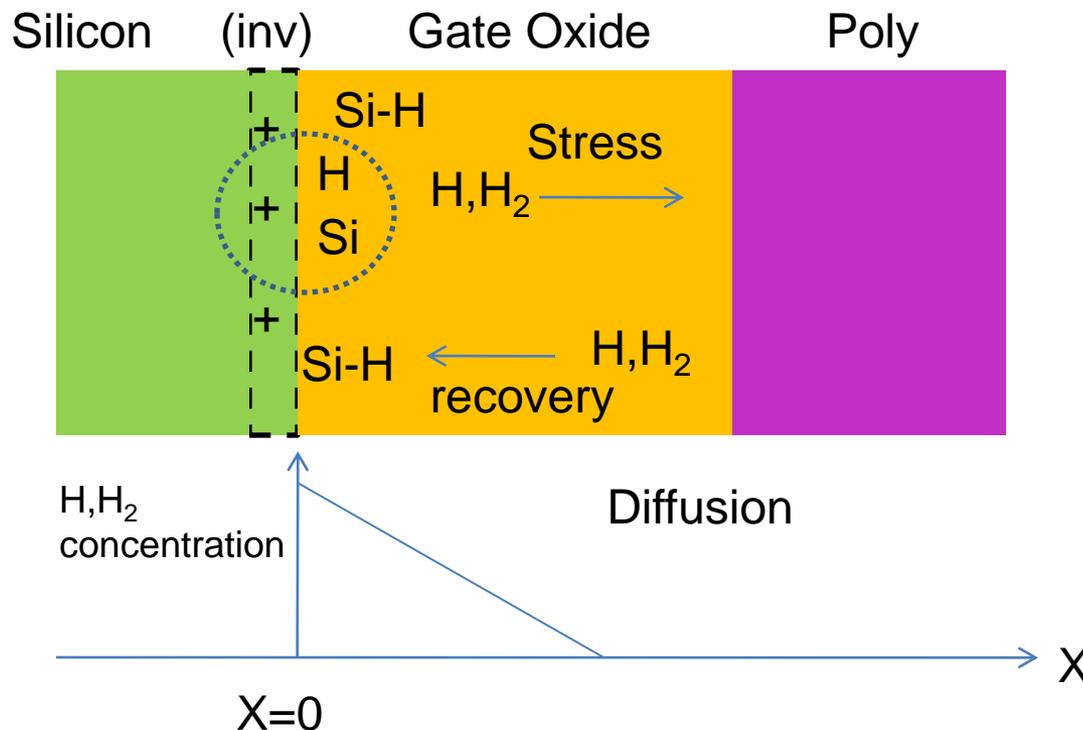
# NBTI vs PBTI



- trade-off between NBTI/PBTI and metal gate thickness

# Reaction-diffusion model

- Interface traps is generated when device is stressed (negative bias)



# Differential Equations for NBTI

$$\frac{dN_{IT}}{dt} = k_F(N_o - N_{IT})P - k_R N_H N_{IT} \quad \text{Reaction}$$

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} \quad \text{Diffusion}$$

## Analytical model

$K_v$  is proportional to Temperature

Stress

$$\Delta V_{th}(t) = (K_v(t - t_0)^{1/2} + \sqrt[2n]{\Delta V_{th}(t_0)})^{2n}$$

$2n=1/3$  for reaction dominant by  $H_2$

Recovery

$$\Delta V_{th}(t) = \Delta V_{th}(t_1) \left( 1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t-t_1)}}{(1 + \delta)t_{ox} + \sqrt{Ct}} \right)$$

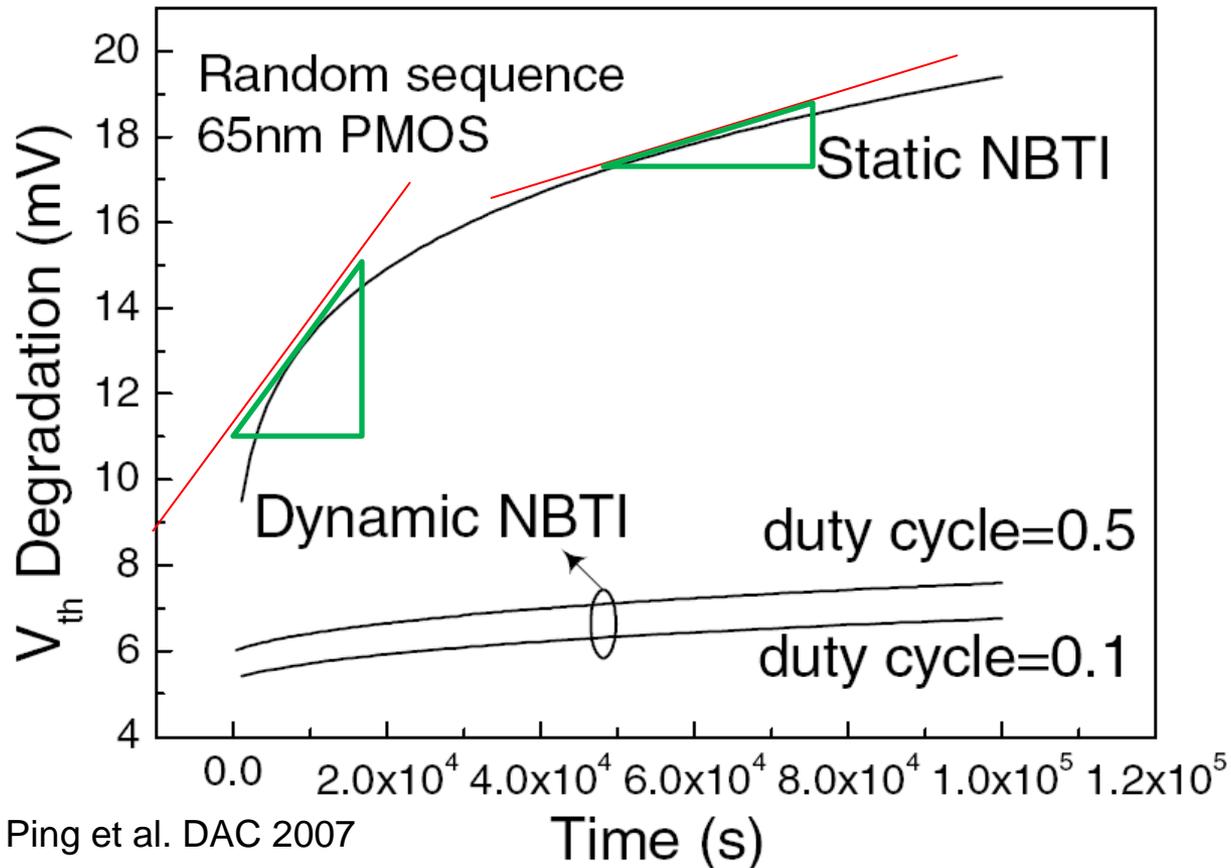
Recovery factor  
Related to

Source : W. Ping et al. DAC 2007

# NBTI Characteristics

- NBTI degradation is front-loaded
- Frequency dependent or independent ?
- $V_{gs}$  dependence
- $V_{th}$  variation reduction due to NBTI

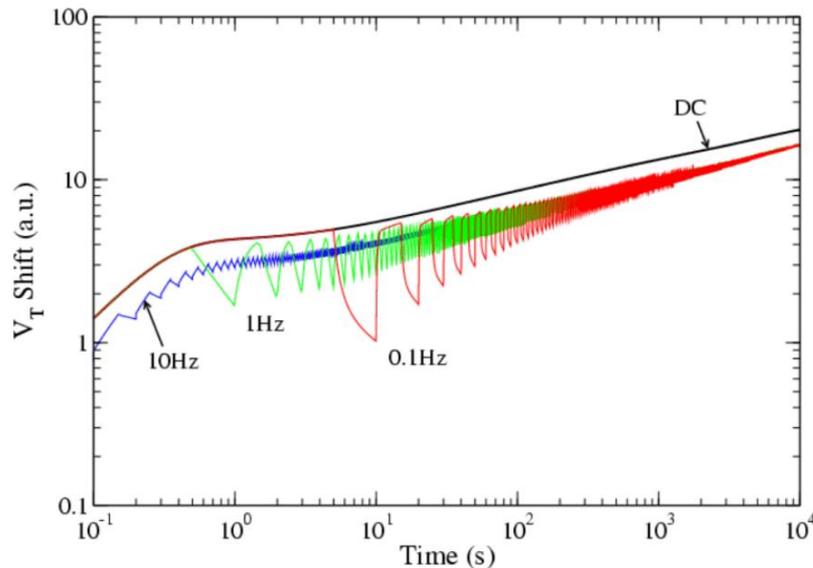
# Front Loaded Degradation



Source : W. Ping et al. DAC 2007

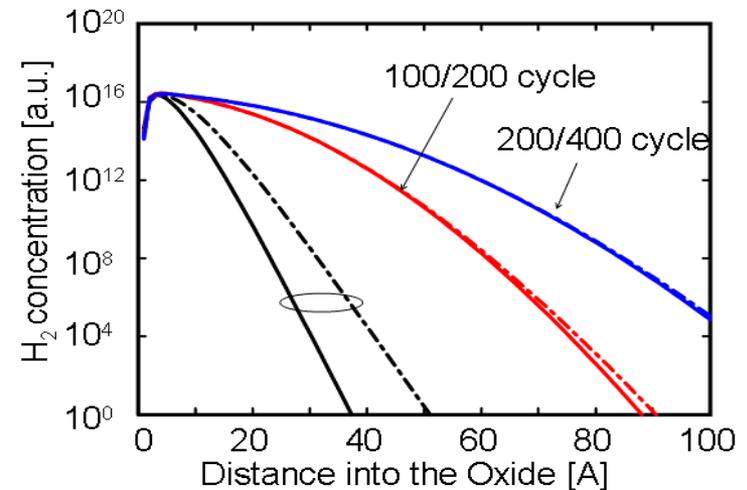
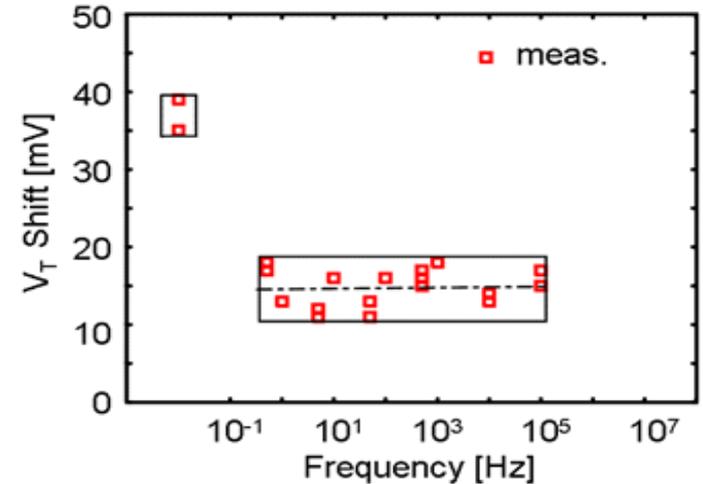
- Degradation rate is steep at the beginning but slows down rapidly

# Frequency independence



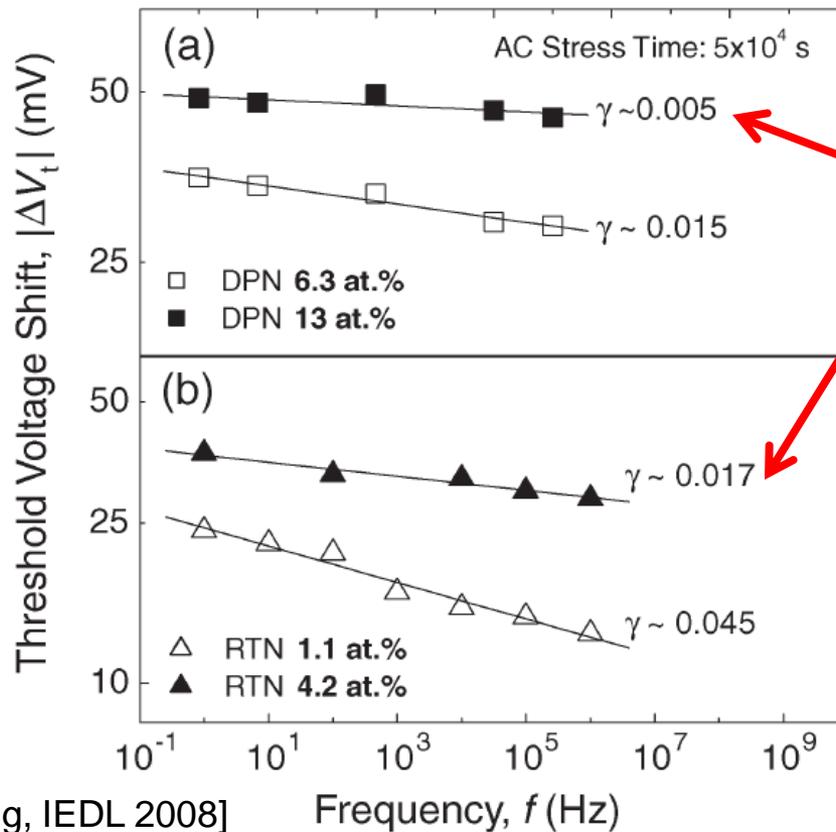
<http://www.iue.tuwien.ac.at/phd/wittmann/node10.html>

- RD model predicts frequency independence [Alam, IEDM 2003]
- Contradict observations are found in



# Frequency Dependence

- DPN : decoupled-plasma-nitrided SiO<sub>2</sub>
- RTN : rapid-thermal-nitrided SiO<sub>2</sub>

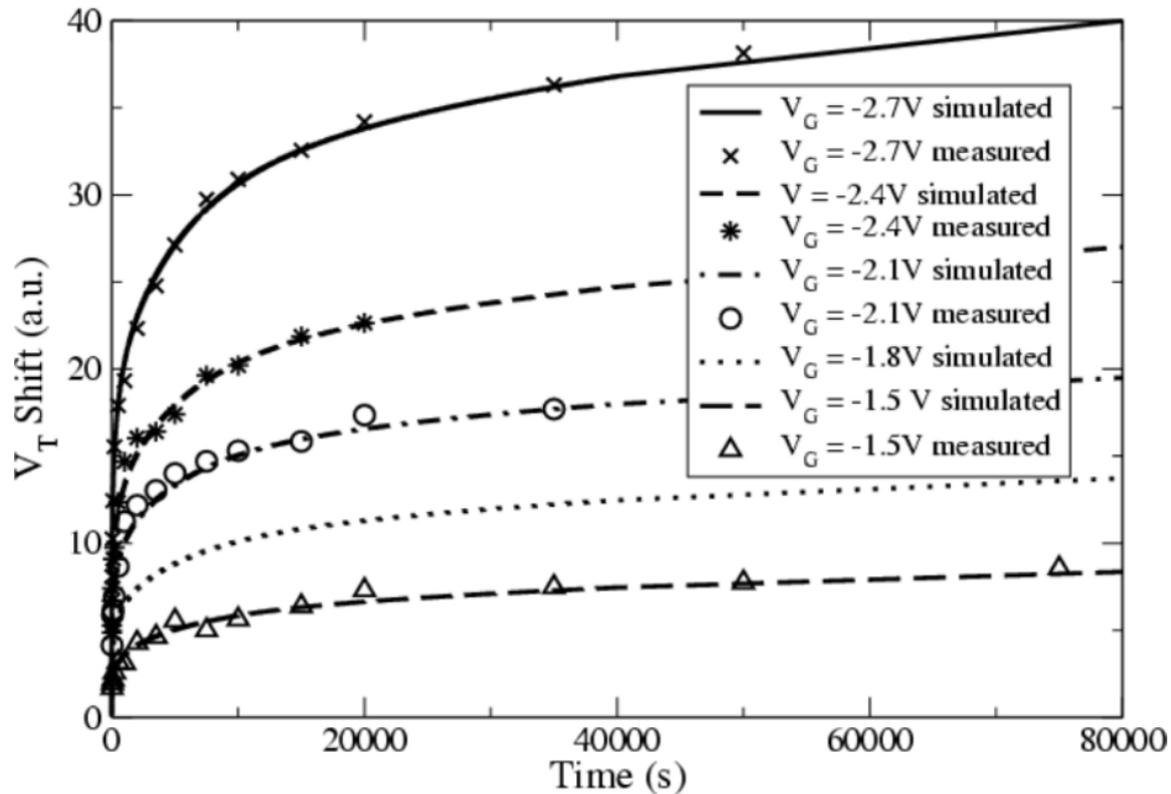


increased nitrogen concentration in gate oxide results weaker frequency dependence

- Frequency dependence is due to deep level holes
  - holes have enough time to generate interface traps during low freq.

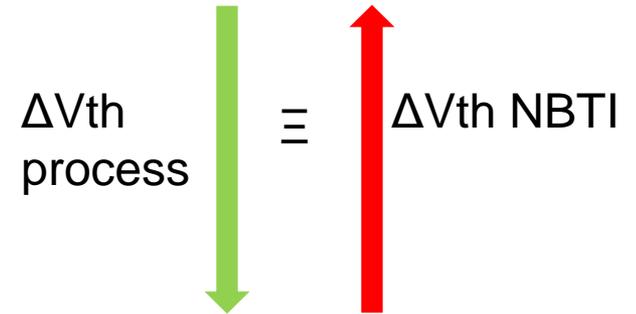
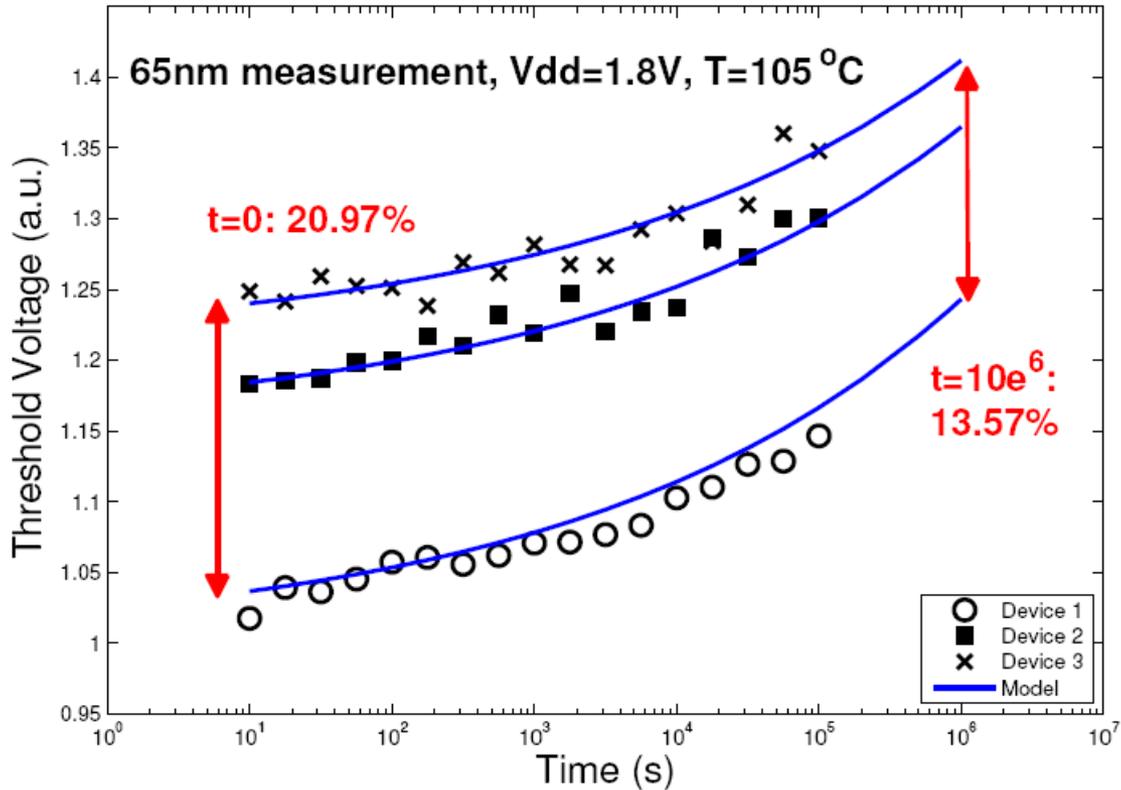
[Wang, IEDL 2008]

# NBTI vs $V_{gs}$



- $\Delta V_t$  increase exponentially with increasing  $V_{gs}$

# NBTI and $V_{th}$ Variation



$\Delta V_{th}$  process +  $\Delta V_{th}$  NBTI

$\Rightarrow$  Overall process variation reduced

Source : W. Ping et al. DAC 2007

# On-going Studies on NBTI

- Modeling and characterizing NBTI
  - Physical mechanism of NBTI
  - Measuring NBTI
  - Circuit and architectural level NBTI model
- NBTI mitigation techniques
  - Input vector control
    - Flipping bit cell data in SRAM
  - Power-gating schemes for NBTI