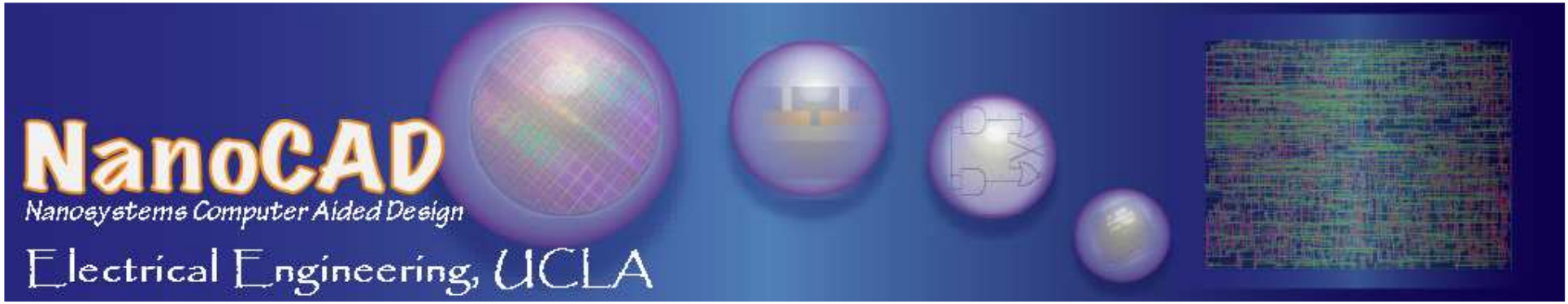


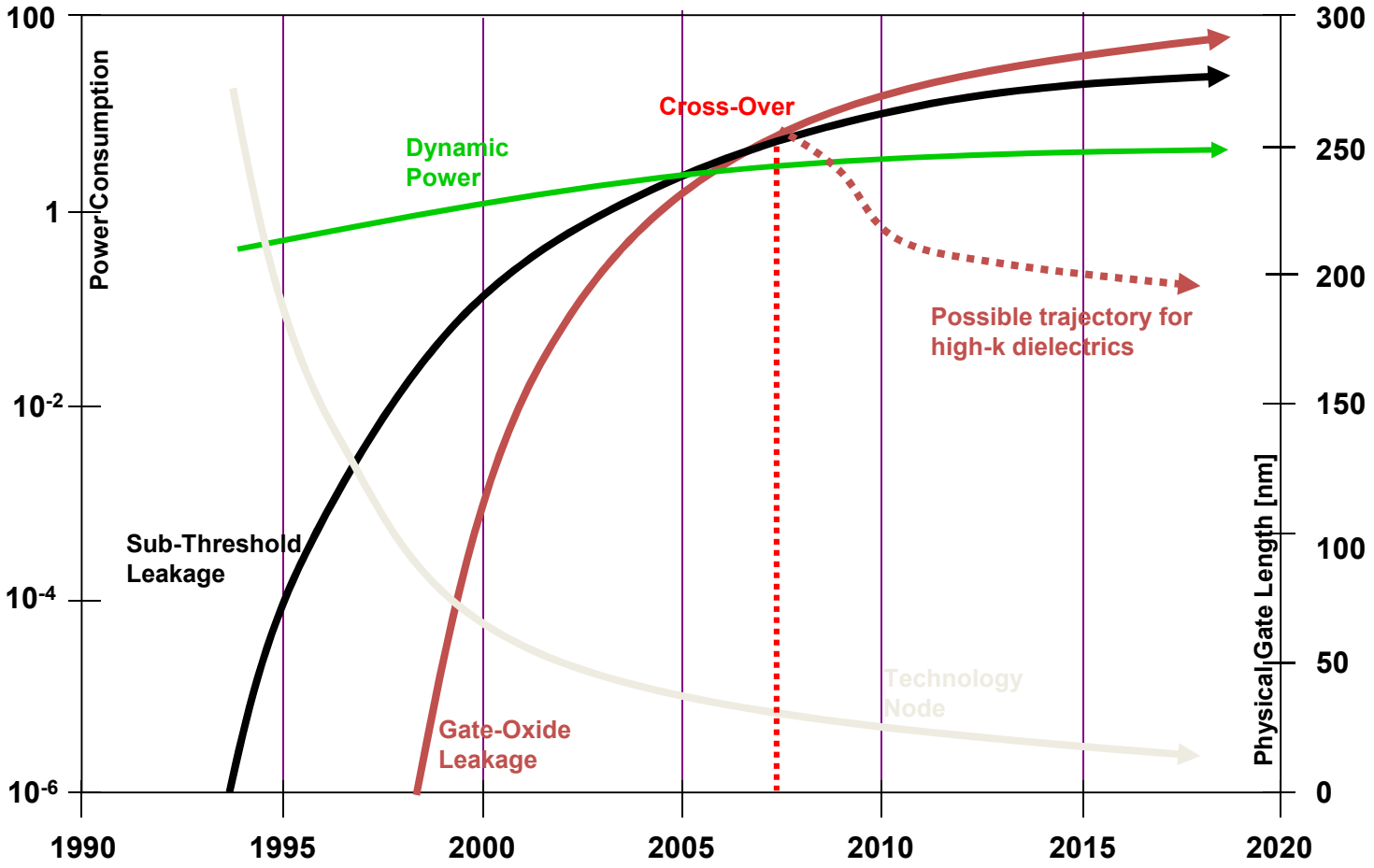
Power Gating Implementation in SoCs

Charwak Apte

http://nanocad.ee.ucla.edu

Dynamic vs. Leakage Power
Componets of IC Power

Source: ITRS Roadmap 2007



Motivation

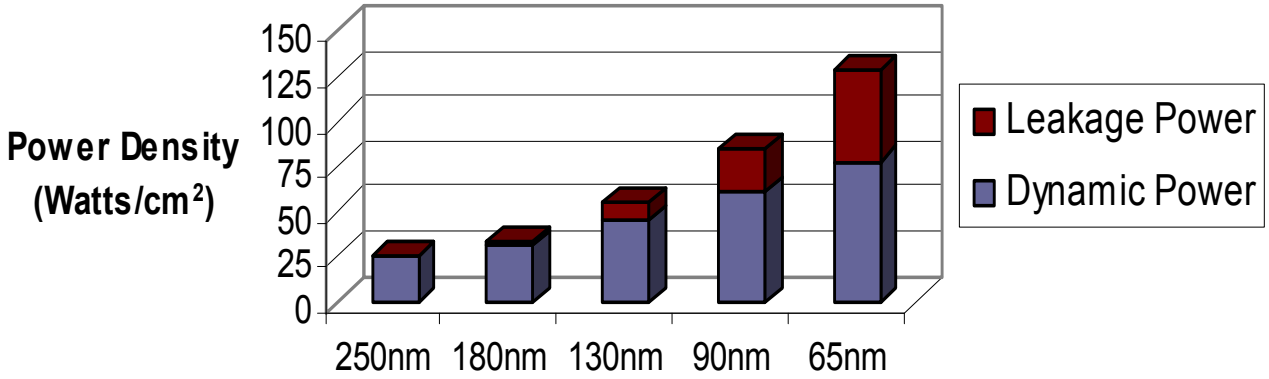
- Battery Life.
- Cost of packaging and cooling.
- Reliability and Performance degradation.
  - Slower, leakier circuits at high temperatures, higher rate of electromigration etc.
- More features being integrated on smaller area.
- **Leakage Power** may soon become the **dominating part** of total power consumption

Low Power Techniques for SoCs

- Parallelism and Pipelining.
- Gate sizing
- Multi Vdd
- Clock Gating
- Power Gating
- DVFS
- Device level techniques (high-k Hf based MOS)

Contribution of leakage power

Example: ASICs [source: STMicroelectronics].



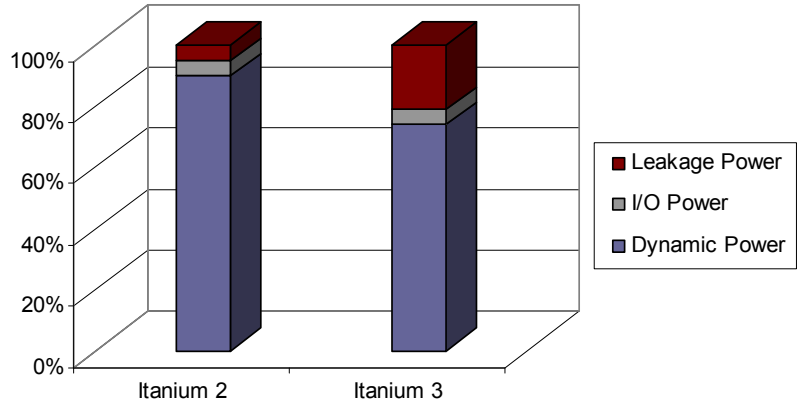
Example: Microprocessors [source: Intel].

Itanium 2:

180nm, 1.5V, 1.0GHz,
221MTx (core+cache)

Itanium 3:

130nm, 1.3V, 1.5GHz,
410MTx (core+cache)

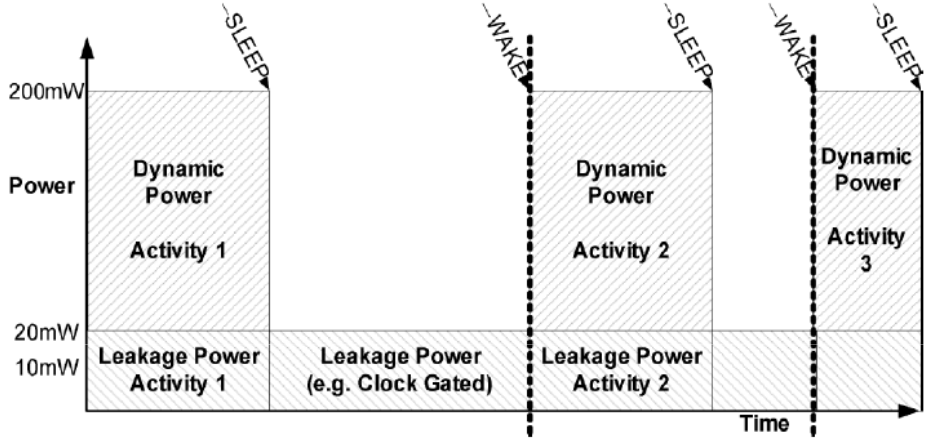


Power gating

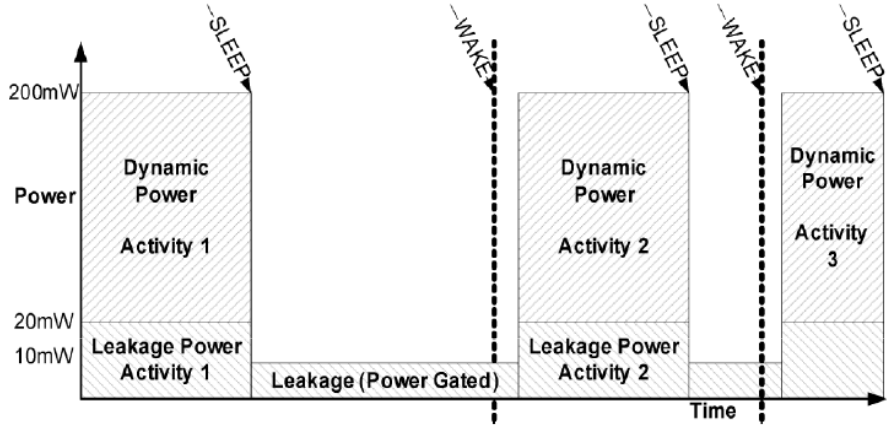
"The basic strategy of power gating is to provide two power modes: a low power mode and an active mode. The goal is to switch between these modes at the appropriate time and in the appropriate manner to maximize power savings while minimizing the impact to performance."

Activity Profile with No Power Gating

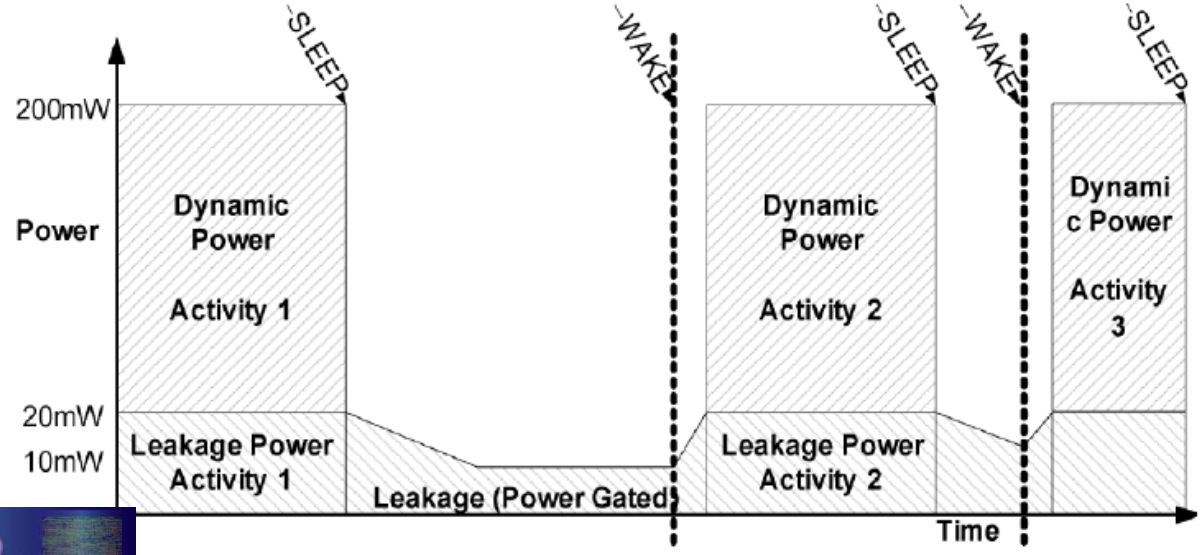
No Power Gating



Power Gating Implemented

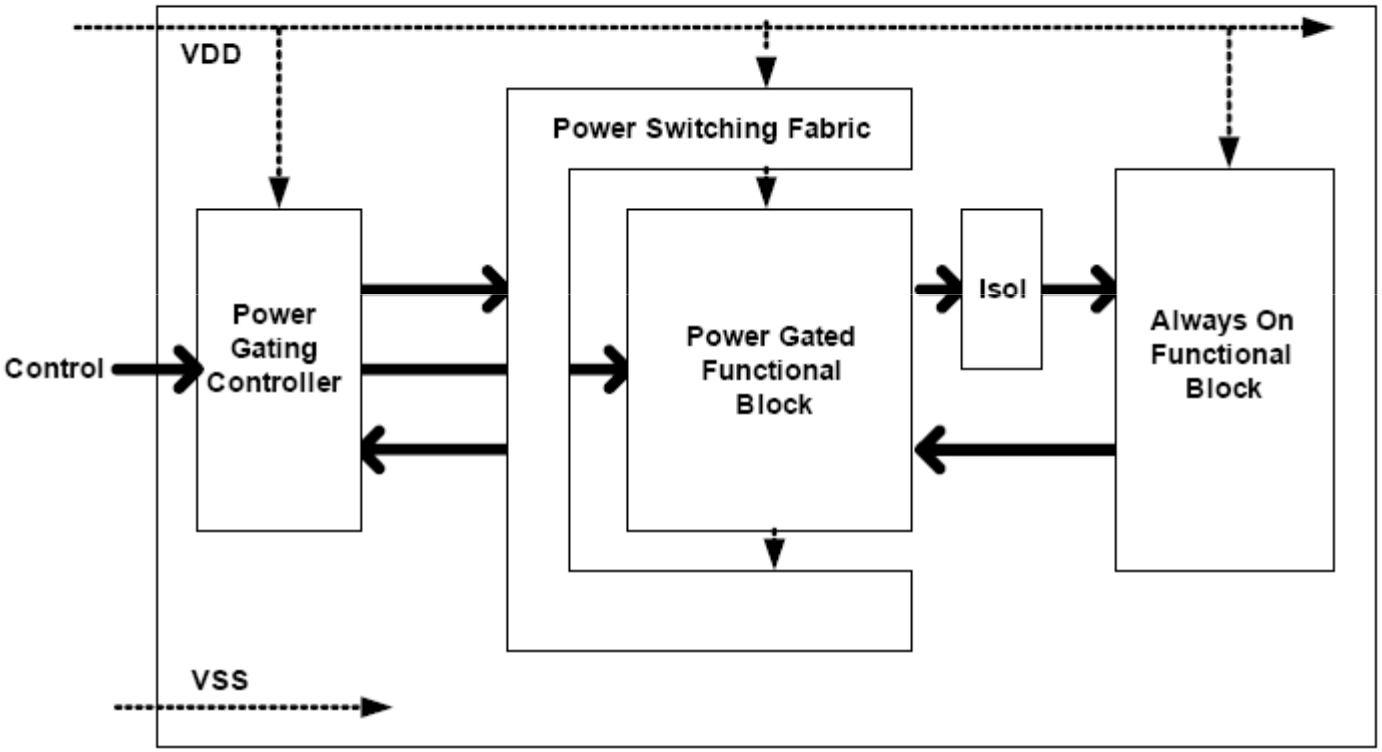


Realistic Power Gating



Ref [2]. LPMM

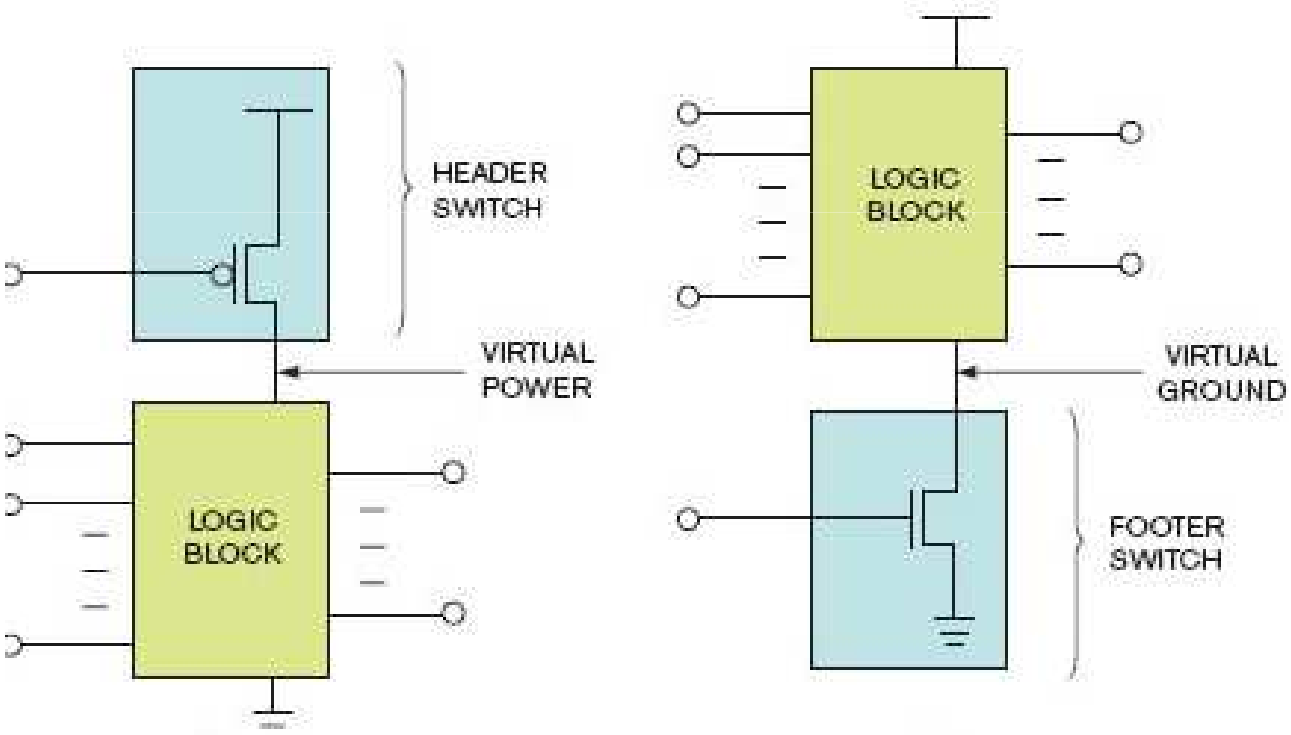
Block Diagram of SoC with power Gating



Ref [2]. LPMM

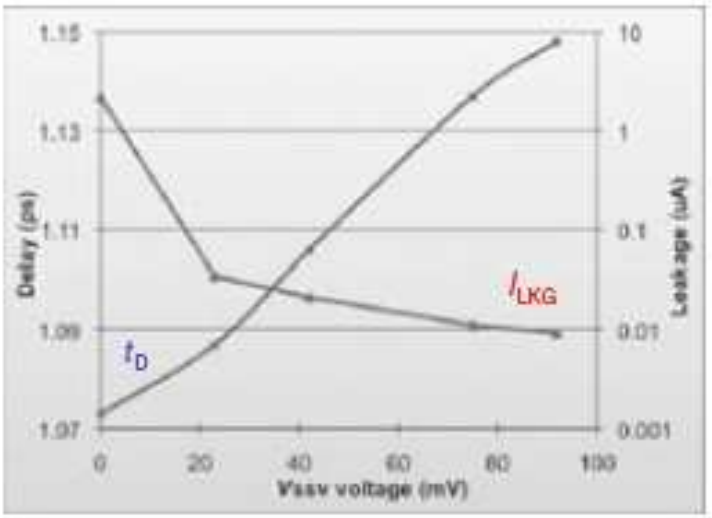
Headers and Footer Switches

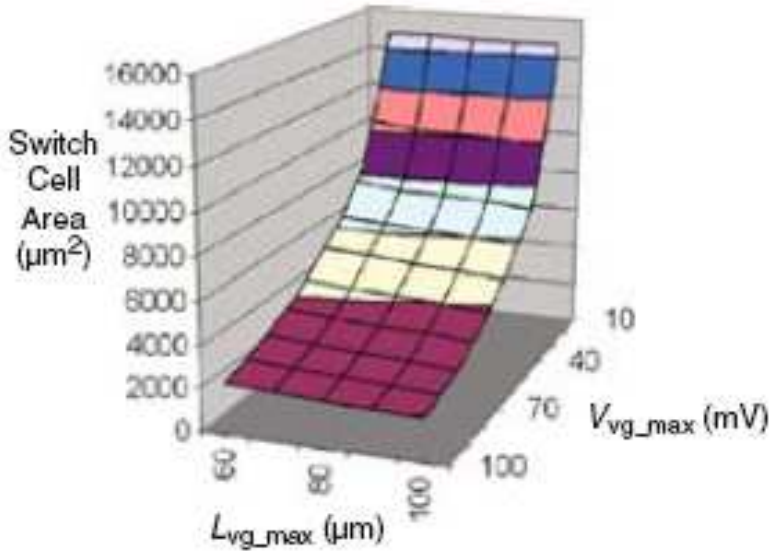
Only Headers or Footers used in design sub 90nm (IR drop)



Switch Sizing Considerations

- Smaller switches ➔ smaller area, larger resistance, good leakage reduction
- Bigger Switches ➔ larger area, smaller resistance, relatively low leakage reduction.

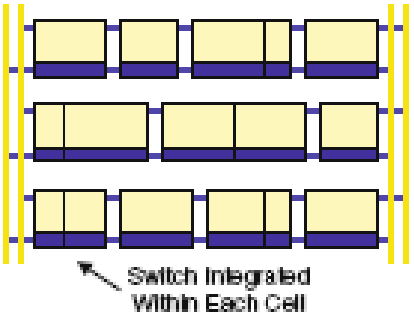




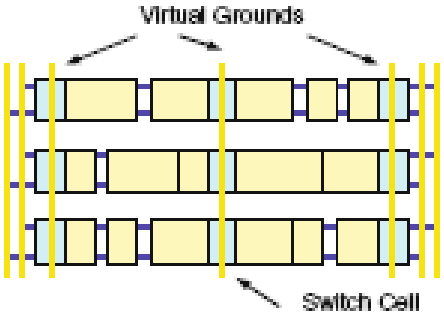
[Ref: J. Frenkil, Springer'07]

Switch Placing Architectures (Physical Design)

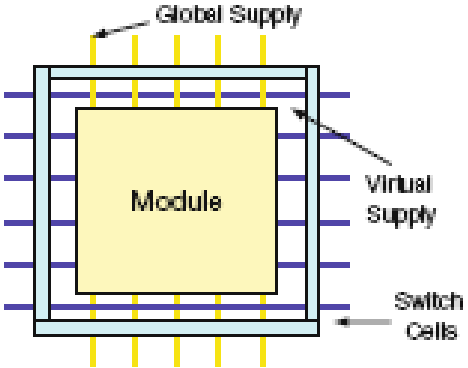
- Switch in Cell: Switch transistor in each standard cell. (Area, Physical Design ease).
- Grid of Switches: Switches placed in an array across the power gated block. 3 rails routed through the logic block. (Power, Gnd, Virtual)



Switch-in-cell



Grid of Switches



Ring of Switches

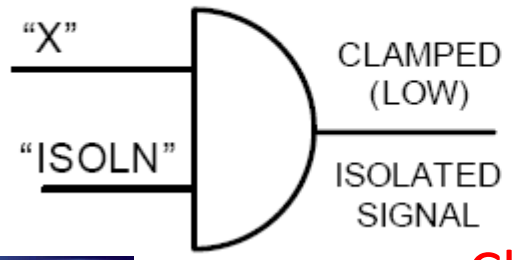
[Ref: S. Kosonocky, ISLPED'01]

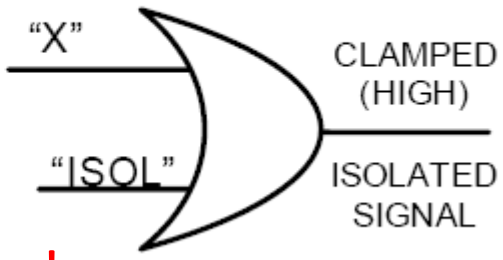
Switch Placing Architectures (Physical Design) .. contd

- Ring of switches: Used primarily for legacy designs where the physical design of the block may not be disturbed.

Signal Isolation

- Powering down the region will not result in crowbar current in any inputs of powered up blocks.
- None of the floating outputs of the power-down block will result in spurious behavior in the power-up blocks.





Clamps add delay!

State Retention

- While Logic Block power Gating, we have to retain some critical register contents (FSM states) .
- Saving and restoring state quickly and efficiently ➔faster and power-efficient method to get the block fully functional after power up.
- DSP Unit – data flow driven – can start from reset on new data input.
- A cached processor – large residual state

State Retention Techniques

- Software based register read writes.

Slow and increases active-sleep-active latency.

Bus conflicts cause non-deterministic save/restore times

- A scan-based approach based on using scan chains to store state off chip.

No area overhead as existing scan chains may be used,

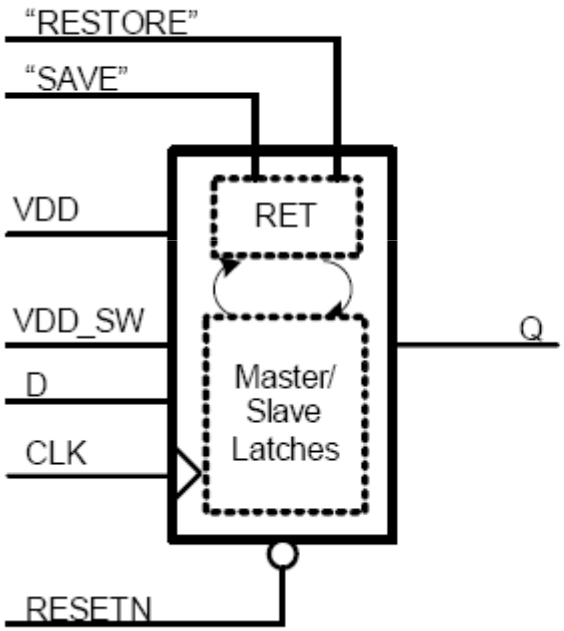
During power down, scan registers are routed to memory.

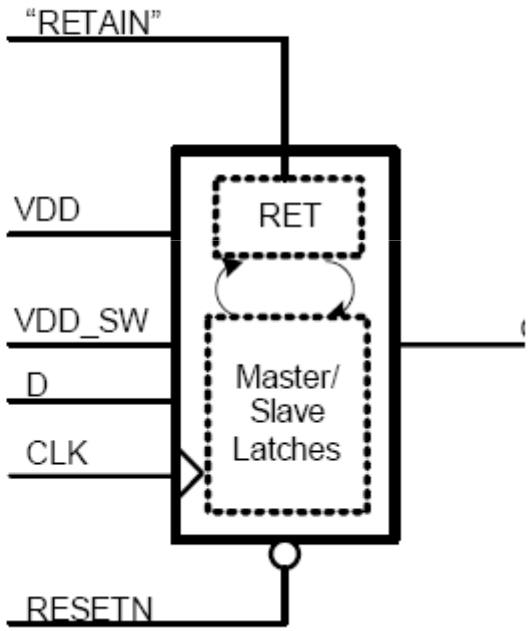
During power up scan chains are loaded from memory.

- Retention registers

Area overhead, typically 20% or more.

Retention Registers





Power gating Design Verification

- Verilog and other HDLs do not provide for specifying power connections at RTL.
- UPF (unified power format) specifies simulation semantics and language format for PG .
- Key Simulator Requirements:
  - Functional modeling of power gating, isolation and retention.

Design for Test Implications

- External controls and observability of power gating signals.
- PDN testing for correct behavior.
- Testing PG controller, retention and isolation behavior

Power Gating Considerations

- Library design: special cells are needed

  Switches, isolation cells, state retention flip-flops (SRFFs)
- Headers or Footers?

  Headers better for gate leakage reduction, but ~ 2X larger
- Which modules, and how many, to be power gated?

  Sleep control signal must be available, or must be created
- State retention: which registers must retain state?

  Large area overhead for using SRFFs
- Floating signal prevention

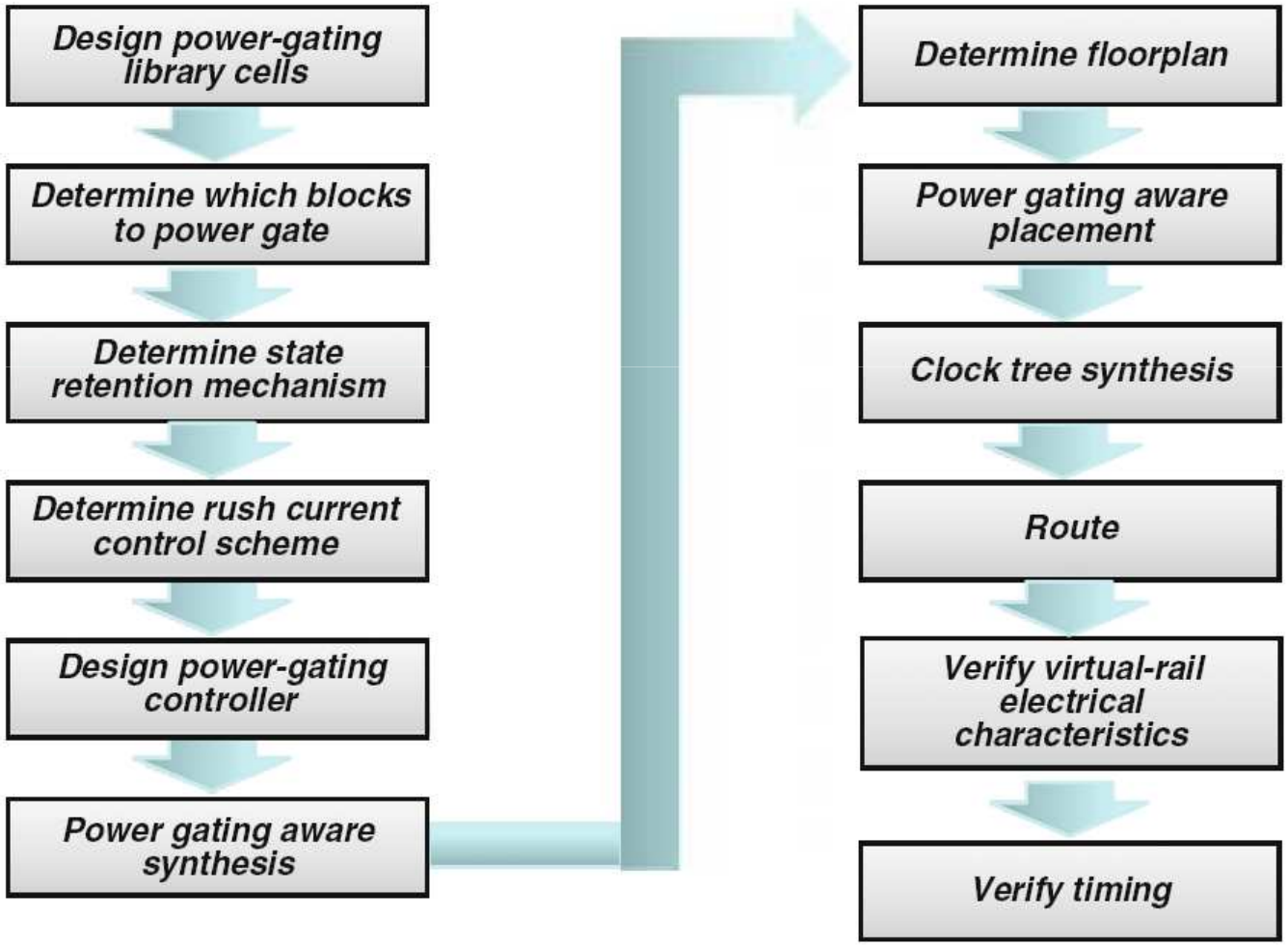
  Power-gate outputs that drive always-on blocks must not float
- Rush currents and wake-up time

  Rush currents must settle quickly and not disrupt circuit operation
- Delay effects and timing verification

  Switches affect source voltages which affect delays
- Power-up & power-down sequencing

  Controller must be designed and sequencing verified

Power Gating Flow



Full Power Gating Results

Parameter	Design		
	A	D	E
Process technology	90nm	130nm	90nm
Supply voltage	1.5V	1.5V	1.2V
Logic function	32-bit ALU	8-bit datapath	multi-processor
Retain state in registers?	yes	yes	no
# of instances	1,852	118	182,225
# of power-gated logic instances	1,388	80	181,809
# of switch instances	104	3	15,872
# of interface instances	206	10	0
Logic cell to switch cell ratio	13.3	26.7	11.5
Power-gated logic cell area (um^2)	15,259	886	1,457,391
Switch cell area (um^2)	2,565	114	136,545
Switch area overhead (%)	16.8%	12.9%	9.4%
Interface cell area (um^2)	791	38	0
Interface cell area overhead (%)	5.2%	4.3%	0.0%
Original bounding-box area (um^2)	977,725	3,483	22,156,698
New bounding-box area (um^2)	977,725	3,483	22,156,698
Bounding-box area increase (%)	0.0%	0.0%	0.0%

Ref: Chinnery, Keutzer et al. [1]

Selective Power Gating Results

Parameter	Design			
	A	B	C	E
Process technology	90nm	90nm	90nm	90nm
Supply voltage	1.5V	1.5V	1.5V	1.2V
Logic function	32 bit ALU	32 bit DSP	32 bit DSP	multi-processor
Retain state in registers?	yes	yes	yes	yes
# of instances	1,808	148,879	226,259	182,225
# of power-gated logic instances	359	14,418	55,479	19,639
# of switch instances	55	1,005	2,057	4,060
# of interface instances	206	9,213	29,140	12,259
Logic cell to switch cell ratio	6.5	14.3	27.0	4.8
Power-gated logic cell area (um^2)	6,136	248,173	218,846	143,563
Switch cell area (um^2)	1,192	46,954	23,303	17,923
Switch area overhead (%)	19.4%	18.9%	10.6%	12.5%
Interface cell area (um^2)	791	35,378	54,820	43,249
Interface cell area overhead (%)	12.9%	14.3%	25.0%	30.1%
Original bounding-box area (um^2)	977,725	5,651,221	34,552,882	22,156,698
New bounding-box area (um^2)	977,725	5,651,221	34,552,882	22,156,698
Bounding-box area increase (%)	0.0%	0.0%	0.0%	0.0%

Ref: Chinnery, Keutzer et al. [1]

References

[1]Closing the Gap between ASIC and custom designs. Chinnery, Keutzer et al.

[2]Low Power Methodology Manual.

[3] Low Power Design Methodologies and Flow. – Frenkil and Rabaey