Spintronics - Magnetoresistive RAM

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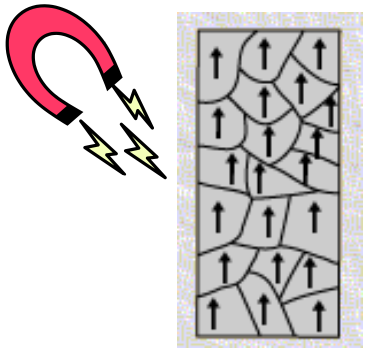
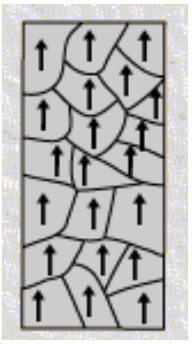
Introduction

- Spintronics
  - Manipulate spin of a particle (in contrast to charge)
  - Each electron spins along an axis
- Ferromagnetic material (FM)
  - Metal which “keeps” magnetic direction

Normal FM



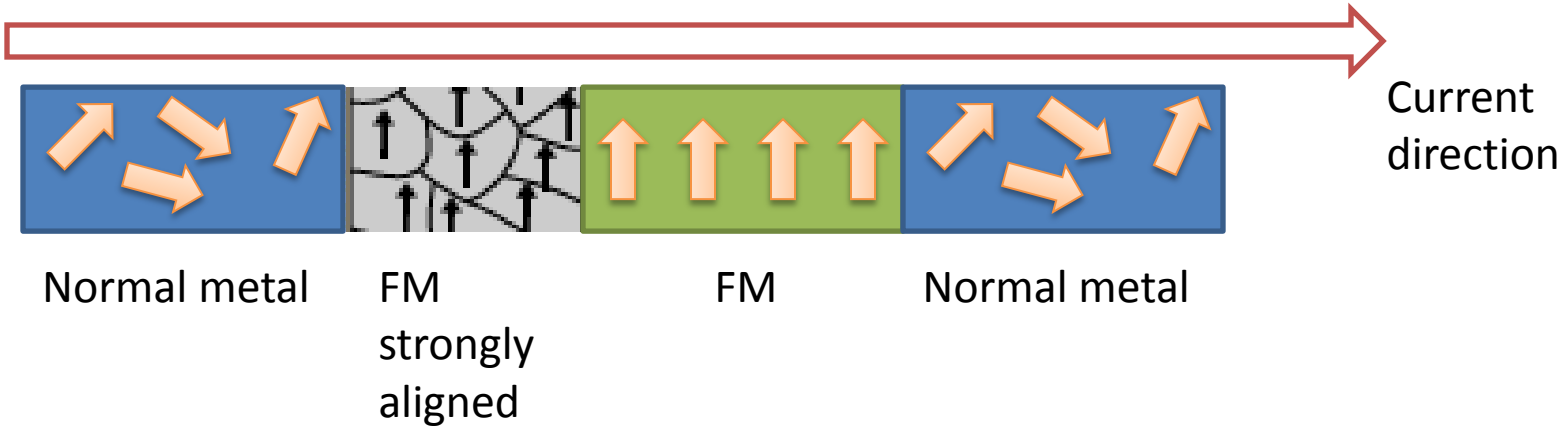
Under magnetic field



After removing magnetic field

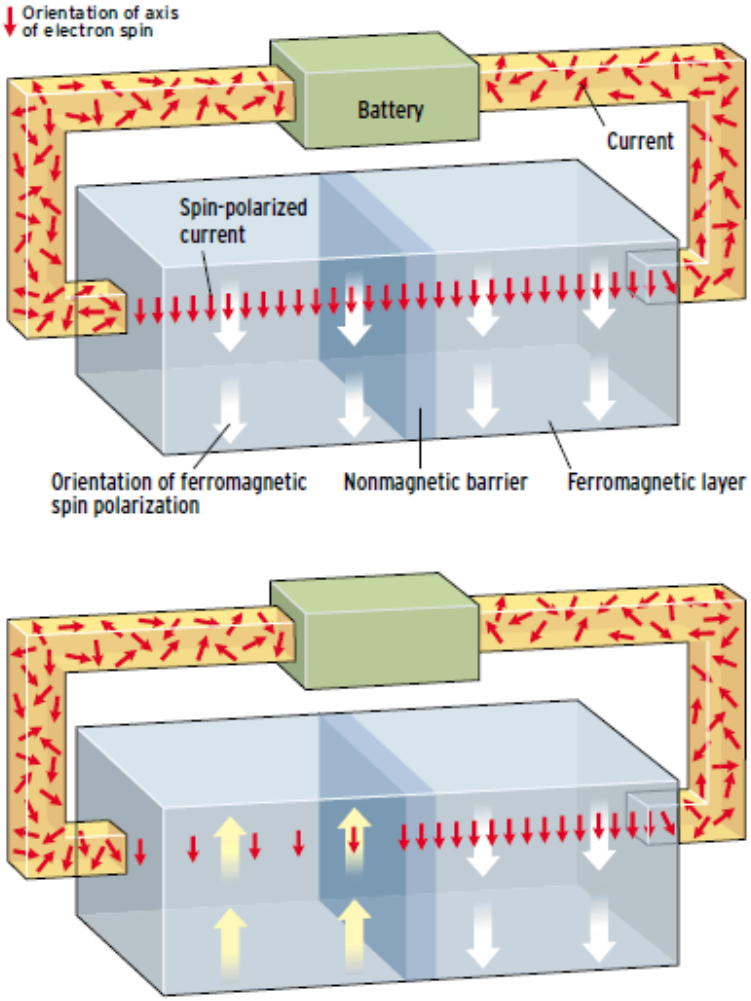
Ferromagnetic material (FM)

- Polarize electron spin (source)
  - Current/electron flows through FM will be aligned



- Store spin direction (memory)
  - Use FM to record information

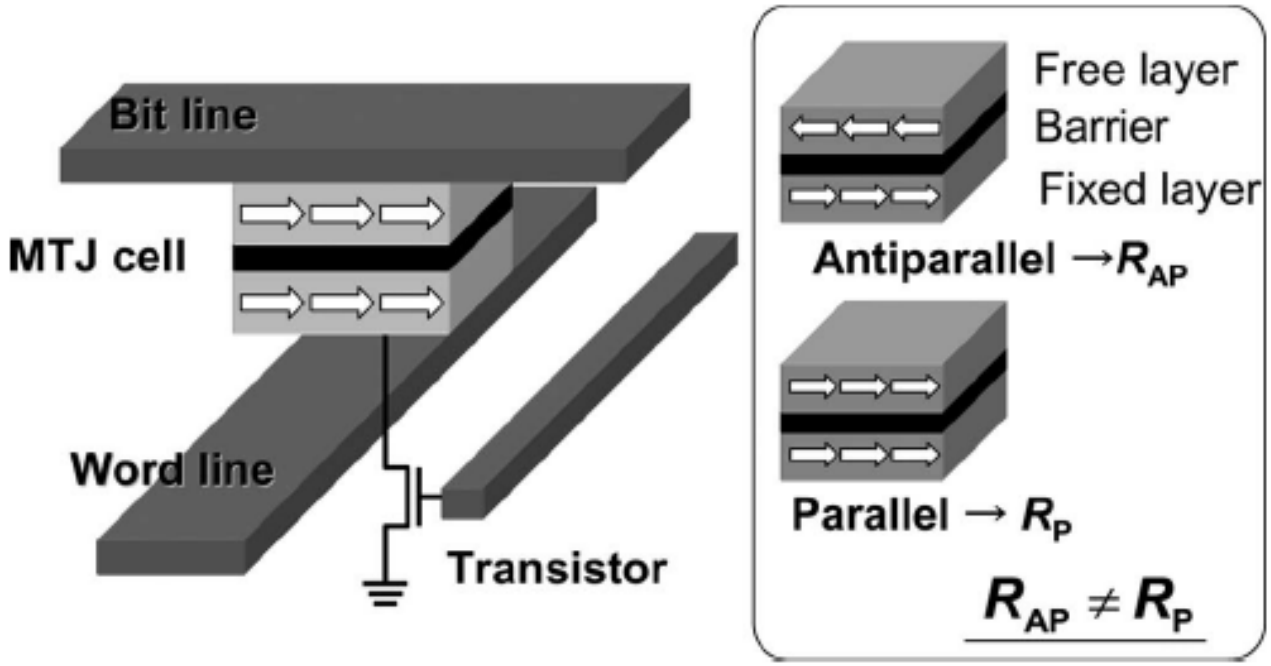
Magnetic Tunneling Junction (MTJ)



- First discovered in 1970s
- 2 layers of FM separated by a thin layer of non-magnetic barrier
- Directions of FM
  - Parallel : low resistance
  - Anti-parallel : Hi resistance

IEEE spectrum Sept. 2001

MTJ-based Memory Structure



- Spin direction of free layer indicates ‘0’ of ‘1’

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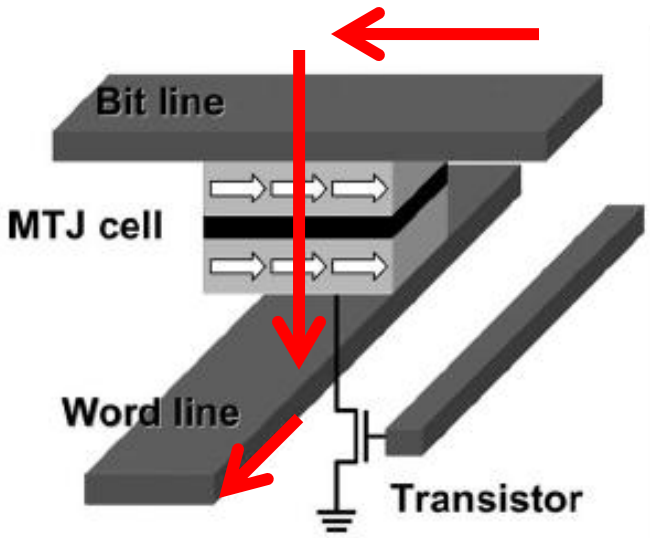
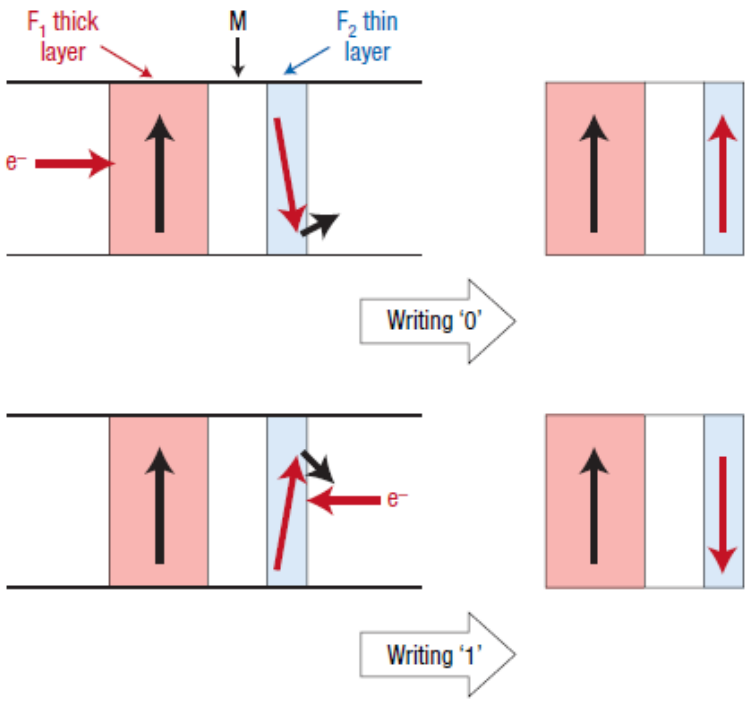
Writing ‘spin’

- Field writing:
  - Apply current flowing through bit line and word line
  - Generates magnetic field and changes direction of free layer

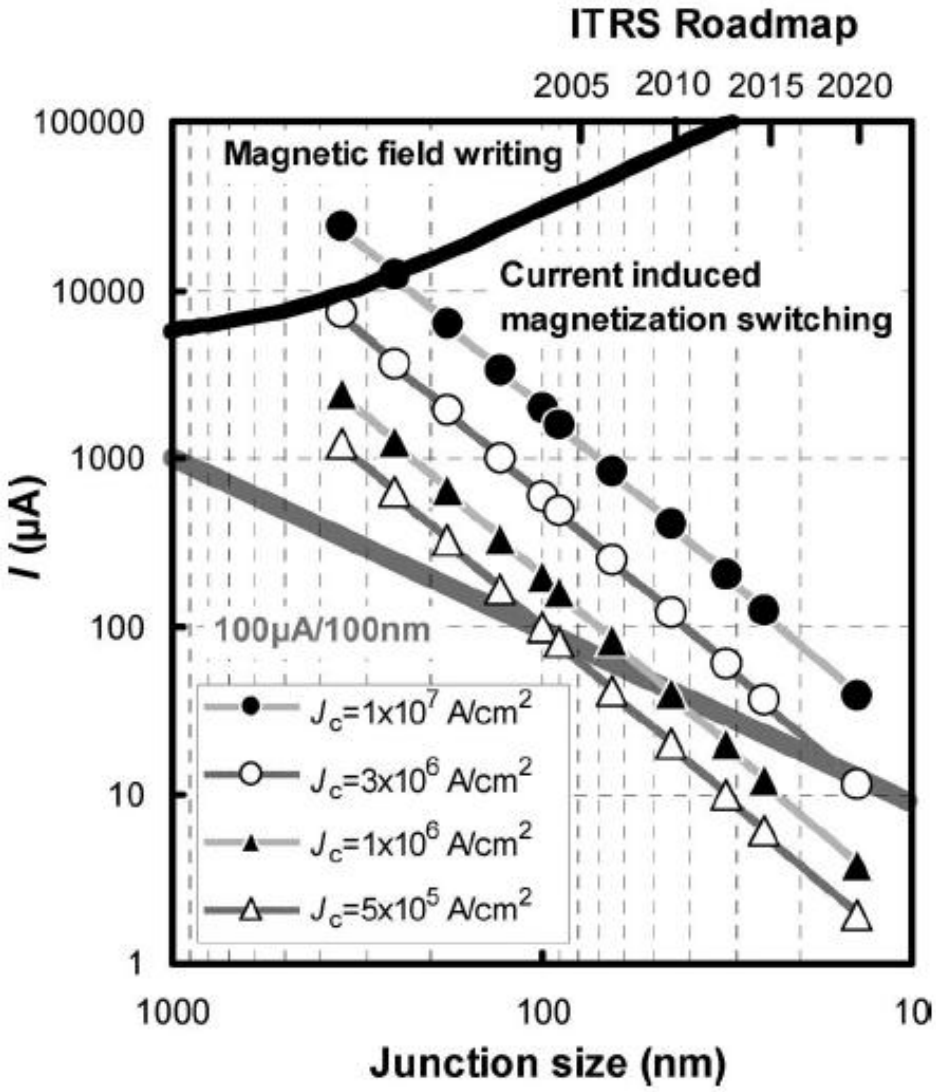


- Spin polarized current can exert torque on magnetization
  - Torque per unit area is proportional to injected current



Trend

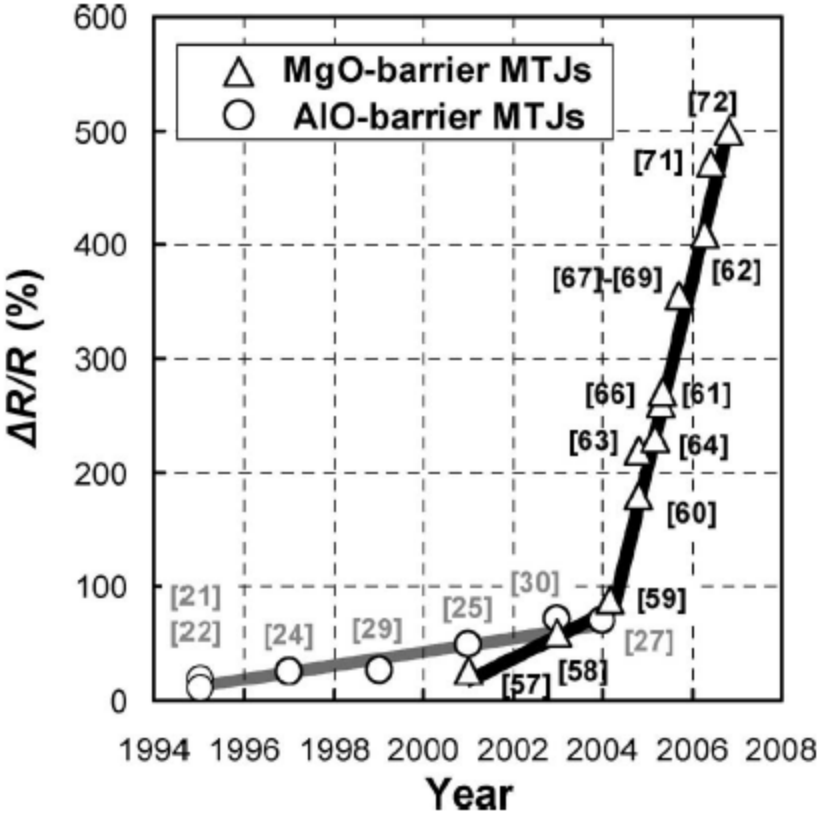
- Field writing is inversely proportional to junction size
- Current induced writing is scalable

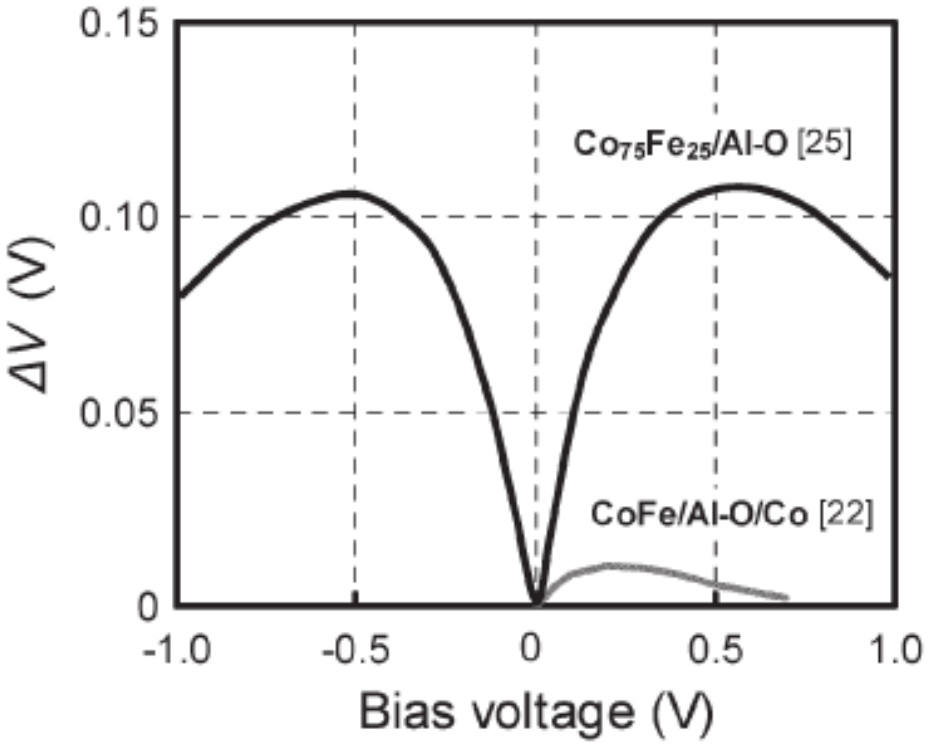


Quality metrics

- Tunnel Magneto-Resistance (TMR)

$$\Delta R/R = (R_{\mathrm{AP}} - R_P)/R_P$$





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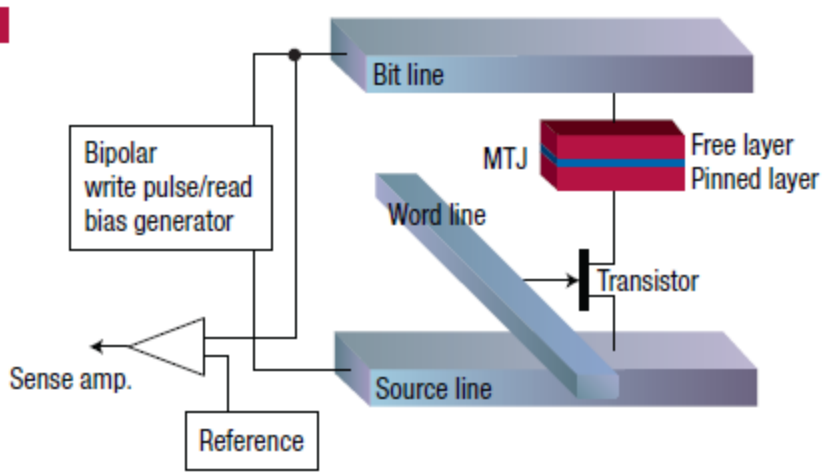
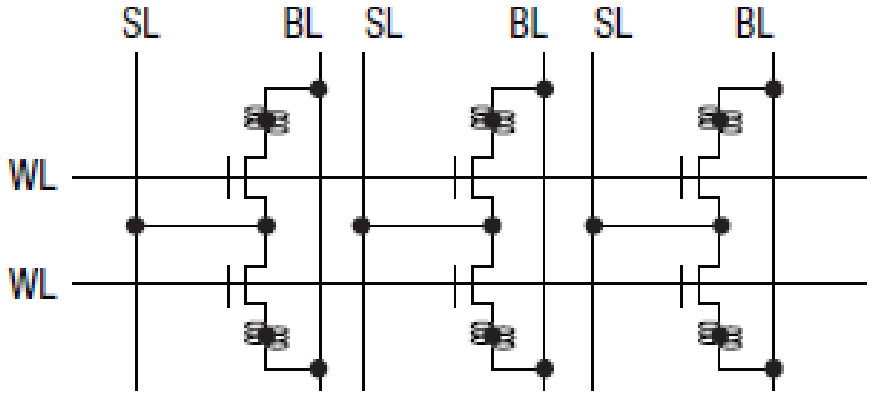
Spin Ram

- Comparable speed
- No static power
- Need to have high magneto resistance ratio



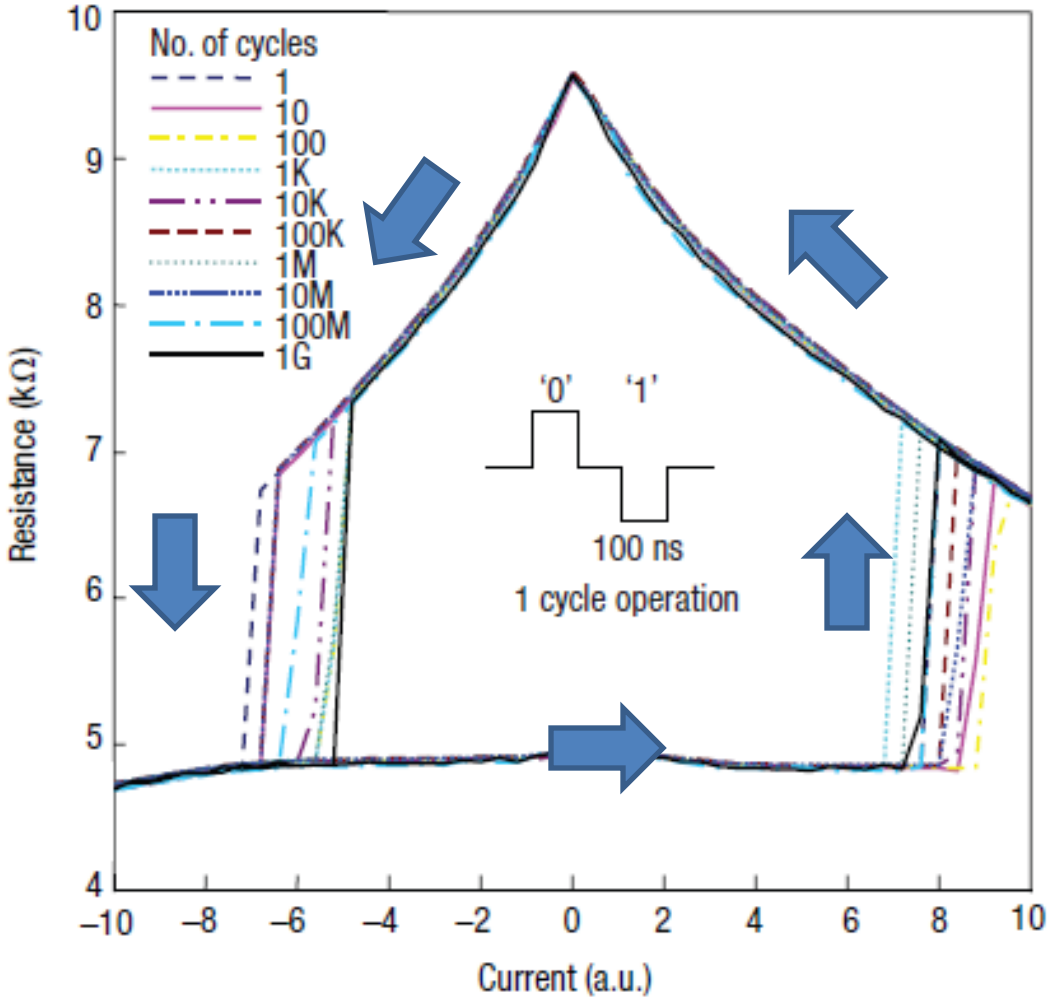
		CMOS	TMR-based
Delay (ns)		0.69	0.61
Power (μW)	Dynamic	275	193
	Static	16.2	0
# of transistors		5	1

(MR ratio: 1000%)



More on current writing

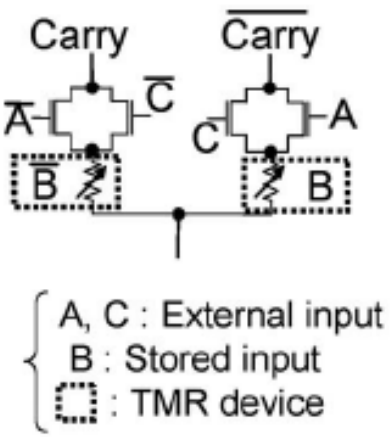
- Stable over many cycles
- Dominant factor: pulse width => speed

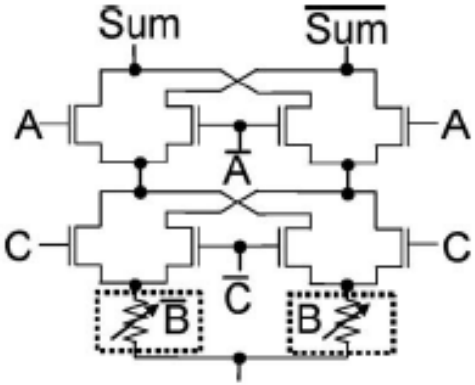


Logic gate?

- TMR/CMOS style
  - Need CMOS because the gain of TMR is not sufficient to drive the next stage

Min Resistance=60 Max resistance=90k

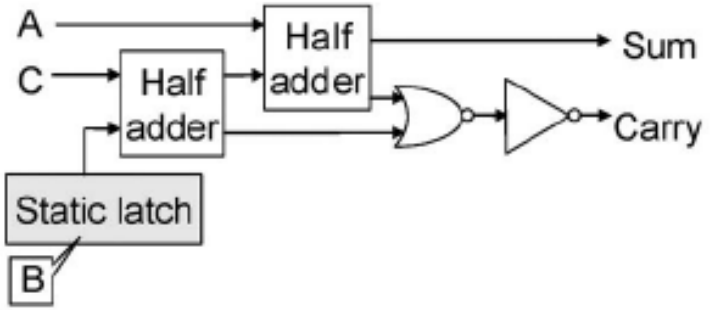




	CMOS	TMR-based
Delay	310ps	310ps
Device counts	40Tr.	24Tr.+2C
Dynamic power	51μW	16μW
Static power	55nW	0.084nW

(0.18μm TMR/CMOS, V_{DD}=1.8V)

CMOS only



Advantages

- Low power
- Compact (if control circuit is minimized)
- Fast and non-volatile

Challenge/variations

- Temperature fluctuation causes electron scattering and resistance variation
- Uniformity of barrier
- Magnetic intensity difference

References

- “The Quest for the Spin Transistor” IEEE spectrum Sept. 2001.
- “The emergence of spin electronics in data storage” Nature, vol. 6, Nov. 2007.
- “Magnetic Tunnel Junctions for Spintronic Memories and Beyond” IEEE Trans. On Electron Devices, vol. 54, no. 5, May 2007.
- “Dynamic current mode logic (DyCML): A new low-power high-performance logic style,” *IEEE JSSCC, vol. 36, no. 3, Mar. 2001.*