UCLA

Highlights on EUV from SPIE advance lithography 2010

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Outline

- Updates on Extreme Ultraviolet Lithography
  - Optical tool, Resists, throughput
  - Defects
- EUV vs Double patterning

Optical Tool Road Map

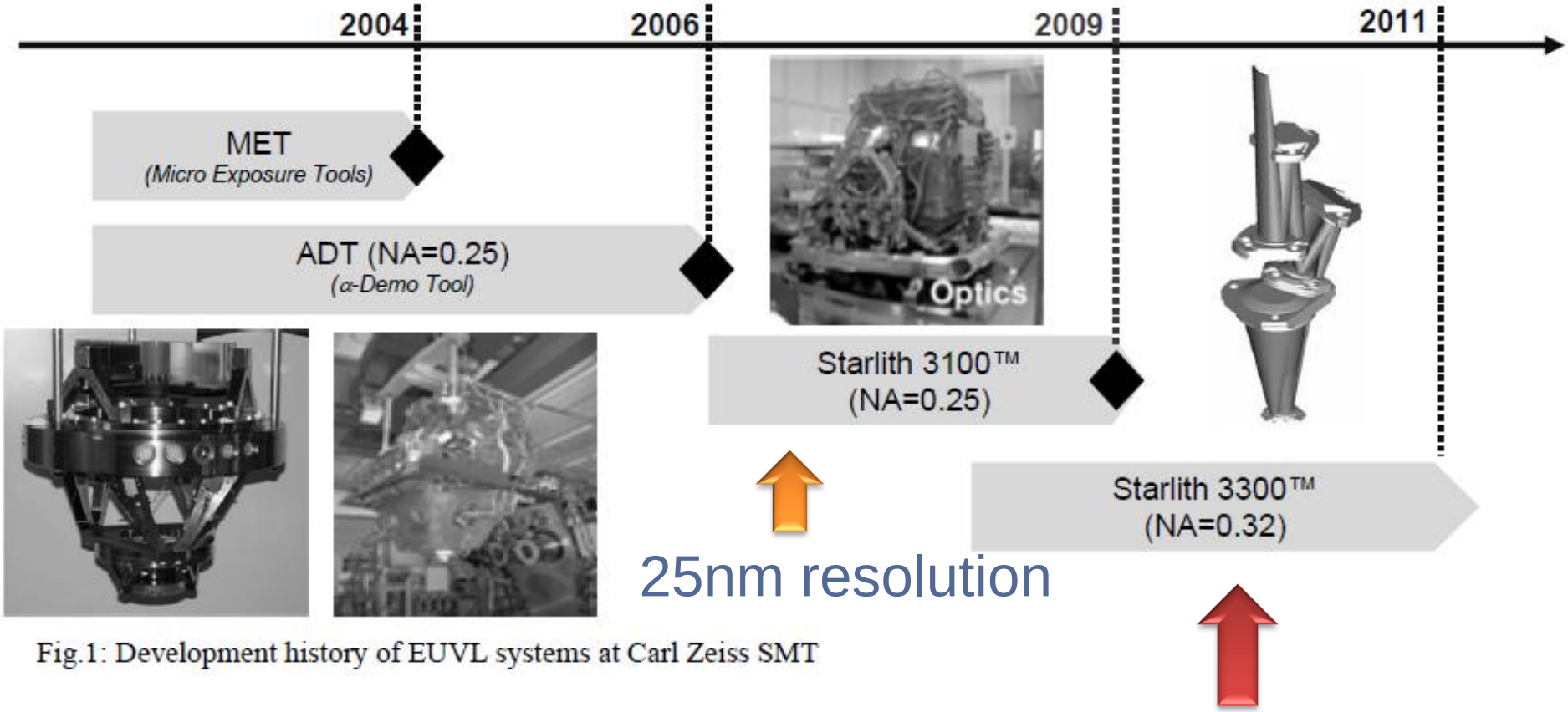
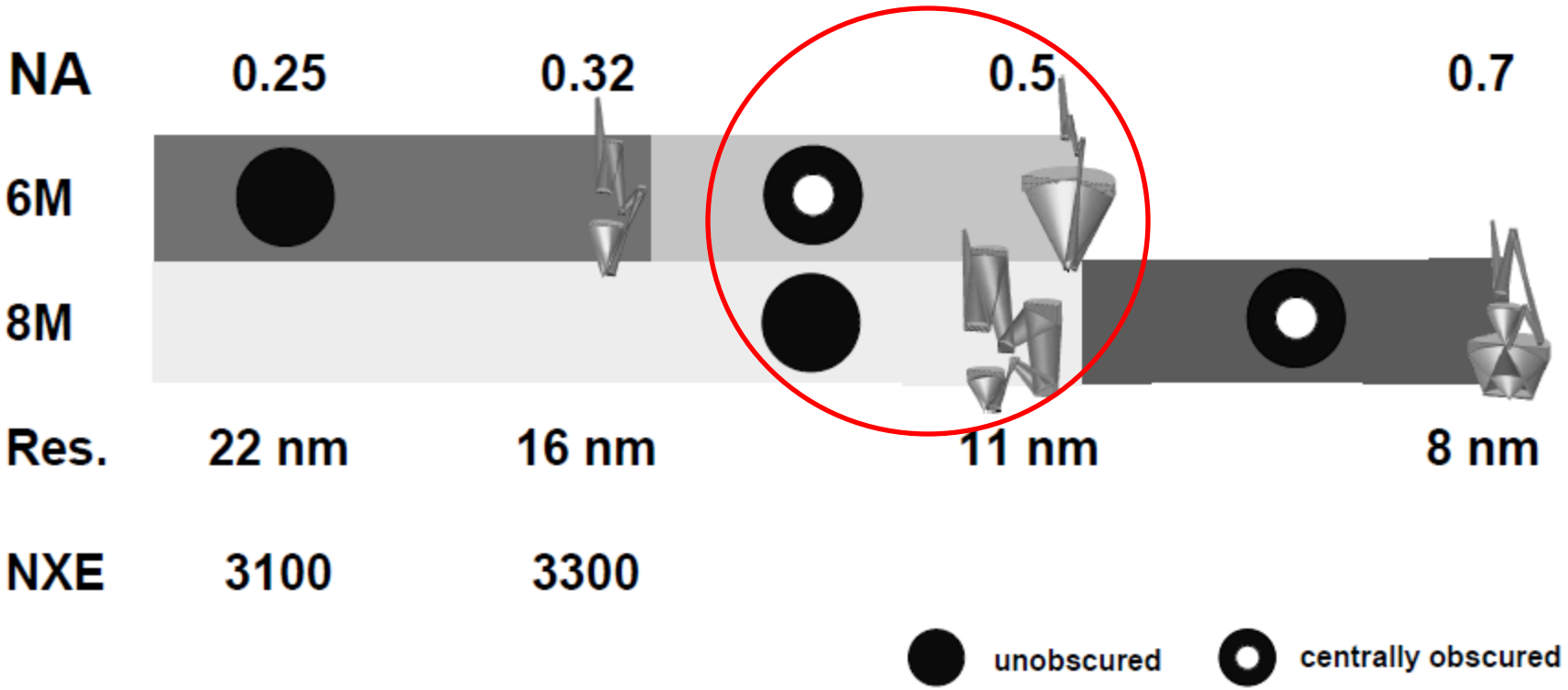


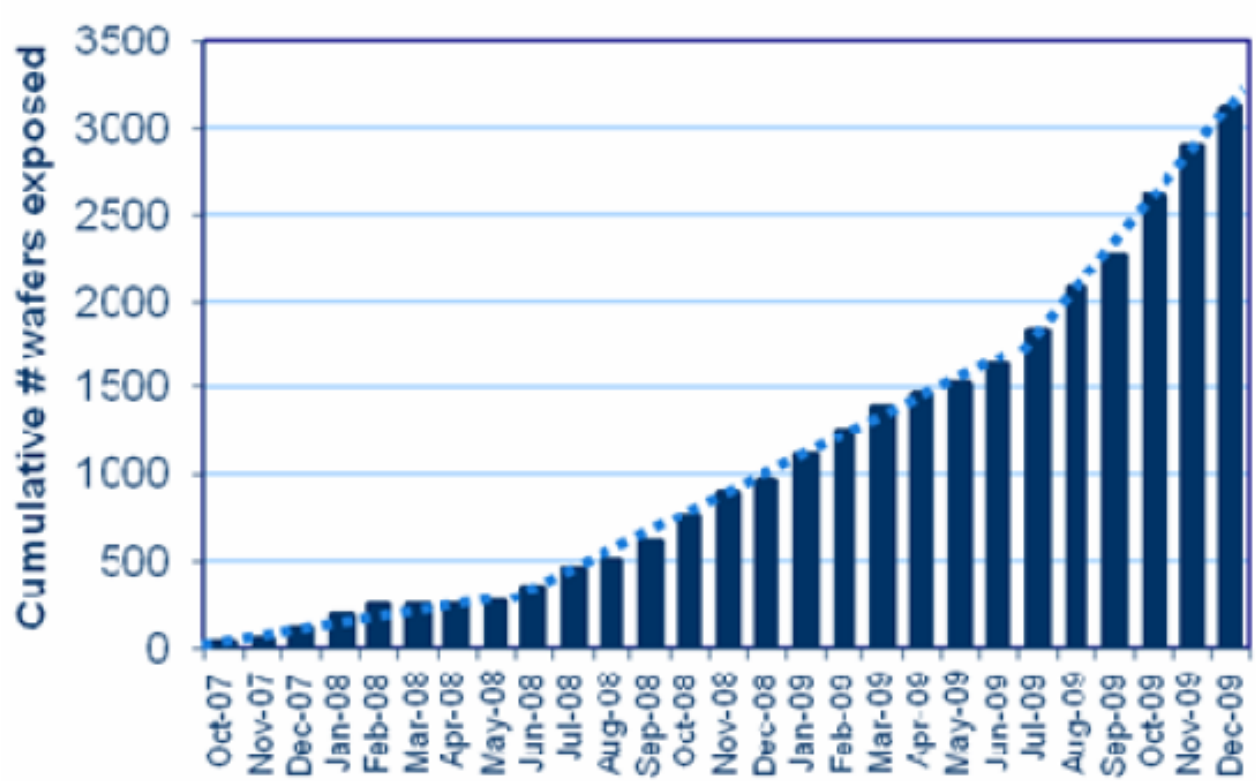
Fig.1: Development history of EUVL systems at Carl Zeiss SMT

Solution Overview



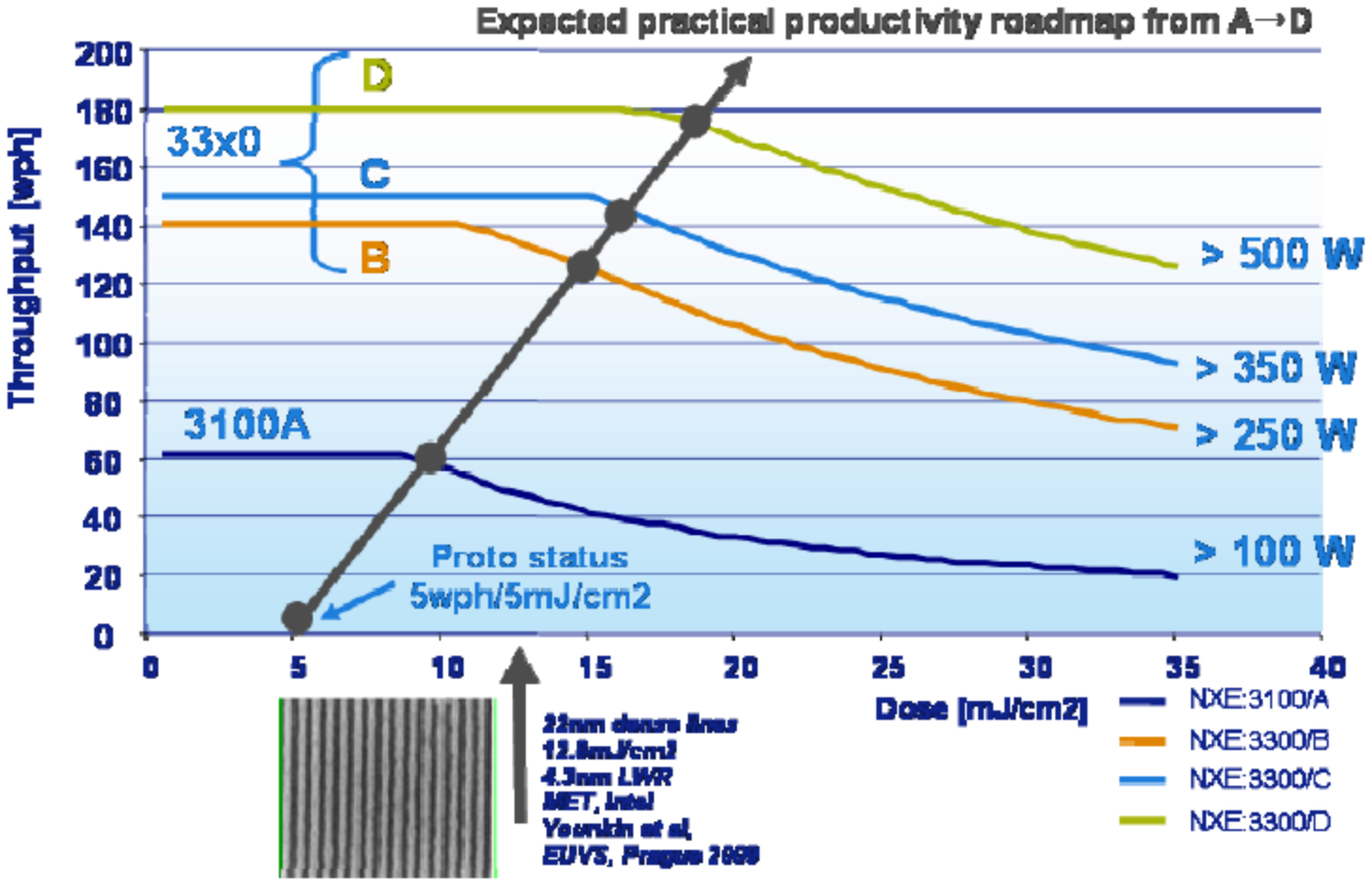
- Resolution ≈ K (λ/NA)
- Reflection efficiency reduced from 6 mirrors to 8 mirrors
  - Higher source power

Current status



- About 350 wafer per month

Throughput



ASML "EUV into production with ASML's NXE platform

EUV source

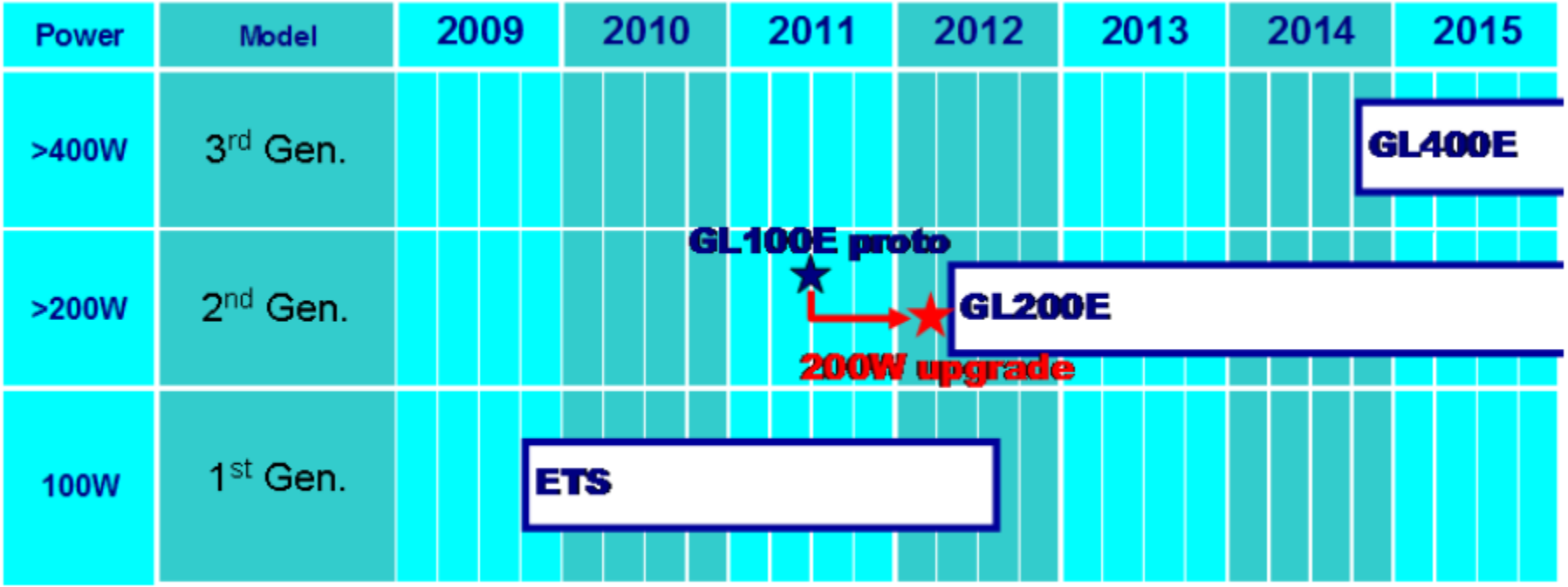


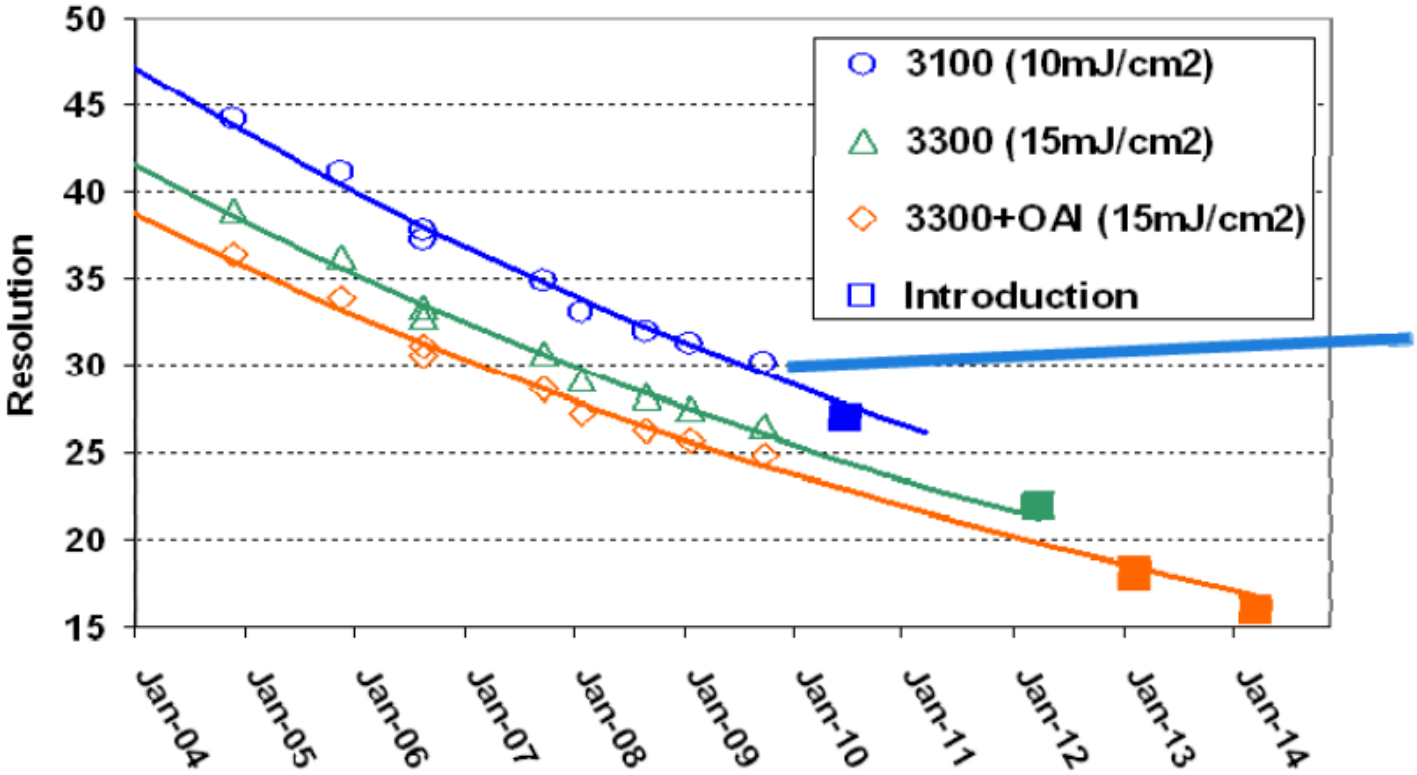
Figure 14 Road map of Gigaphoton LPP EUV source

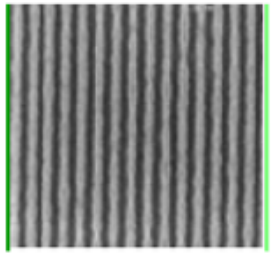
- EUV targets ~3x of an ArF scanner source power (Cymer)

Resist for EUV

	Key Item	Target for 28 nm HP	Resist A (Polymer-bound PAG)	Resist B (PHS Hybrid)	Resist C (Molecular Glass)
1-1	Resolution	28 nm	25	26	27
1-2	Resist Collapse (Useful DOF at 28 nm HP)	160 nm	40	80	0
1-3	%EL @ 28 nm HP	10%	18	13	7
1-4	DOF @ 28 nm HP	160 nm	120	120	80
2	LWR (nm)	2.8 nm	3.8	4.8	5.4
3	Sensitivity (mJ/cm^2)	$15mJ/cm^2$	23.2	22.8	24.2
4	Relative Etch Resistance	A/R 2.2	70	100	68
5	MEEF	<1.4	1.29	1.33	2.11
6	ID Bias (nm)	<2.8 nm	2.4	5.9	29.2
7	CD Linearity (Average % Deviation)	<5%	1.4	3.7	9.2
8	PEB Sensitivity (nm/°C)	<1 nm/°C	1.6	0.53	0.53
9	PED Stability (nm/1hr)	<1 nm/Hr	0.6	-0.4	0.7
10	Line Slimming (After 12 sec. inspection charging)	-	4.1	2.7	4.2

Resolution

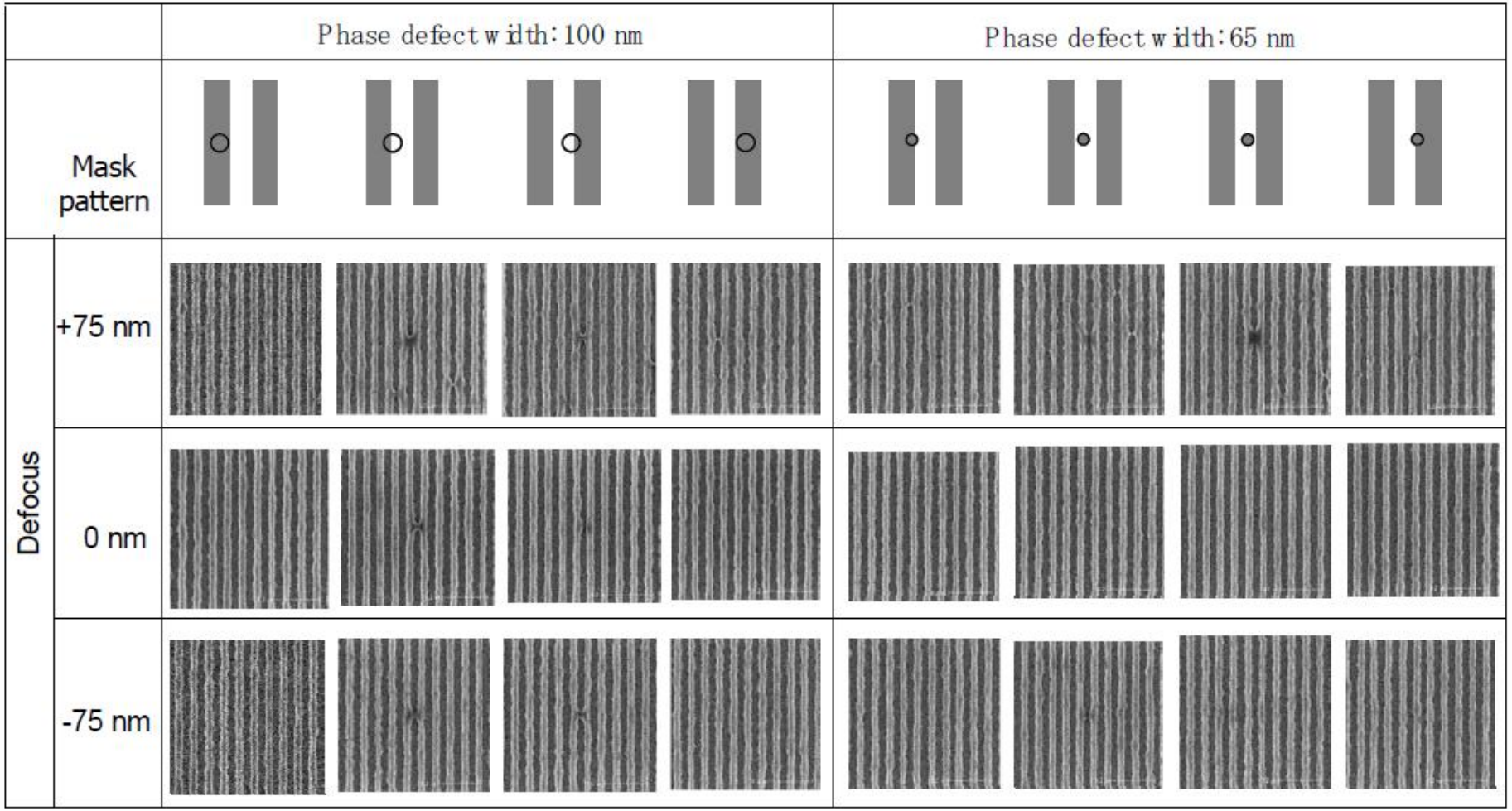




22nm dense lines
12.8mJ/cm2
4.3nm LWR
MET, Intel
Younkin et al,
EUVS, Prague 2009

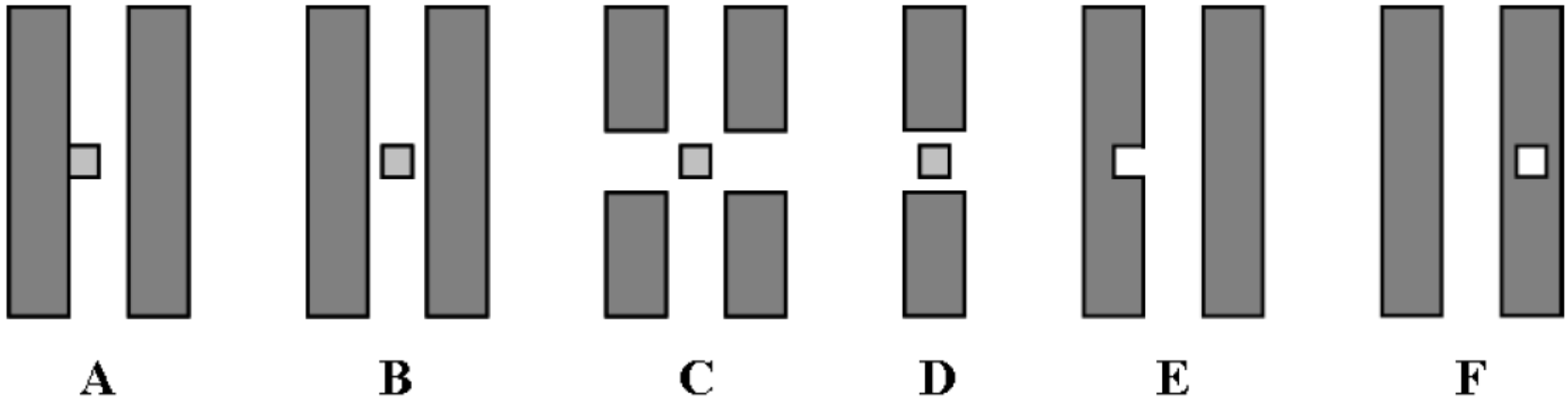
ASML "EUV into production with ASML's NXE platform

Defects



Need to consider defect size, pattern, defocus **together**

EUV Defect Printability (ΔCD>10%)

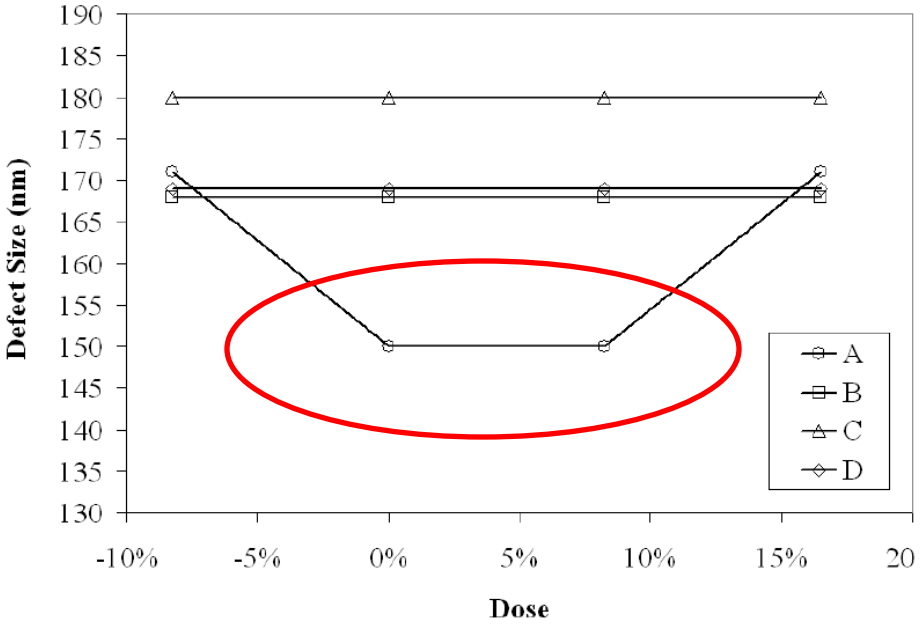


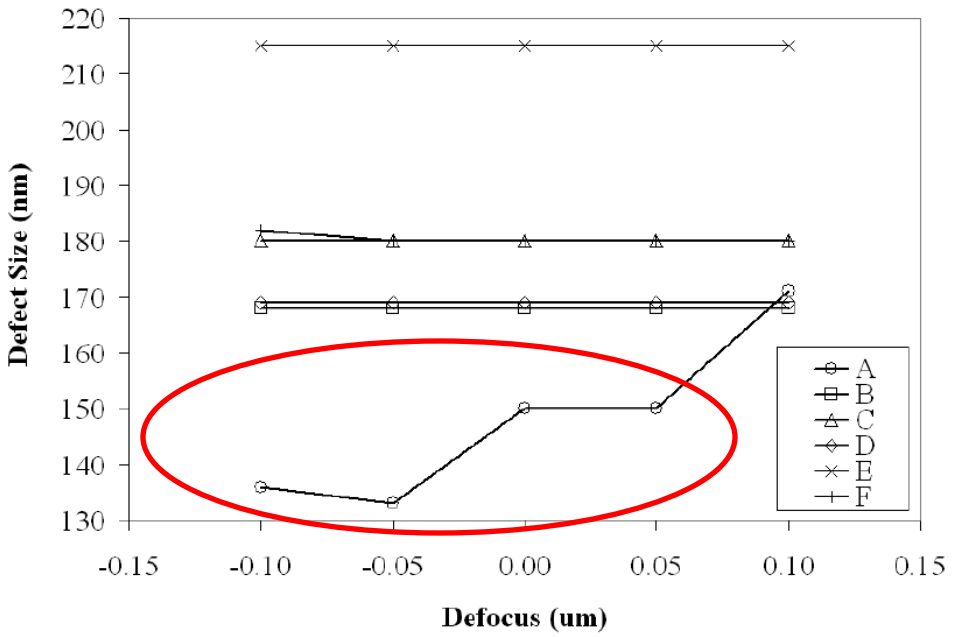
- Minimum Programmed Defect Size Observed on the EUVL Mask

Defect Type	110 nm Half-Pitch	150 nm Half-Pitch	200 nm Half-Pitch
A	30 nm	40 nm	40 nm
B	50 nm	70 nm	80 nm
C	80 nm	80 nm	90 nm
D	70 nm	70 nm	70 nm
E	40 nm	40 nm	40 nm
F	70 nm	80 nm	80 nm

GM Kloster (Intel) "**Printability of extreme ultraviolet lithography mask pattern defects for 22-40 nm half-pitch features**"

Effect of Dose & Exposure





- Pattern A (protusion) has minimum printable defect size
  - Sensitive to dose and focus
- Defect aware layout / design rule

Judges Chris Progler and Donis Flagello

EUV

Double patterning

Cymer, Toshiba, Intel & Globa Foundaries

IBM, Nikon, IMEC & Synopsis

It's all about k1 (resolution)!

- Significant degradation in DPL at 40-nm HP
- Carl Zeiss had optical designs below 22 nm
- ASML : Single-exposure EUV has lowest cost of all options (excluding tool?)
- Toshiba roadmap :
  - 2x-nm HP node process study begin this year
  - Primary challenge
    - defectively < 0.1/cm2
    - throughput 100 wph

Intel:

- Needs to ramp up manufacturing at the 22-nm node by 2015.
- logic layouts might need 4+ masks @ 22nm.
- Intel made a zero-defect EUV reticle recently.

Global Foundaries :

- EUV can backfill to earlier technologies, while DPL cannot.

Strong demand from chip makers for EUV

Double Patterning

- Synopsis: multiple design rule and patterning options to extend into 22 nm and below
- IBM : overlay improvements will enable 193 nm DPL extension to 22 nm and beyond
- DPL **is** available **today**

Challenges:

- CD variation is critical , need error budget for other processes
- Increasing mask complexity and cost

Summary

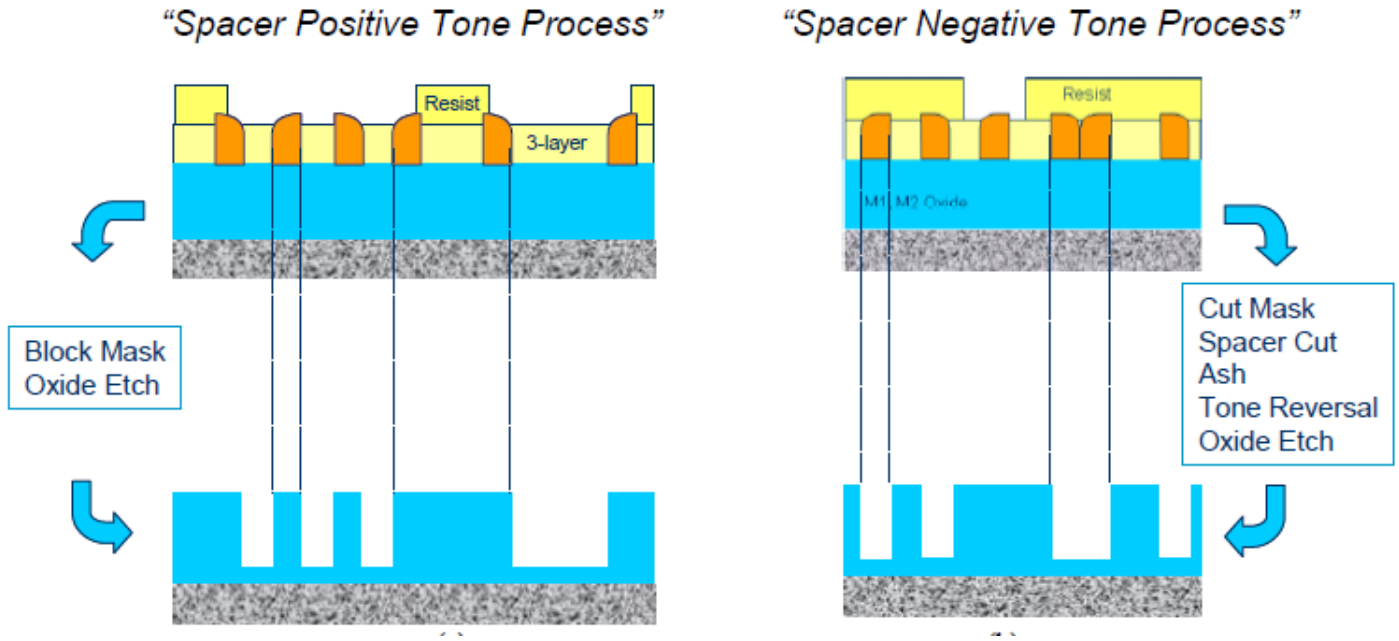
- EUV tools improved, Yet
  - Has not fulfill sources, resists and masks requirements
- Targeted for the 16-nm node or …

- DPL is the promising technology available now
  - Commercial tool available to solve coloring conflict
  - Overlay improved

- Alternative next generation lithography
  - E-beam
  - Nano-imprint
  - Self assembly

Decomposition strategy for self-aligned DP

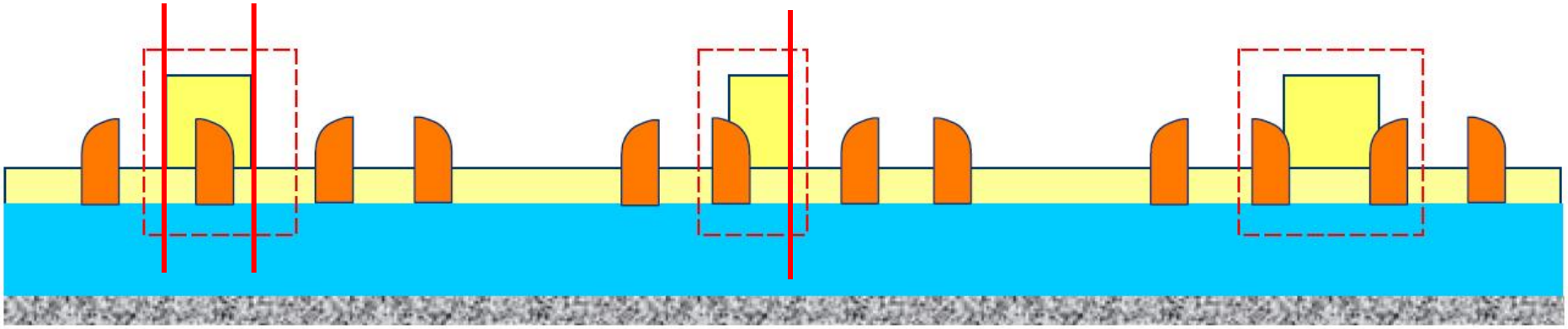
- Advantage of SADP : less overlay
- Lack of decomposition flexibility
- Need to decompose layout with minimum masks (2)

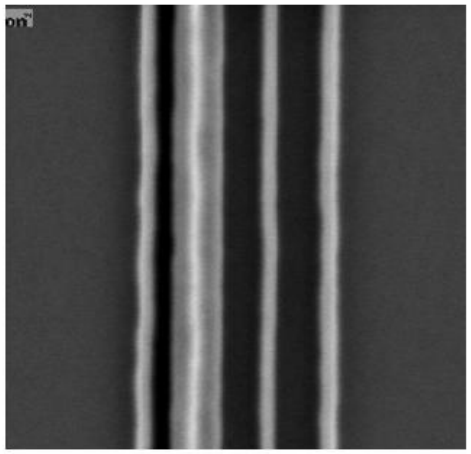


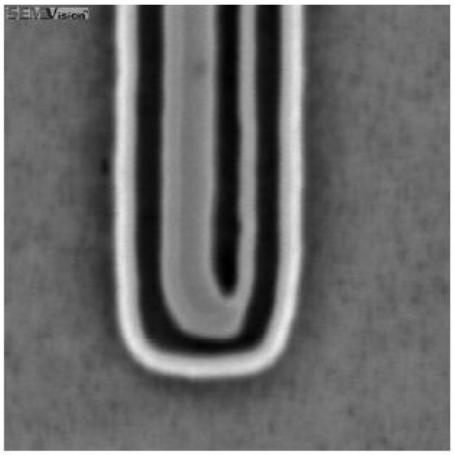
Y. Ma "**Decomposition Strategies for Self-Aligned Double Patterning**"

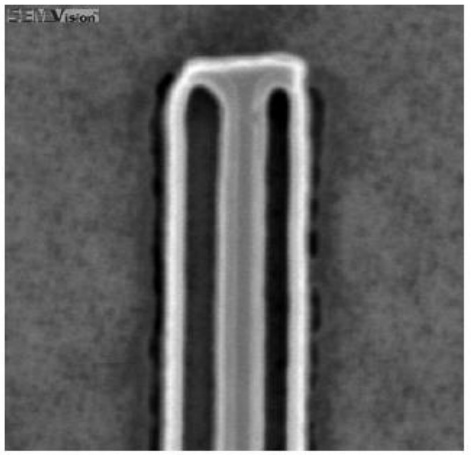
Patterning wide lines

Overlay of second mask :

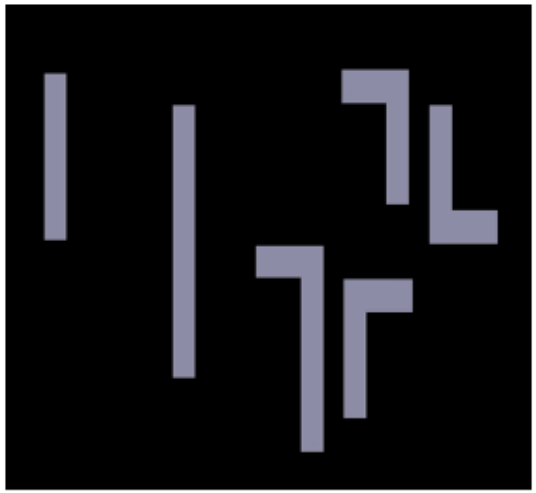




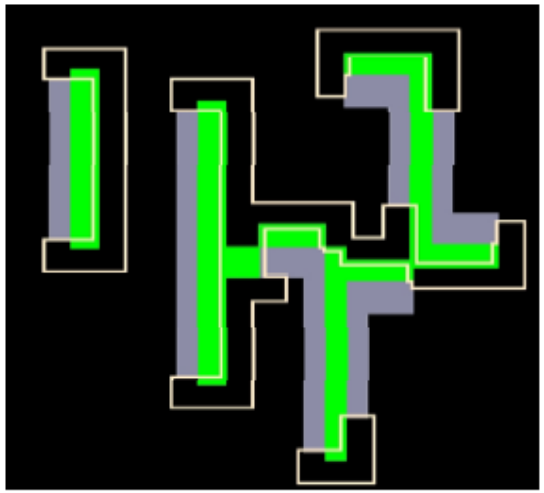




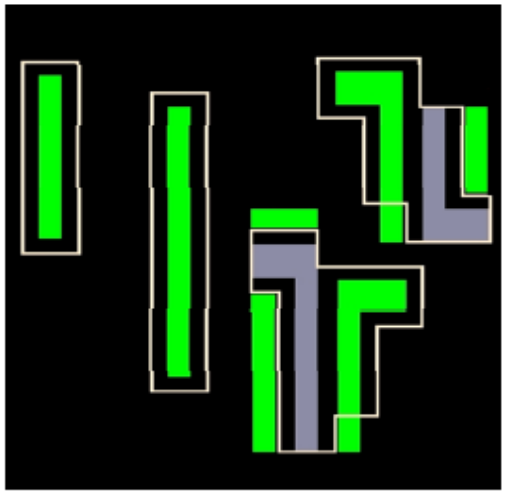
Decomposition example



a. Drawn Target



b. Positive Tone Decomposition



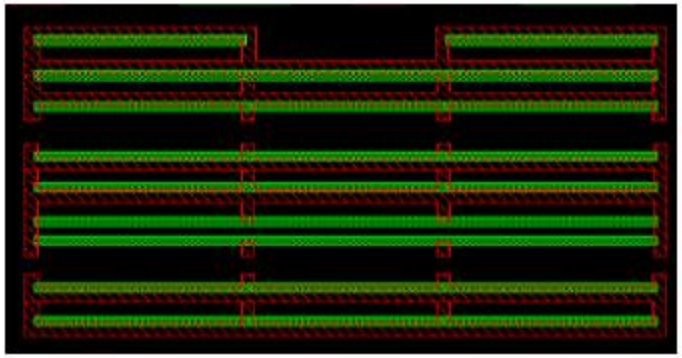
c. Negative Tone Decomposition

target

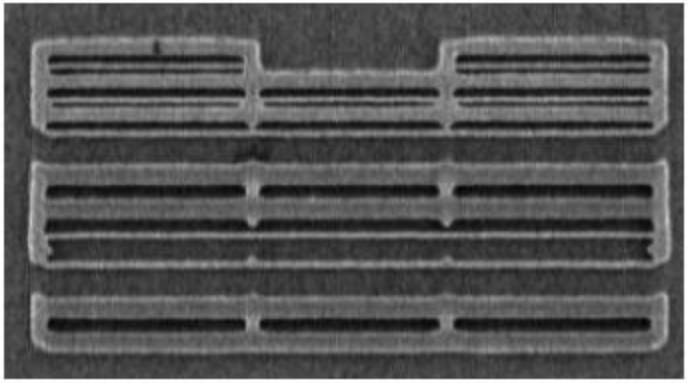
mandrel

Trim Mask

Decomposed Layout



On-Wafer Result



How and Where To Use?

- Mask, scanner, OPC etc limits
  - Over constraint : need to relax to allow certain structures
- Tight Process constraints
  - Restrict layout patterns

- Basic rules for SADP friendly?
- Early adoption of decomposition tool ?
  - Quick iteration of change and check for layout designer