UCLA

E-Beam Direct Write

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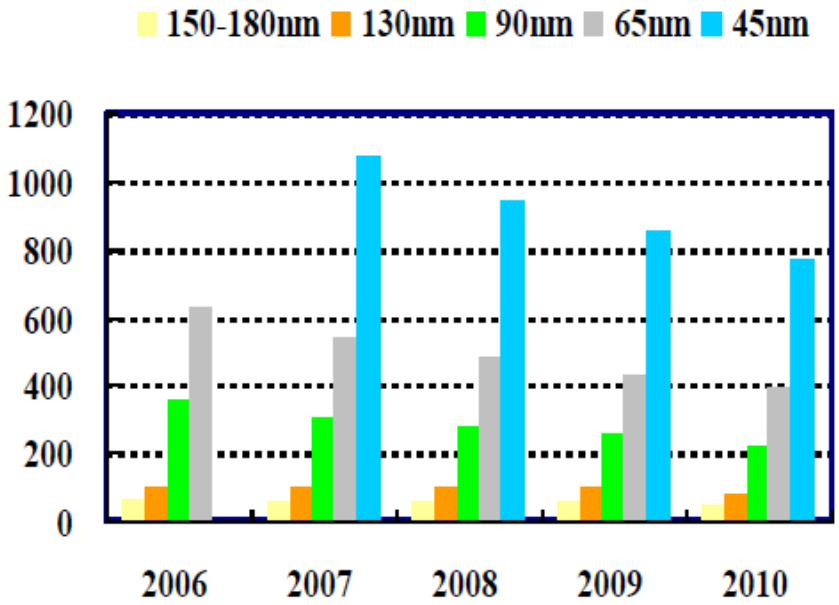
EBDW Motivation

- EUV: -- high CoO → might be suitable only for high-volume
  -- Unable to reach acceptable throughput
- Mask cost threatening the profitability of scaling
- EBDW: accurate printability and maskless!



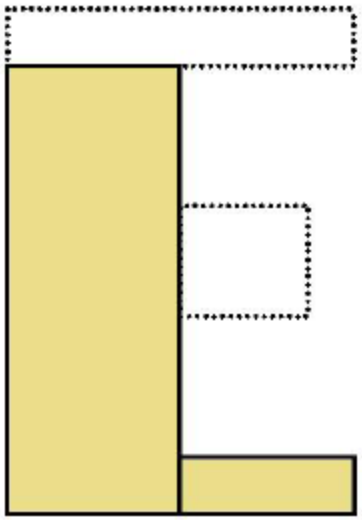
Source: Maruyama EIPBN'09

% of wafer cost that mask costs represent

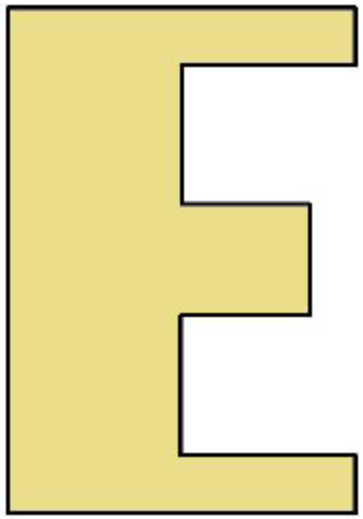
	250nm	130nm
ASIC	32%	56%
DRAM	7%	10%
Logic	12%	24%

Source: IC Knowledge

VSB vs. Character Projection



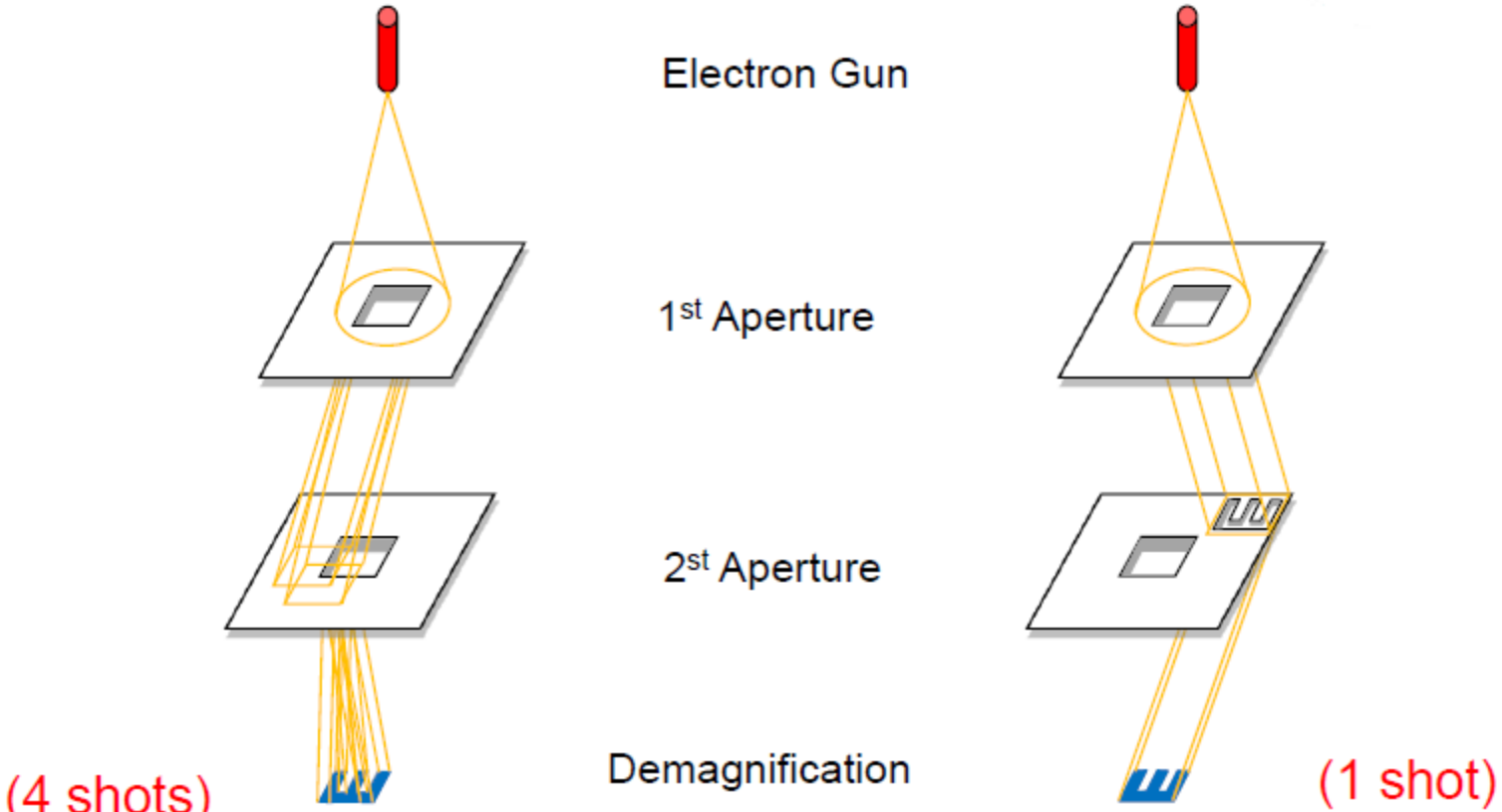
VSB (Variable Shaped Beam)



CP (Character Projection)

Source: Sugihara ISCAS'06

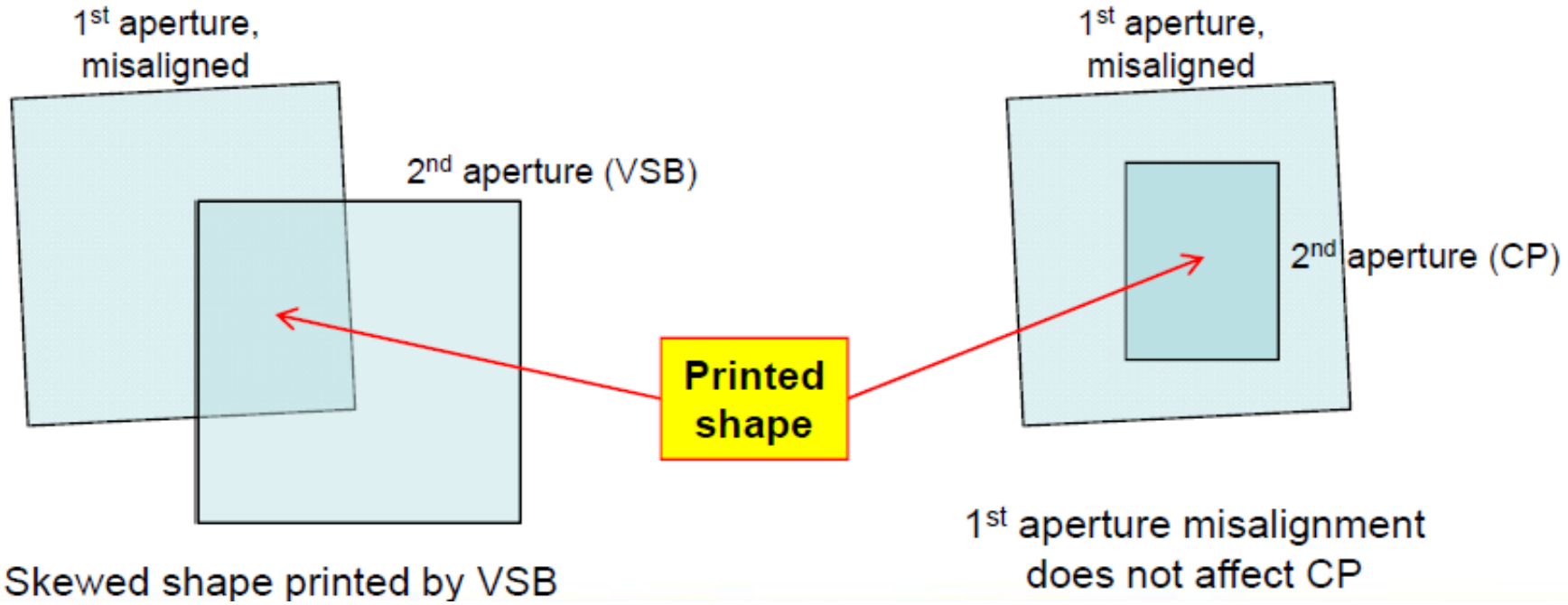
VSB vs. Character Projection



Source: ebeam.org

Aperture Misalignment

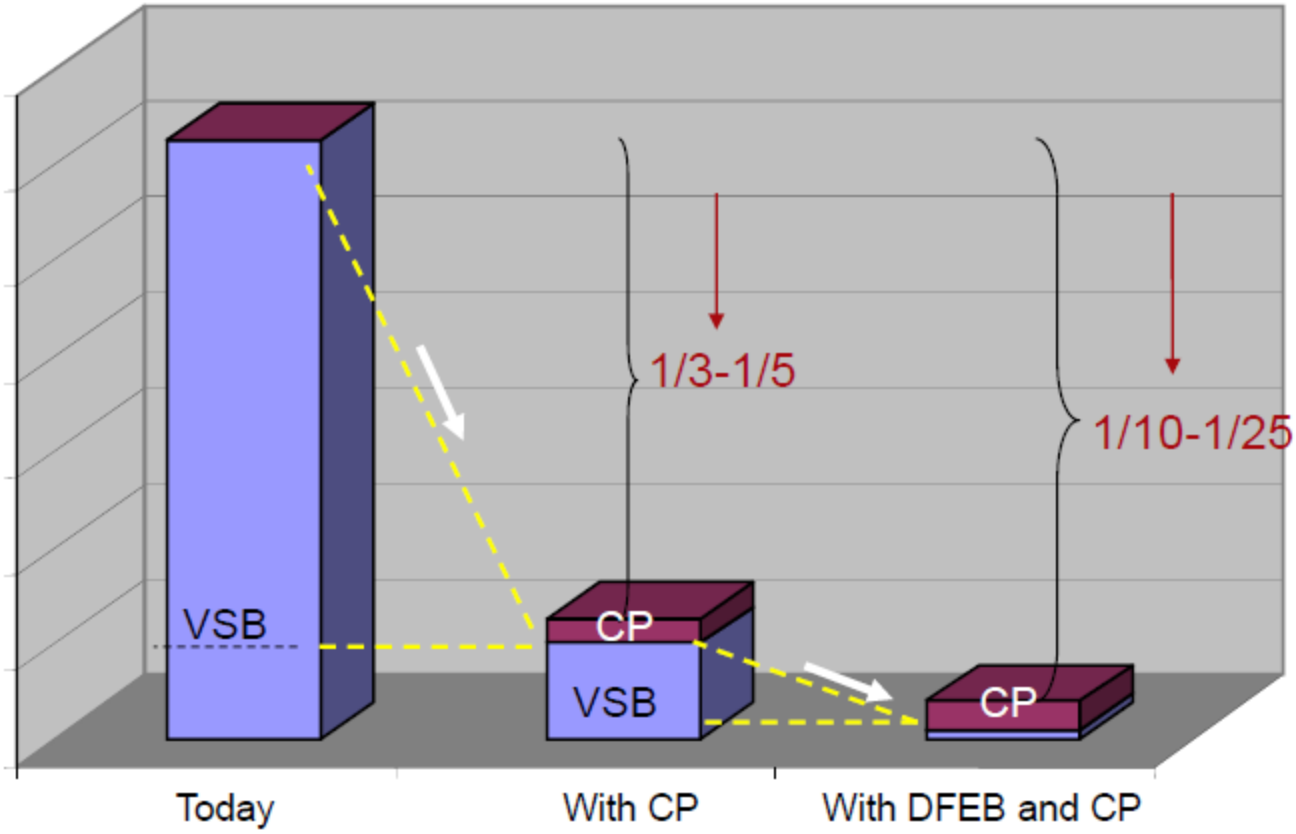
- CP unaffected by apertures misalignment



Source: ebeam.org

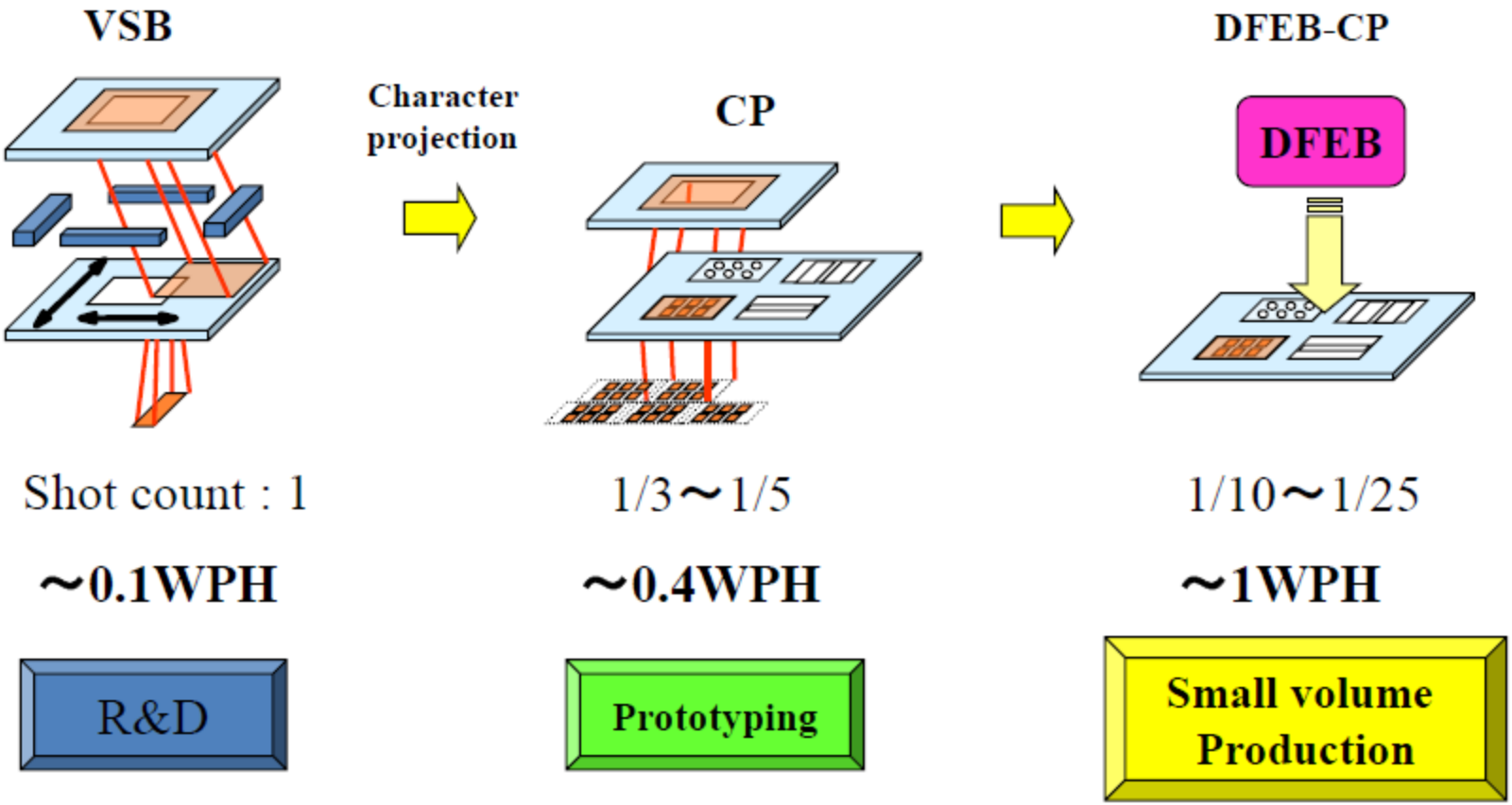
Shot Count

- Design for E-Beam
  - Co-designing the cell library and the stencil mask
  - Optimizing the physical design for CP



Source: ebeam.org

Throughput for Small Volume

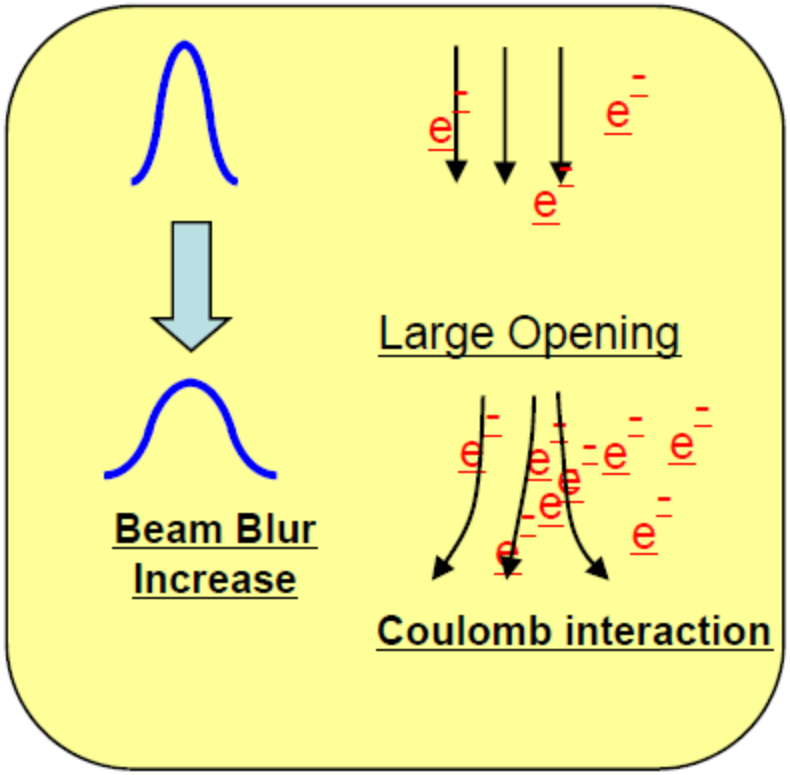


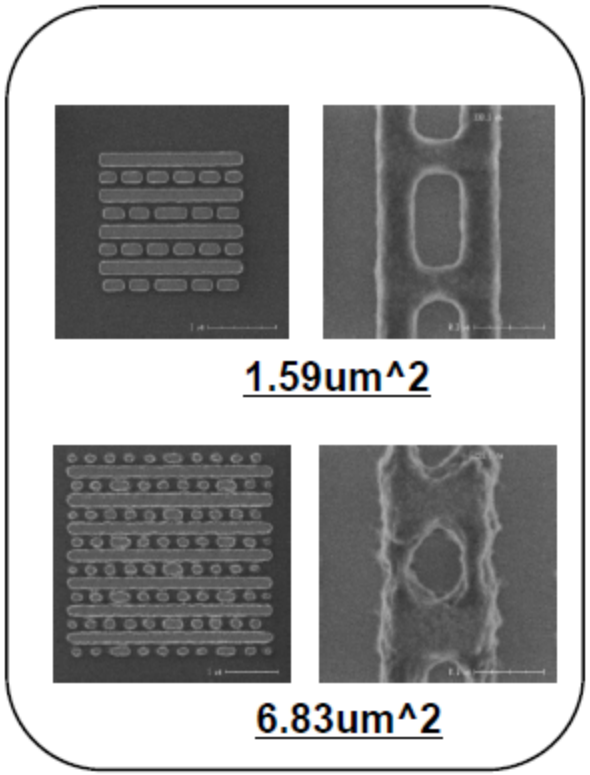
Source: Maruyama EIPBN'09

Limited Character Size

- Electrons in an e-beam repel each other
- As an e-beam becomes larger, printed image gets more blurred
- Use close to maximum allowed e-beam

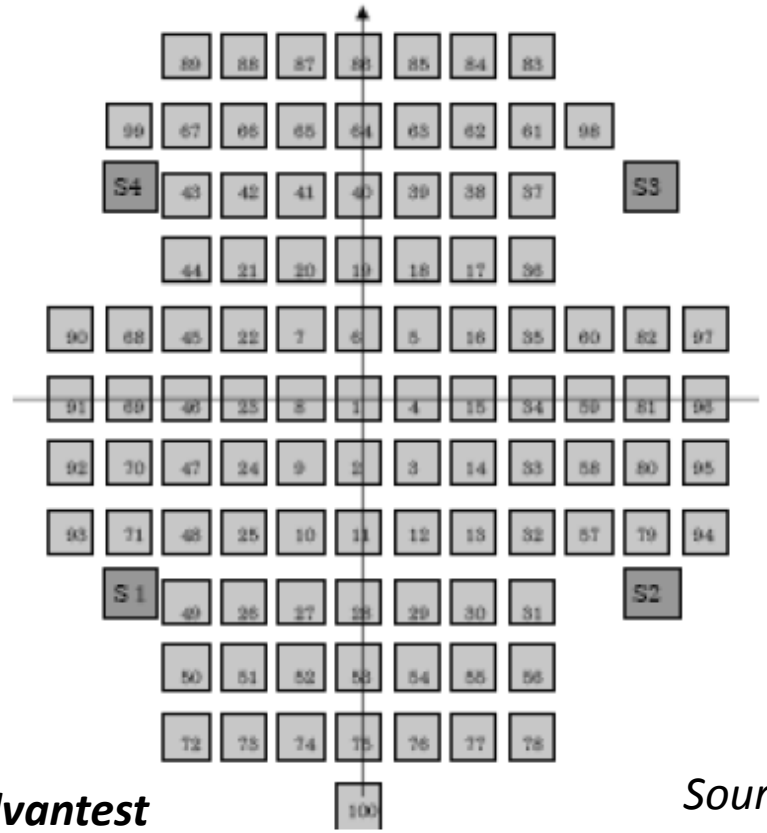
Entire Flip-flop in 1 shot is possible



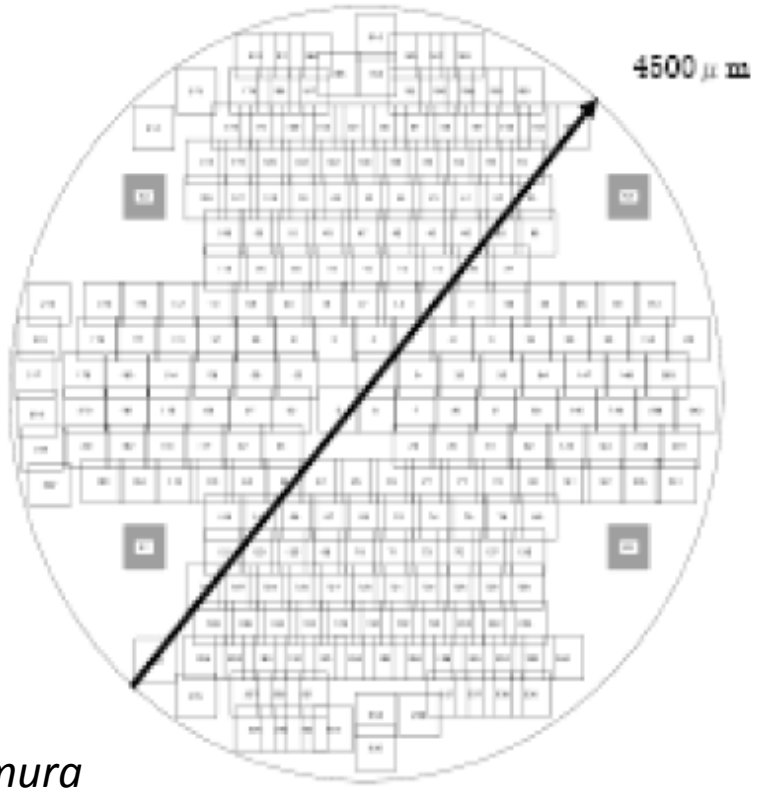


Source: ebeam.org

Limited Number of Characters



Advantest



Source: A. Fijumura ICCAD'09

Previous specification of the F3000 character block with 100 characters

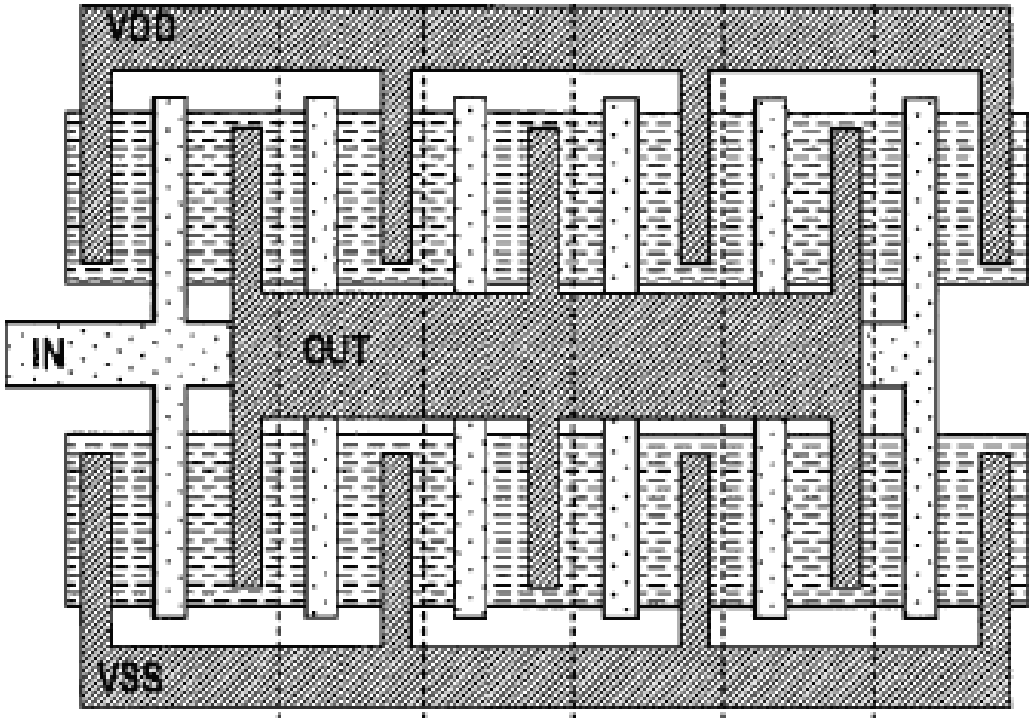
Up to 12 character blocks

The Packed Stencil allows, for example, this packed layout of 220-280 characters

Up to 20 character blocks

Minimizing the Number of Characters

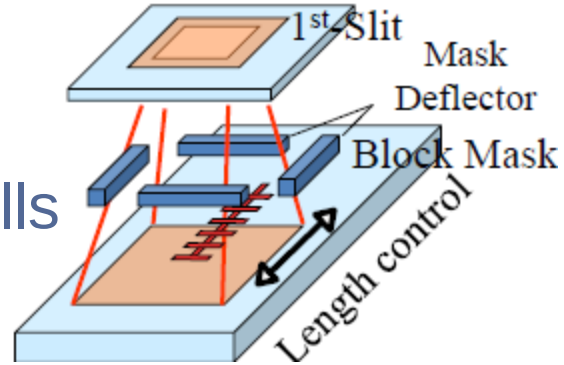
- Common Component as a character
- One cell can be printed using multiple shots of the same base character

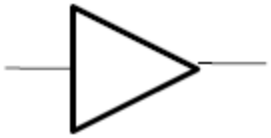
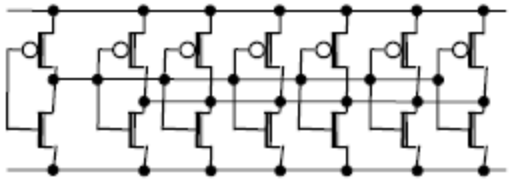
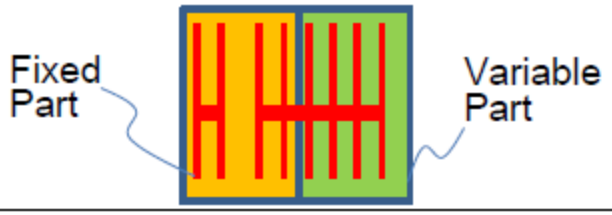
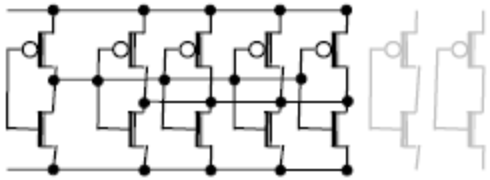
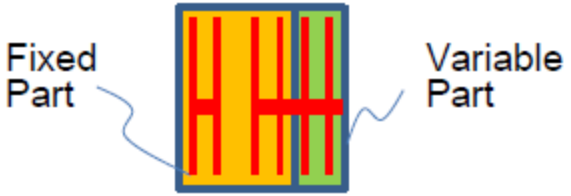
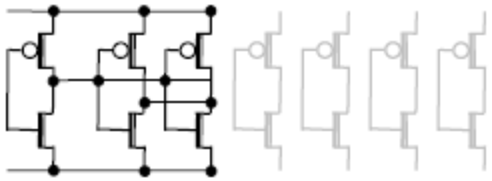
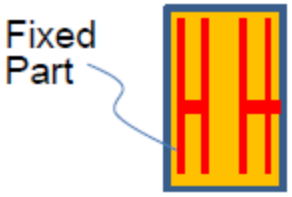


Source: A. Fijumura ICCAD'09

Minimizing the Number of Characters

- Large character is placed on a stencil
- Partial CP conversion to create smaller cells
  - Misalignment issues



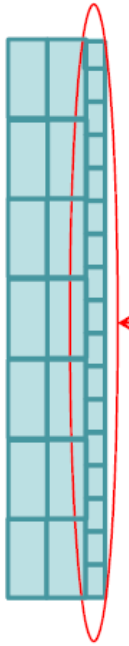
Logic Symbol	Projected Circuit image on wafer	Partial CP Conversion
Large Buffer 		
Middle Buffer 		
Small Buffer 		

Source: Maruyama EIPBN'09

Design for E-Beam

- Optimize shot count at every SP&R step
- Allow only discrete metal widths
- Arrange some cells in one direction for less characters (e.g., SRAM)
- Avoid M1 stub routing
- Enclose via geometries completely inside standard cell pins

14 CP shots
(Preferred)

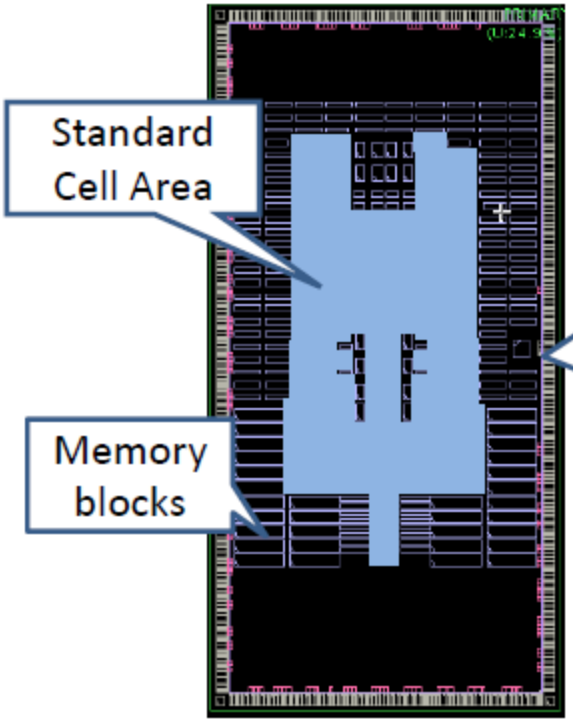


Source: ebeam.org

14 CP shots + VSB shots
(Avoid)

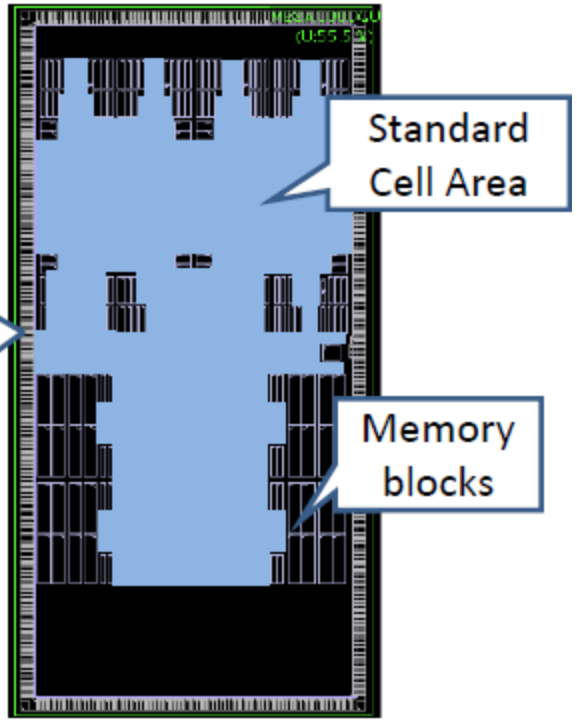
65nm Test Chip

Chip-A floor plan with DFEB library
Chip size = 4.2mm*8.4mm



1. Process: Fujitsu 65nm CMOS, 7 layer metal
2. Chip size: 4.2mm*8.4mm
3. VDD: 1.20v for core, 3.3v for IO
4. Clock: 166MHz, 162MHz and 33.3MHz
5. Random Logic size: 3+Mgates
6. Memory size: 786Kbit

Chip-B Floor plan with original library
Chip size = 4.2mm*8.4mm



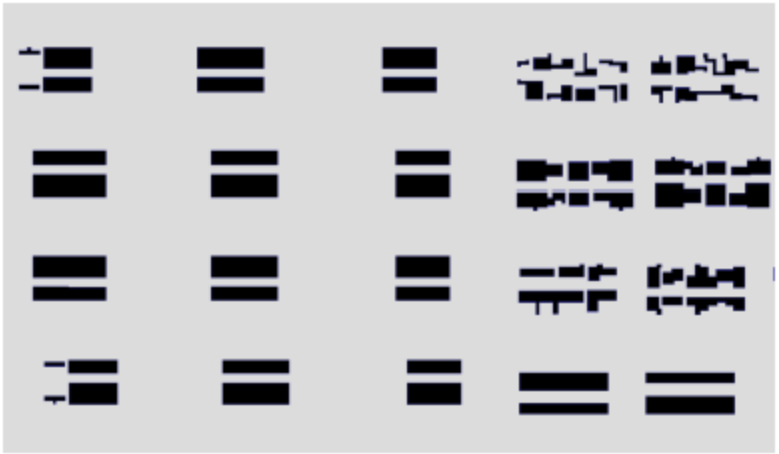
Standard-cell lib

Total cell count	
DFEB	Original
142	349

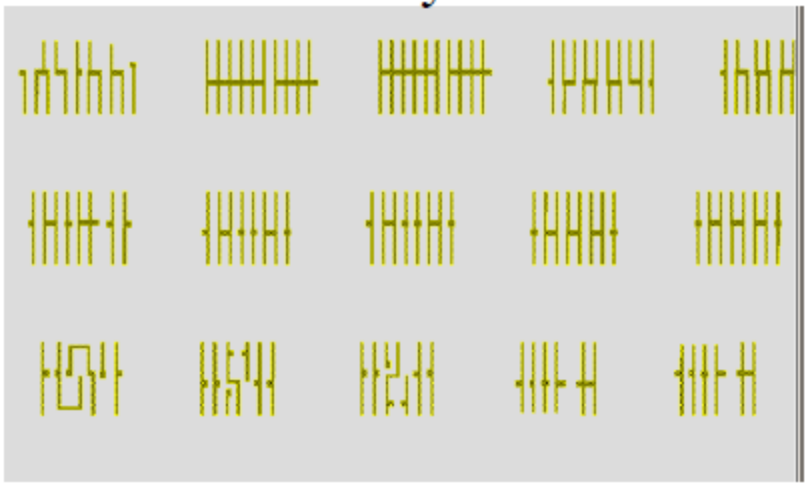
Source: Maruyama EIPBN'09

Character Layouts

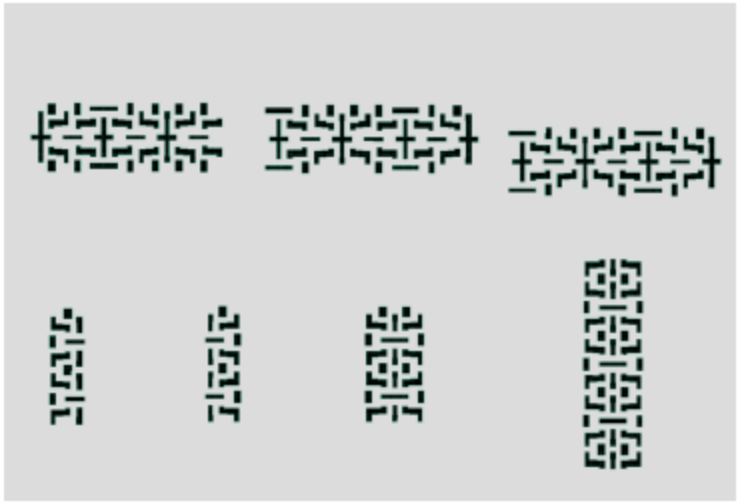
Diffusion (active)



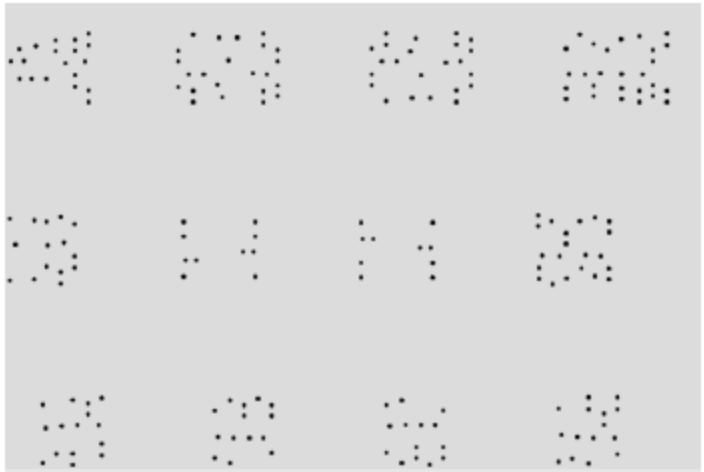
Poly



Metal-1

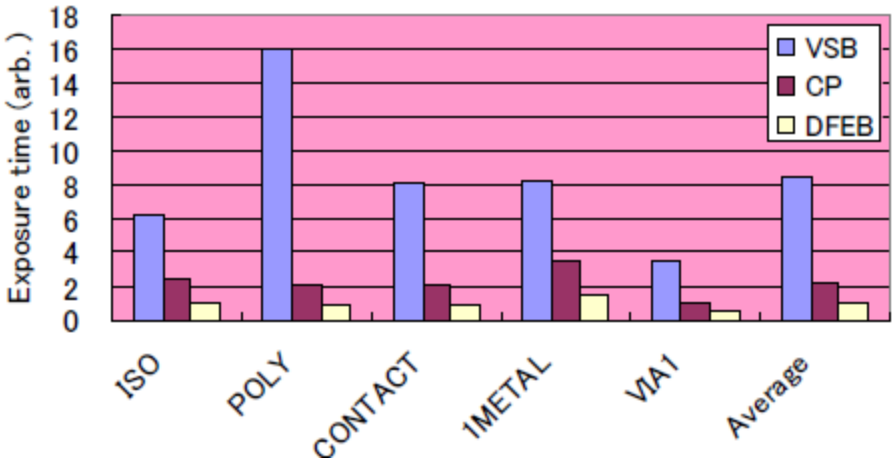


Contact

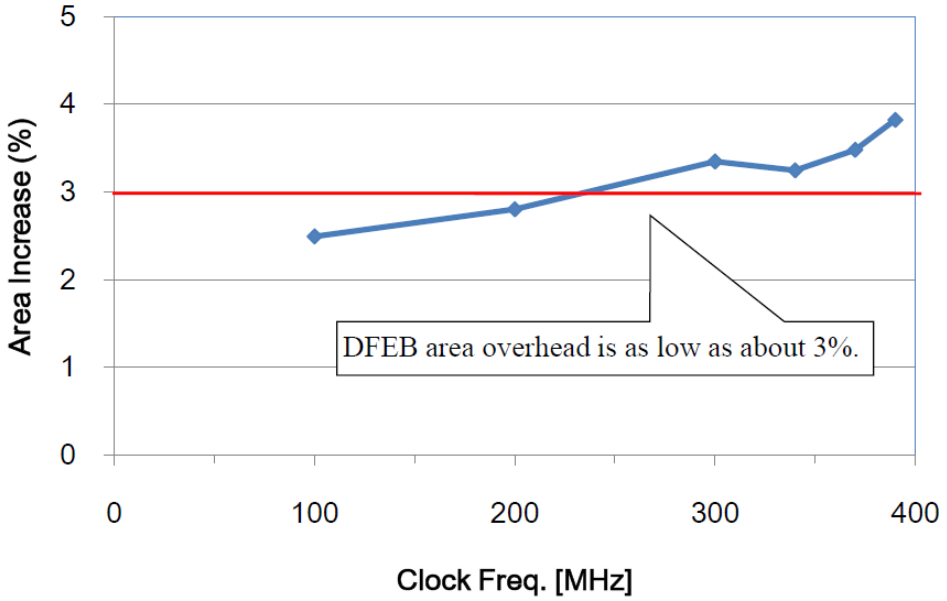


Source: Maruyama EIPBN'09

Area Overhead and Exposure Time



10x avg reduction in shot count compared to VSB (20x for poly)

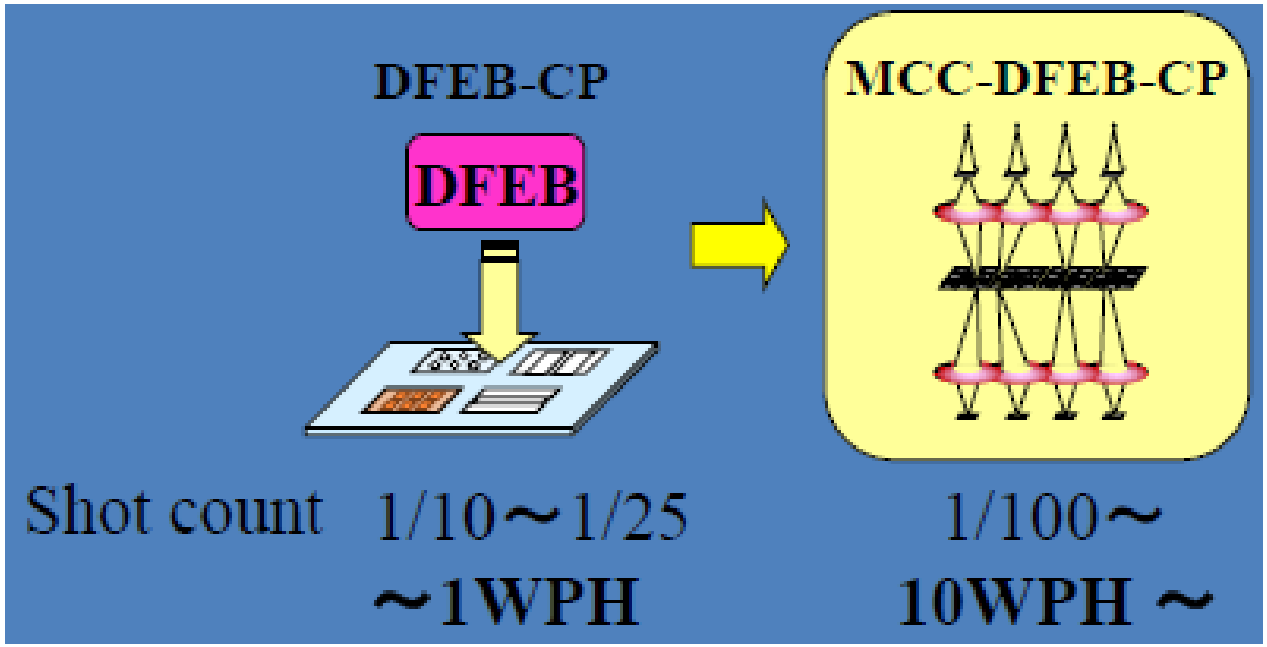


< 4% chip-area overhead

Source: Maruyama EIPBN'09

Future Directions

- Combine DFEB with Multi-Column Cell E-beam
  - Extension of character set
  - Throughput enhancement



Source: Maruyama EIPBN'09