Interconnect RC extraction

Amarnath Kasibhatla <u>amar@ee.ucla.edu</u>

What's Capacitance?

 $+\mathbf{Q} - \mathbf{Q}$ $\bigcirc \quad \ddagger \qquad \ddagger \qquad \begin{vmatrix} \vdots \\ \vdots \\ \vdots \end{vmatrix}$

Simplest model: parallel-plate capacitor

- It has two parallel plates and homogeneous dielectric between them
- The capacitance is
 - $-\epsilon$ permittivity of dielectric
 - A area of plate $C = \mathcal{E} \frac{A}{d}$
 - *d* distance between plates
- The capacitance is the capacity to store charge
 - charge at each plate is
 - one is positive, the other is negative

$$Q = CV$$

General Picture



- For multiple conductors of any shapes and materials, and in any dielectric, there is a capacitance between any two conductors
- Each conductor has a resistance associated with it and is calculated using foundry-provided sheet-resistance tables.
- Resistance of a net is calculated independent of its neighbors.

Capacitance Matrix

Capacitance is often written as a symmetric matrix



 $C = \begin{array}{cccc} c_{11} & c_{12} & c_{13} \\ c_{21} & c_{22} & c_{23} \\ c_{31} & c_{32} & c_{33} \end{array}$

 $c_{ii} = -\sum_{j=1}^{m} c_{ij} (j \neq i)$ is the self-capacitance for a conductor • *e.g.*, $c_{11} = c_{12} + c_{13}$

The charge is given by $Q^m = C^{mm} (V^m)^T$

• e.g.,
$$q_1 = c_{11}v_1 - c_{12}v_2 - c_{13}v_3$$

= $c_{12}(v_1 - v_2) + c_{13}(v_1 - v_3)$

Application in VLSI Circuits

- **Conductors: metal wire, via, polysilicon, substrate**
- Dielectrics: SiO₂,...
- Total cap for a wire
 - delay, power
- Mutual cap between wires
 - signal integrity



Characteristics of Capacitance

Coupling capacitance virtually exists only between adjacent wires or crossing wires but more pronounced between layers i and i-2/i+2.



Capacitance can be pre-computed for a set of (localized) interconnect structures using a GOLDEN 3-D field solver extraction tool.



 $C_{i,i-2}$ coupling between victim and aggressor on layer *i*-2



 $C_{i,i}$ lumped capacitance for victim on layer *i*

 $C_{i,i-2}$ coupling between victim and aggressor on layer *i*-2

Shielding Effect of Ground and Neighbors

.

.....

..........

..........

.....

layer <i>i</i>	$C_{i,i}$	C _{<i>i</i>,<i>i</i>-2}
no GND	458.4	130.1(28.4%)
 + GND	486.6	79.49(16.3%)
+ neighbors	1428	24.77(1.8%)
layer <i>i-2</i>		

 $C_{i,i}$ lumped capacitance for victim on layer *i*

C_{*i*,*i*-2} coupling between victim and aggressor on layer *i*-2



Coupling between Layers *i* and *i*-2



2x 4x 8x12x486.6 534.5 581.3 622.2 635.9 C_{*i*,*i*-2} 79.49 48.45 21.99 3.47 2.47

lumped capacitance for victim on layer *i* coupling between victim and aggressor on layer i-2



Effect of Non-immediate Neighbors (Second Aggressor)



$C_{i,i}$	1436
C_1	616.6
Cr	616.5

 $C_{i,i}$: lumped capacitance for victim.

Effect of Non-immediate Neighbors (Second Aggressor)



$C_{i,i}$	1436	1436(0%)
C_1	616.6	639.8(+3%)
Cr	616.5	639.5(+3%)

 $C_{i,i}$: lumped capacitance for victim.

Table Generation for Lateral, Area andFringe Capacitances



Functions of (w,s)
Pre-computed for per-side per unit-length



Table Generation for Crossing Capacitances



Function of (w,s,wc,sc)







Per-side fringe capacitance = $C_F(w,s_1) * L_1$



2 Add in Per-Side Area, Fringe and Lateral Capacitances



BFind All Crossovers and Crossunders







One-corner crossover correction = $C_{over}(w,s_1,w_c,s_c)$







One-corner crossover correction = $C_{over}(w,\infty,w_c,s_c)$

Summary of Capacitance Extraction

- Find nearest neighbors on the same layer
- Add in per-side lateral, area and fringe capacitances w.r.t. each neighbor
- S Find all crossovers and crossunders
- Add in crossing capacitances corner-by-corner w.r.t. each crossover and crossunder

Sum of capacitance components in above steps is the lumped capacitance of the victim.

References

J. Cong, L. He, A. B. Kahng, D. Noice, N. Shirali and S. H.-C. Yen, "Analysis and Justification of a Simple, Practical 2 1/2-D Capacitance Extraction Methodology", *ACM/IEEE Design Automation Conference*, June 1997, pp.627-632

<u>http://eda.ee.ucla.edu/pub/c7.pdf</u>

L. He, N. Chang, S. Lin, and O. S. Nakagawa, "An Efficient Inductance Modeling for On-chip Interconnects", (nomination for Best Paper Award)*IEEE Custom Integrated Circuits Conference*, San Diego, CA, pp. 457-460, May 1999.

<u>http://eda.ee.ucla.edu/pub/c11.pdf</u>

M. Xu and L. He, "An efficient model for frequency-based on-chip inductance," IEEE/ACM International Great Lakes Symposium on VLSI, West Lafayette, Indiana, pp. 115-120, March 2001.

<u>http://eda.ee.ucla.edu/pub/c18.pdf</u>