Matching in Analog Integrated Circuits

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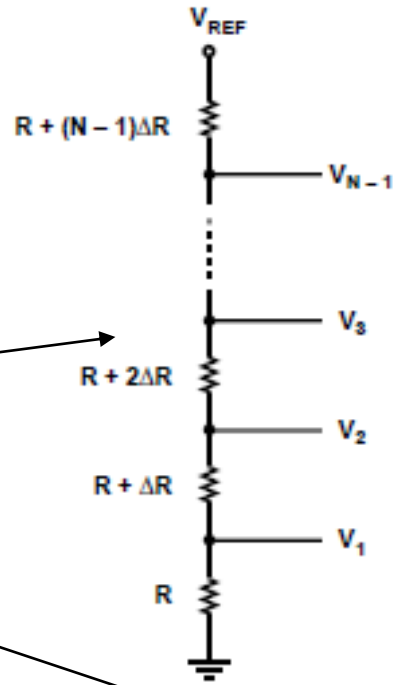
In Analog Design Ratios are more important than the Absolute Values

- Absolute values depend on large parameter drifts.Ratios depend on local variation of parameters.
- Specs of Analog/RF Circuits rely critically on Ratios
  - Cap/Res:
    - INL, DNL in DACs
  - MOS:
    - CMRR, PSRR of opamps
    - Gain error in amplifiers
    - I/Q mismatch in RF Rx



$$INL_j(max) = INL_{N/2} = \frac{N}{8}\left(\frac{\Delta R}{R}\right)V_{REF}$$

$$DNL(max) \equiv \left(\frac{\Delta R}{2R}\right)V_{REF}$$

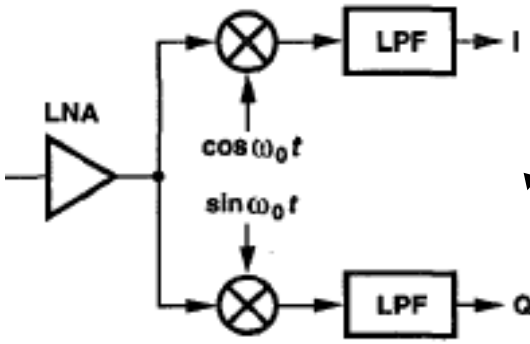
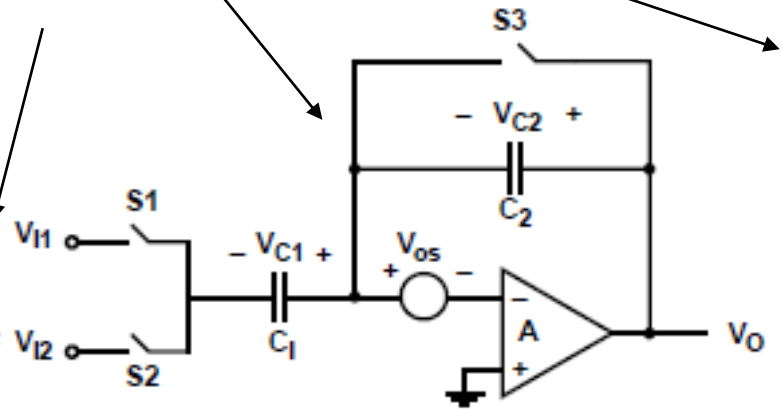
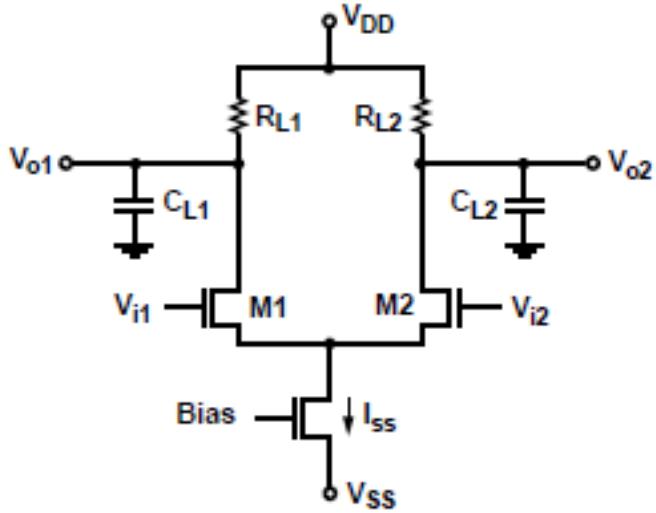


Fig. 2. Direct-conversion receiver.



$$V_O = \left(\frac{C_1}{C_2}\right)(V_{I1} - V_{I2}) + V_{os}$$



Device Matching

- Capacitor

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL \qquad \left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2$$

- Resistor
  - L >> W

$$R = \frac{L}{W} R_{\square} = \frac{L}{W} \cdot \frac{\bar{\rho}}{x_j} \qquad \left(\frac{\Delta R}{R}\right)^2 = \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta \bar{\rho}}{\bar{\rho}}\right)^2 + \left(\frac{\Delta x_j}{x_j}\right)^2$$

- Caps match better than Resistors

$$\left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right) << \left(\frac{\Delta \bar{\rho}}{\bar{\rho}}\right) \qquad \left(\frac{\Delta W}{W}\right)_{cap} < \left(\frac{\Delta W}{W}\right)_{res} \qquad \left(\frac{\Delta t_{ox}}{t_{ox}}\right) < \left(\frac{\Delta x_j}{x_j}\right)$$

- Transistors (Pelgrome JSSC oct.1989)

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL} + S_\beta^2 D^2 \qquad \sigma^2(V_T) = \frac{A_{V_T}^2}{WL} + S_{V_T}^2 D^2$$

A_β , A_{vt}, S_β , S_{vt} are tech constants, D is the seperation between the devices.

Accuracy ↔ Speed Tradeoff

- As W & L are increased, two effects happen:
  - The individual contributions for mismatch i.e. (ΔW/W) & (ΔL/L) decrease
  - Actual variation of parameters i.e. ΔW, ΔL also decrease due to more spatial averaging.
    - This happens till the large distance effects kick in.
- Hence, mismatch of the devices decreases as they are made bigger.
- However, speed decreases as devices get bigger. This points to a fundamental trade-off between Accuracy ↔ Speed.

Symmetry and Matching

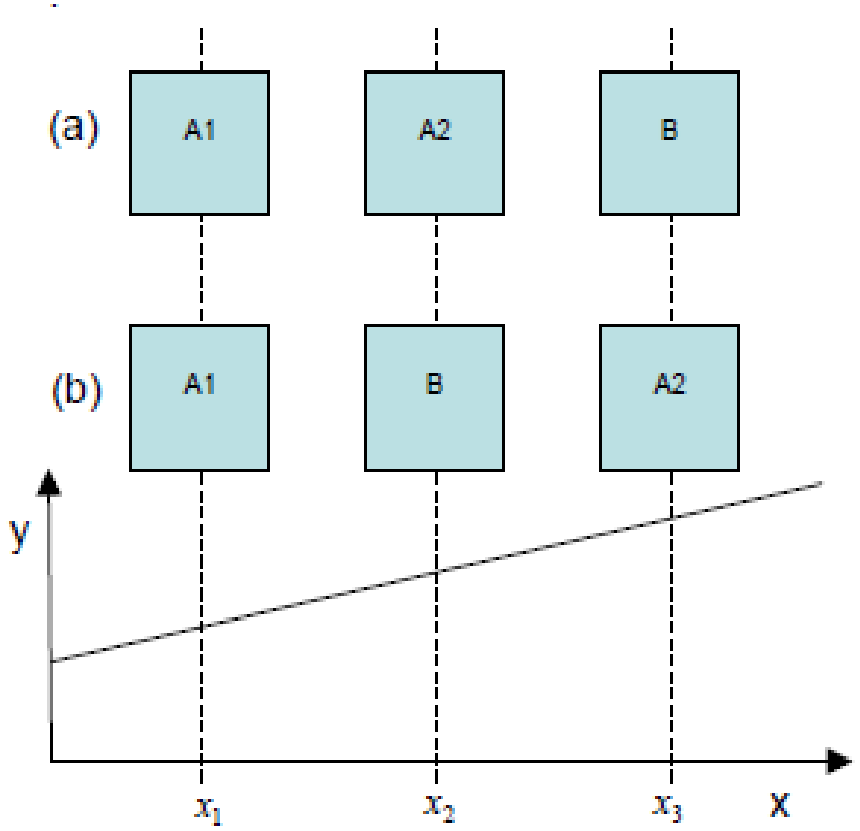
- Interdigitized (common centriod) layout
  - Assume that the gradient of variation is described as; y = mx + b
  - A (composed of A1 & A2) should be twice of B.

- For layout (a) we have:

$$A1 = mx_1 + b$$
$$A2 = mx_2 + b$$
$$B = mx_3 + b$$
$$\frac{A1 + A2}{B} = \frac{m(x_1 + x_2) + 2b}{mx_3 + b} \neq 2$$

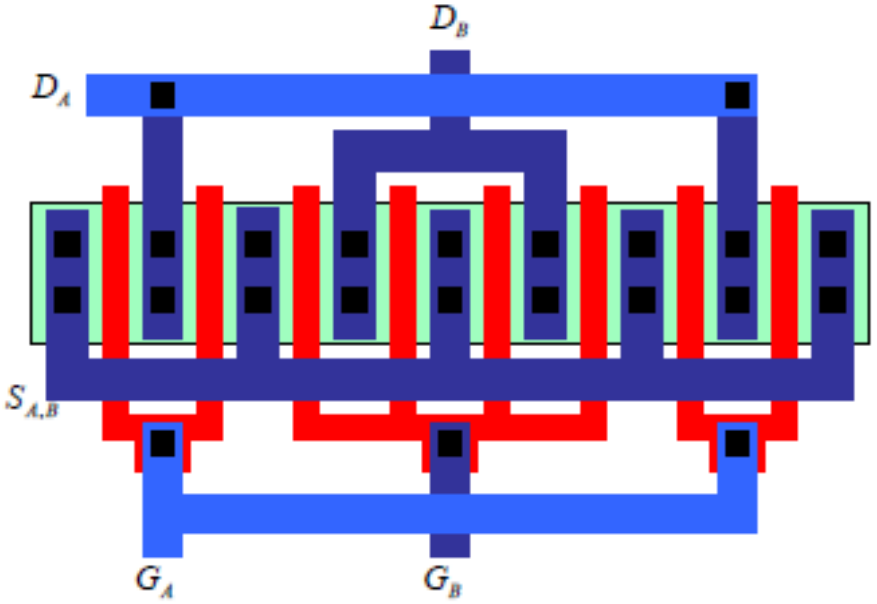
- For layout (b) we have:

$$A1 = mx_1 + b$$
$$A2 = mx_3 + b$$
$$B = mx_2 + b$$
$$\frac{A1 + A2}{B} = \frac{m(x_1 + x_3) + 2b}{mx_2 + b} = 2$$

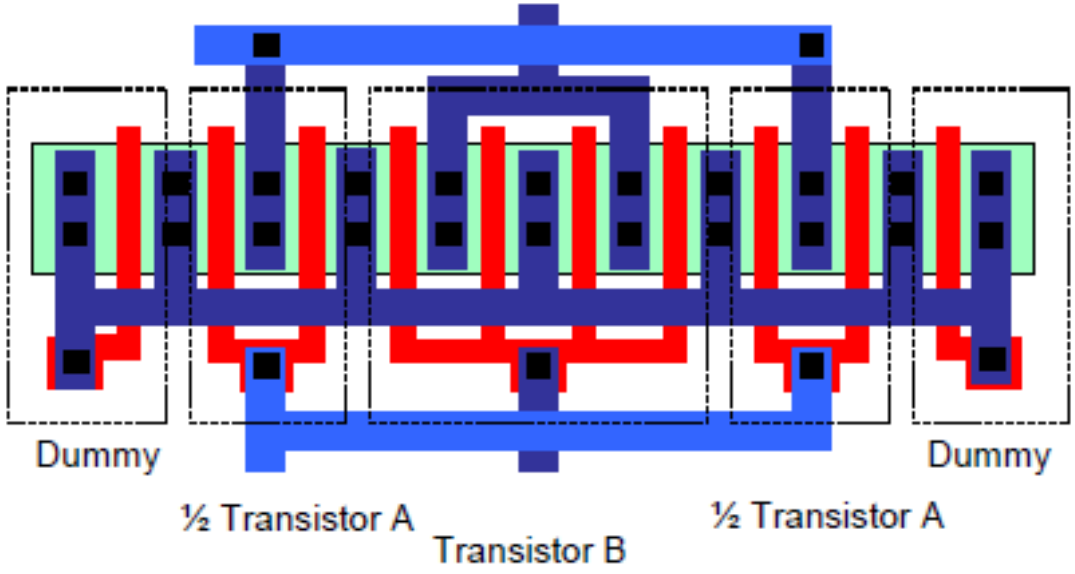


Symmetry and Matching

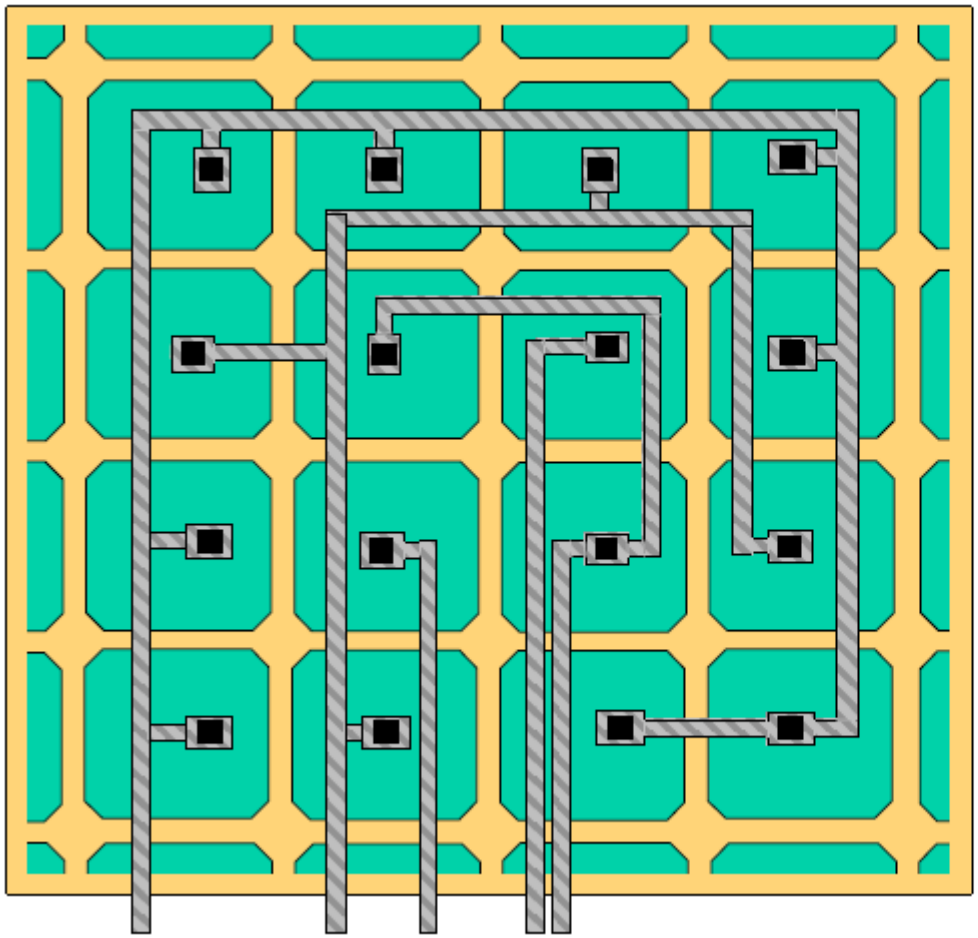
- Dummy transistors improves the matching between transistor A and B by providing similar environment to the circuit that is on the boundary of a layout.

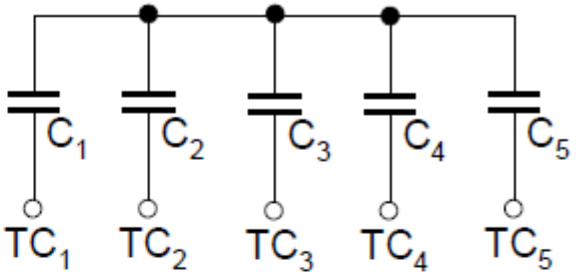


An Example of common centroid layout



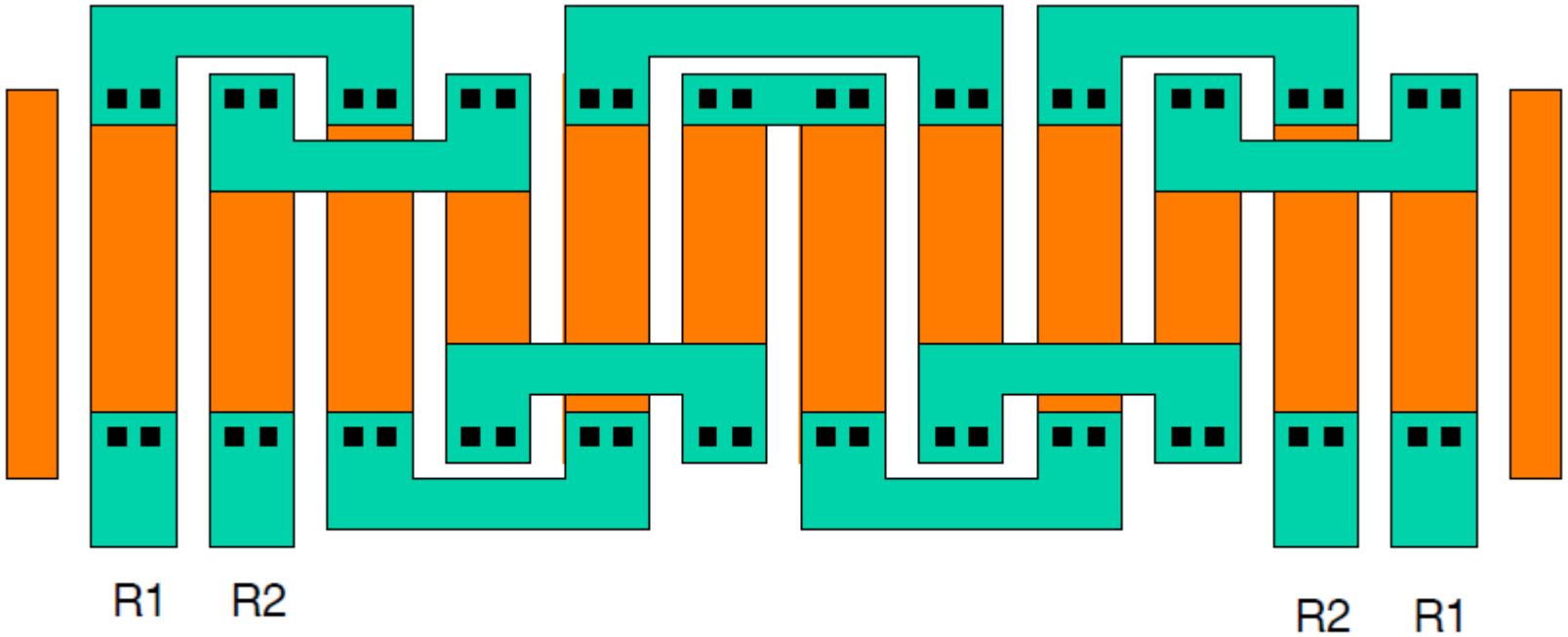
Capacitor Layout





$C_2 = C_1$
$C_3 = 2C_1$
$C_4 = 4C_1$
$C_5 = 8C_1$

Resistor Layout



Conclusions

- Matching is very critical for Analog IC designs.
- Good layout techniques help in improving matching.
- However, as the feature size decreases, the variation is increasing.
- Designers are resorting to various techniques to manage the growing mismatches.
  - Auto-Zeroing in Comparators.
  - Digital Calibration for mismatch correction.
  - Dynamic Element Matching to randomize or shape the mismatch errors.