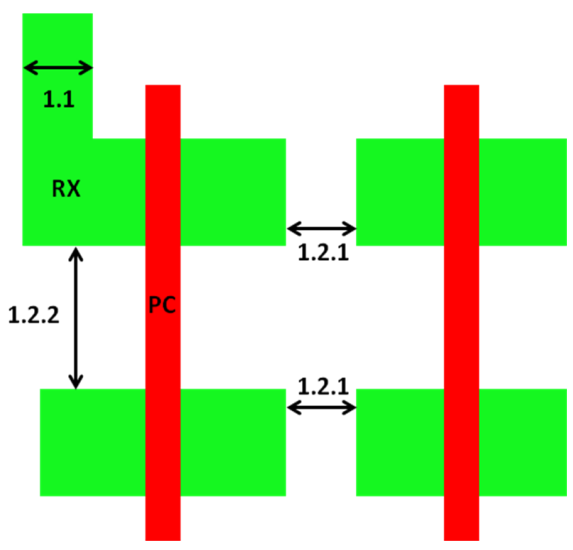
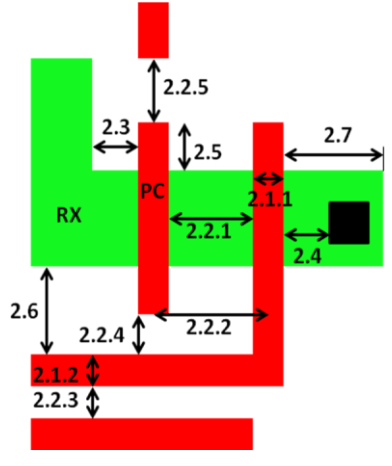
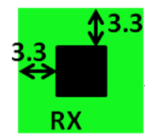


Supported DRs in UCLA-DRE Design Rule Evaluator Release 1.1

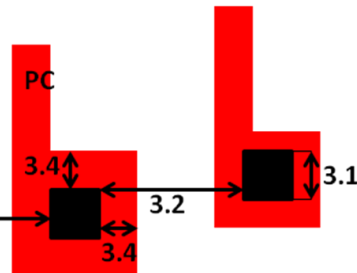
	Rule	#	Note
1. Diffusion (RX)	Min diff-width	1.1	
	Diff-to-diff spacing same network	1.2.1	
	Diff-to-diff spacing p/n network	1.2.2	
			
2. Poly (PC)	Gate poly width	2.1.1	We assume unidirectional gates
	Field poly width	2.1.2	Field poly is all non-gate poly in any direction
	Gate poly spacing (side to side)	2.2.1	
	Fixed Gate pitch	2.2.2	Only for fixed-gate implementation
	Field poly spacing (side to side)	2.2.3	Field poly is all non-gate poly in any direction
	Gate poly line-end to field poly side	2.2.4	
	Gate poly line-end gap (tip to tip)	2.2.5	
	Gate poly-to-diff spacing	2.3	
	Gate poly-to-contact spacing	2.4	
	Gate poly line-end extension	2.5	
	Field poly-to-diff spacing	2.6	
	Diffusion extension of gate	2.7	
			

3. Contact (CA)	Contact width	3.1	
	Contact spacing	3.2	This is edge-edge spacing (full common run-length). Center-center contact spacing (no or some common run-length) is not included because these have typically a large spacing in our implementation. This rule will have an effect and will be taken into consideration once we include evaluation of staggered poly-contacts.
	Contact enclosure within diff	3.3	
	Contact enclosure within poly	3.4	
	Contact to diffusion spacing	3.5	

Diffusion contact

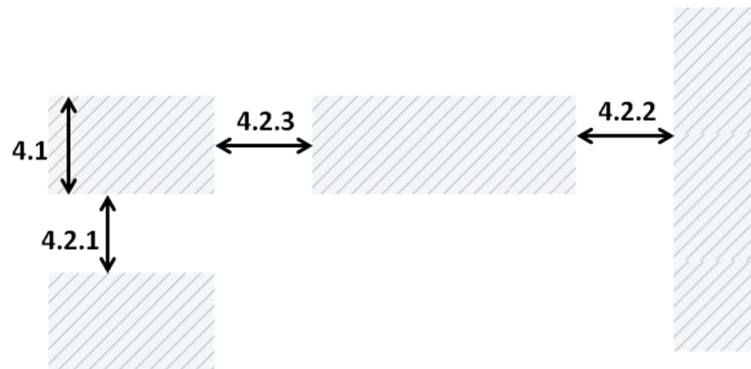


Poly contacts

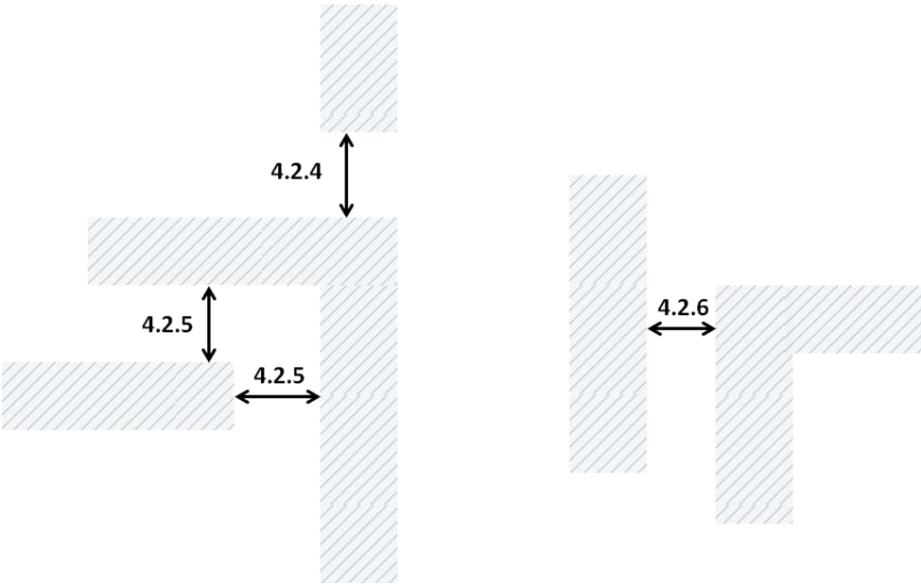


3.5

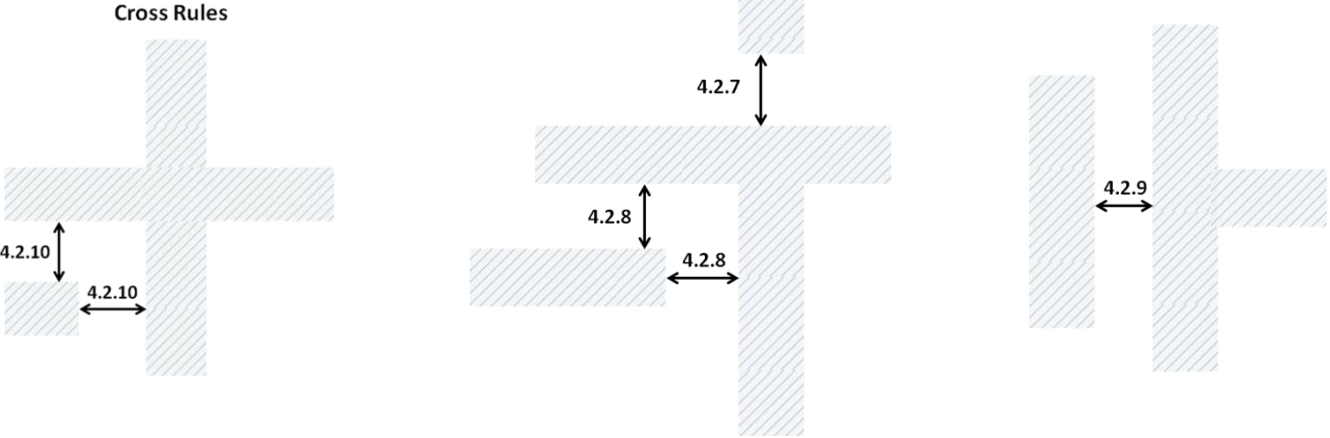
4. Metal 1 (M1)	M1 width	4.1	
	M1 spacing (side to side)	4.2.1	We are planning to perform some sort of simple M1 routing similar to probabilistic congestion estimation techniques used in global routing.
	M1 spacing (tip to side)	4.2.2	
	M1 spacing (tip to tip)	4.2.3	
	M1 spacing (L-bend to outer line-tip)	4.2.4	
	M1 spacing (L-bend to inner line-tip)	4.2.5	
	M1 spacing (L-bend to outer line-side)	4.2.6	
	M1 spacing (T-bend to outer line-tip)	4.2.7	
	M1 spacing (T-bend to inner line-tip)	4.2.8	
	M1 spacing (T-bend to outer line-side)	4.2.9	
	M1 spacing (Cross to inner line-tip)	4.2.10	
	M1 spacing with wide M1 power rail	4.2.11	
	M1 overhang over diff-contact 1 st 2 sides	4.3.1	
	M1 overhang over diff-contact 2 nd 2 sides	4.3.2	
	M1 overhang over poly-contact 1 st 2 sides	4.3.3	
	M1 overhang over poly-contact 2 nd 2 sides	4.3.4	



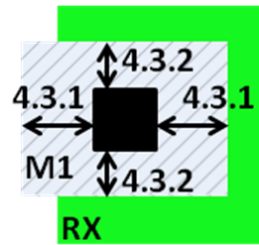
L-Bend Rules



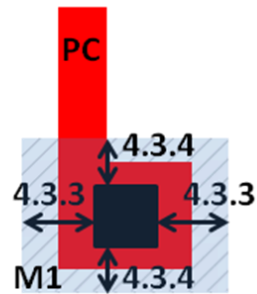
T-Bend Rules



Diffusion contact

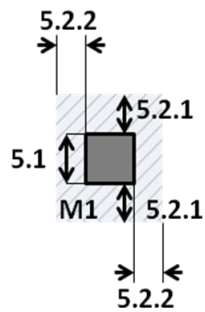


Poly contacts

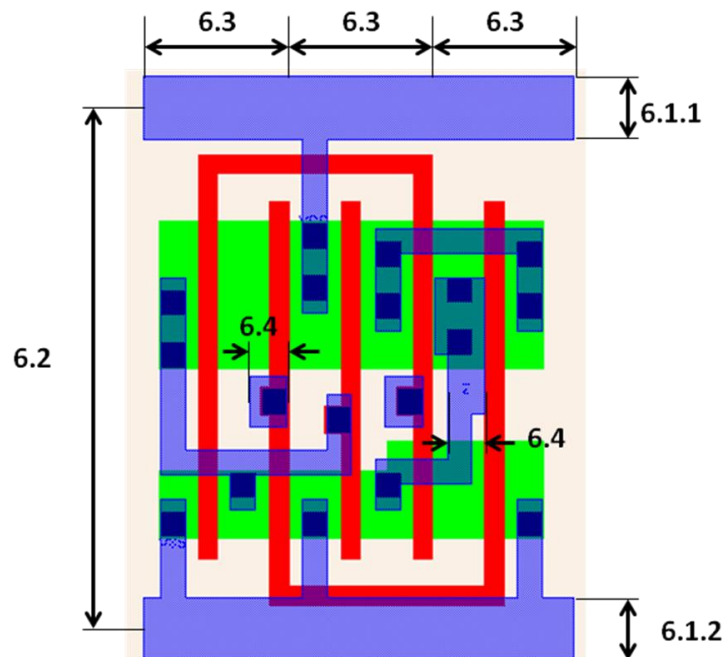


5. Via 1 (V1)	Via1 width	5.1	
	Via 1 enclosure within M1 first 2 sides	5.2.1	
	Via 1 enclosure within M1 second 2 sides	5.2.2	

Via 1



6. Cell	Vdd power-rail width (on M1)	6.1.1	
	GND power-rail width (on M1)	6.1.2	
	Cell-height	6.2	Either # of M3 tracks or exact value
	Cell unit-width	6.3	Only if cell-width is discretized
	I/O pins M1 width	6.4	



7. Styles	Fixed gate-pitch	7.1.1	Yes/no
	1D-poly	7.1.2	Yes/no
	Limited poly routing	7.1.3	Yes/no, only allow U and W shapes poly
	Power-straps	7.2	With diffusion or M1
	PMOS vertical location	7.3.1	Top/bottom, center of row, or near p/n interface
	NMOS vertical location	7.3.2	Top/bottom, center of row, or near p/n interface
	Poly line-end extension span cell-height	7.4	Yes/no
	Discrete cell width	7.5	Yes/no
	Diff-contact redundancy	7.6.1	Yes/no
	Poly-contact redundancy	7.6.2	Yes/no
	Input pins access requirement on M1	7.7.1	Block neighboring track if IO M1 width > min M1 width for length of input pad
	Output pins access requirement on M1	7.7.2	Block neighboring track if IO M1 width > min M1 width for length of vertical wire connecting n/p transistors connected to final cell-outputs

Process Parameter		Note
General	Grid size	
	Overlay (3σ)	
	CDU (3σ)	
	Line-end pull-back (mean)	
Defects	Defect density, D_0 [faults/m ²]	
	Critical defect size, r_0	Defect size with peak density (Eq. 2 in draft)
	Maximum defect size, r_{max}	(Eq. 2 in draft)
	Fab cleanliness parameter, n	(Eq. 2 in draft)
	Diff-contact hole failure rate [ppm]	Contact-defectivity
	Poly-contact hole failure rate [ppm]	Contact-defectivity
	Critical M1 width	Min acceptable width for defect not to cause failure
	Critical Poly width	
Tapering	Critical Contact width	
Tapering	parameter n	(footnote 11 in draft)
	Parameter k	(footnote 11 in draft)
Congestion related	α, β parameters for vertical direction	(Section II-C in draft)
	α, β parameters for horizontal direction	(Section II-C in draft)
	γ parameter	For considering pin-access overhead (Section II-C)