Supervia: Relieving Routing Congestion using Double-height Vias

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Master of Science Project Presentation

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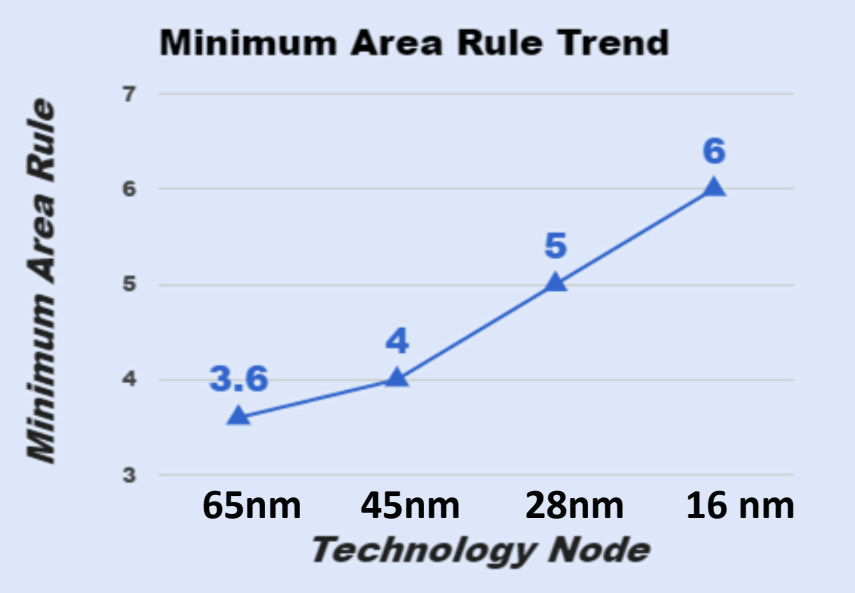
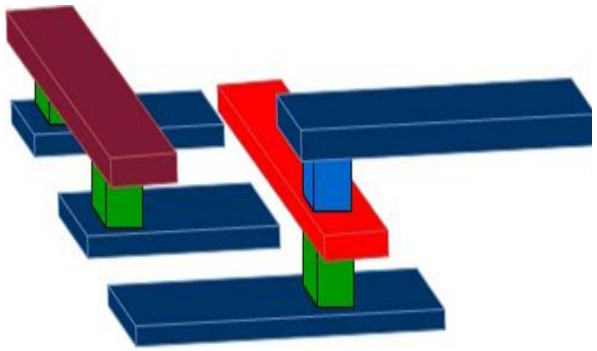
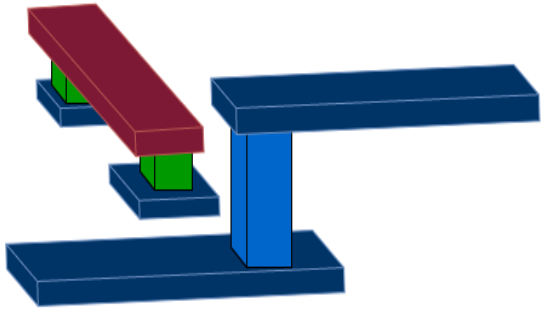
5th June, 2017

Motivation





Conventional stacked via with intermediate landing pad



Proposed Supervia structure -- double-height via

- Minimum area rule ↑ → Via blockage ↑ → Congestion ↑
- Via blockage on M2 : **11% (3x) & 18% (5x)**
- MinArea rule shows **increasing trend** in newer nodes

Possible Reasons for Min Area Rule

- **Lithography**
  - Patterning small polygons difficult for sub-20nm node.
  - Multiple Patterning improves pitch but not minimum achievable polygon area
- **Deposition**
  - Deposition of uniform **barrier/seed layer** difficult
  - PVD/CVD/electroplating used for deposition
  - Minimum trench area required
- **CMP**
  - Hardness mismatch between Cu and SiO_X
  - Difficult to optimize for small metal polygons

Impact of Minimum Area Rule

TABLE I: Maximum achievable utilization with different minArea rules (1x, 3x, 5x, 7x) and different numbers of metal layers.

Testcase	#Layers	Tool	Via Generate	MinArea rule			
				1x	3x	5x	7x
MIPS_4	4	*Enc_v11*	N	95%	90%	86%	<60%
	4	*Invs_v16*	N	97%	95%	92%	91%
	4	*Invs_v16*	Y	97%	97%	95%	94%
MIPS_5	5	*Enc_v11*	N	97%	94%	93%	<60%
	5	*Invs_v16*	N	97%	95%	93%	92%
	5	*Invs_v16*	Y	98%	98%	97%	95%
M0_5	5	*Enc_v11*	N	84%	75%	68%	<60%
	5	*Invs_v16*	N	88%	77%	71%	69%
	5	*Invs_v16*	Y	91%	89%	88%	84%
M0_6	6	*Enc_v11*	N	88%	82%	74%	<60%
	6	*Invs_v16*	N	94%	91%	89%	85%
	6	*Invs_v16*	Y	95%	95%	92%	91%
AES_5	5	*Enc_v11*	N	92%	85%	79%	<60%
	5	*Invs_v16*	N	97%	95%	92%	87%
	5	*Invs_v16*	Y	91%	88%	86%	84%
AES_6	6	*Enc_v11*	N	93%	86%	83%	<60%
	6	*Invs_v16*	N	97%	95%	95%	93%
	6	*Invs_v16*	Y	97%	95%	94%	93%

We report numbers from two tools, *Cadence Encounter v11.10*, and *Cadence Innovus v16.10*. Via Generate options is used to generate optimal via structures considering MinArea rule

- MinArea Rule ↑ , Utilization ↓ , Area ↑
- **Utilizations drop up to 7% even using MinArea aware router (Innovus) with via generation**
- **Sub-16nm node is expected to have MinArea > 6x**

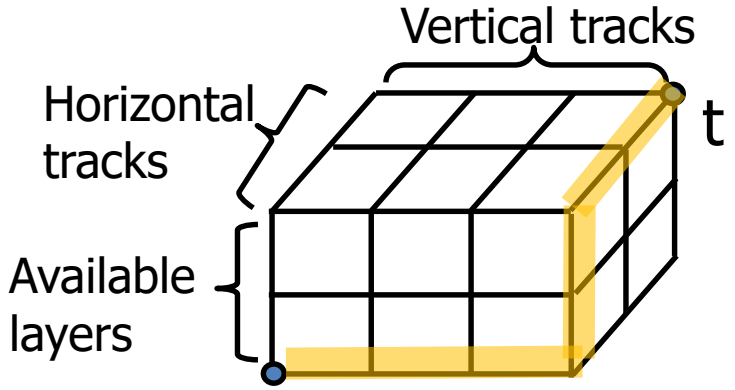
Do We Need Supervia in all layers?

minArea Rule	Utilization with rule imposed on all Layers		Utilization with rule not imposed on M2		Utilization with rule not imposed on M2 and M3	
0x	**0.95** (MIPS)	**0.91** (AES)	**0.95** ((MIPS)	**0.91** (AES)	**0.95** (MIPS)	**0.91** (AES)
3x	**0.89** (MIPS)	**0.85** (AES)	**0.93** (MIPS)	**0.88** (AES)	**0.95** (MIPS)	**0.9** (AES)
5x	**0.86** (MIPS)	**0.78** (AES)	**0.91** (MIPS)	**0.88** (AES)	**0.94** (MIPS)	**0.9** (AES)

- **MinArea rule primarily impacts M2 and M3 congestion.**
- Supervia between M1 & M3 and M2 & M4 gives most benefit

Optimal ILP-based Detail Router [HanKL'15]

- Routing resources ⇒ A 3D-mesh graph
  - Horizontal and vertical tracks
- Metal layers
- A routed net = a set of edges
- Pin shape



- **Objective:** Find an optimal routing for a given set of nets under design rule constraints
- **Subject to**
  - Unidirectional routing
  - Via shape
  - **Minimum area rule (new constraint)**
  - **End-of-line extension (new constraint)**
  - **Super via (new constraint)**

[HanKL15] K. Han, A. B. Kahng and H. Lee, "Evaluation of BEOL Design Rule Impacts Using an Optimal ILP-Based Detailed Router", *Proc. ACM/IEEE Design Automation Conf.*, 2015..

Optimal ILP-based Detail Router [HanKL'15]

Objective

c: cost, e: edge, f: flow

$$\min \sum_{nets\ k} \sum_{edges\ (i,j)} c^k{}_{ij}\, e^k{}_{ij} \longrightarrow \text{Minimize cost}$$

For each net routing

$$\sum_{v_j:(i,j)\in A} f_{ij} - \sum_{v_j:(j,i)\in A} f_{ji} = \begin{cases} \#sinks & if\ j = source \\ -1 & if\ j = sink \\ 0 & otherwise \end{cases}$$

$0 \le f_{ij} \le \#\text{sinks}$ → Flow conservation (= connection)

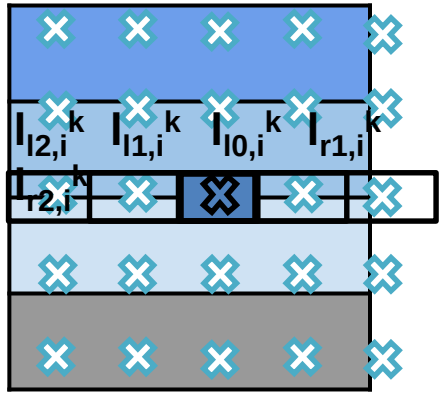
$e_{ij} = 1$ if $\sum f_{ij} \neq 0$ → Edge is taken when there is a flow

Routing constraints

+ more constraints for design rules

New Constraints

- **EOL extension**
  - Create EOL variable **l**, which represent EOL options



- $f_{i,j}^k$ variable represents a flow on via, where $x_j = x_i$, $y_j = y_i$ and $z_j = z_i \pm 1$
- $\mathbf{l_{r2,i}^k + l_{r1,i}^k + l_{r0,i}^k + l_{l0,i}^k + l_{l1,i}^k + l_{l2,i}^k \geq f_{i,j}^k}$

→ **If a via is placed at *i*, one of EOL extension options must be picked**

- **Minimum area rule**
  - Given min area **M,**

- $\sum_{(i,j)\in A'} e^k_{ij} \geq \mathbf{M \cdot l_{r2,i}^k}$

→ If a EOL extension option is picked, sum of corresponding e^k_{ij}, where $(i,j) \in A'$ must be **≥ M**

- **Super-Via**
  - $f_{i,j}^k$, where j = (x_i, y_i z_i – 1) and $f_{i,j'}^k$, where j' = (x_i, y_i, z_i + 1)
  - $\mathbf{l_{r2,i}^k + l_{r1,i}^k + l_{r0,i}^k + l_{l0,i}^k + l_{l1,i}^k + l_{l2,i}^k \geq f_{i,j}^k - f_{i,j'}^k}$

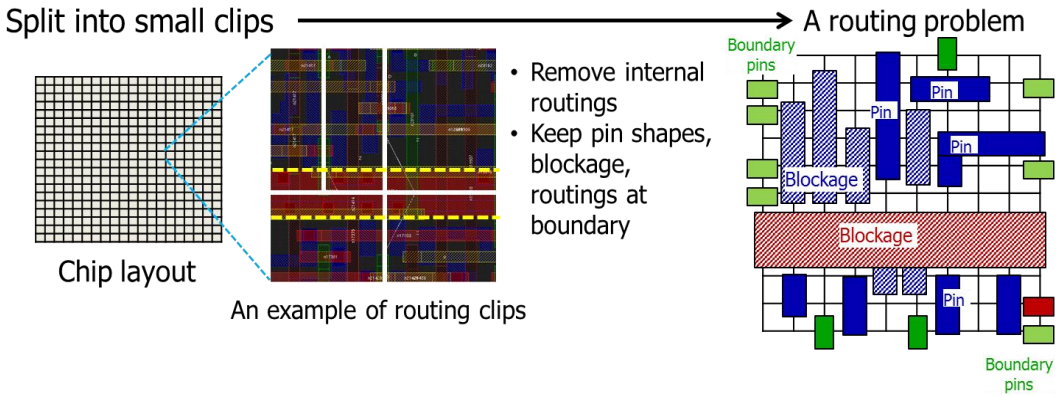
→ **If there are two aligned consecutive vias, min area rule is not applied for intermediate layer**

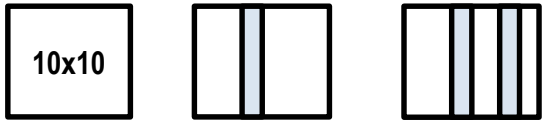
Clip-based Area Cost Estimation

- OptRouter ➞Routability Analysis
  - 3x, 5x min area rules

- Feasibility ➞ Area cost: Count the minimum number of additional routing tracks which makes an infeasible clip feasible
  - Tracks are inserted between the most critical pins

- Initial results with AES, 7nm library
  - Total nine clips are tested; #layers = 5
  - 5x min area rule, **4 out of 9 clips feasible with SV**, **zero clips feasible without SV**
  - Average area benefit of SV = 1.25 tracks





Clip A

Clip B
Clip A + 1 track

Clip C
Clip A + 2 tracks

	# Feasible clips	(%)
3x, SV	9	100%
3x, noSV	9	100%
5x, SV	4	44%
5x, noSV	0	0%
5x, noSV + 1 track	3	33%
5x, noSV + 2 tracks	4	44%

Clip-level Evaluation Results

TABLE V: Routing completion rate results.

Testcase	3x		5x		7x	
	non-SV	SV	non-SV	SV	non-SV	SV
MIPS_4	100%	100%	87%	97%	57%	88%
MIPS_5	100%	100%	87%	96%	50%	77%
AES_5	100%	100%	85%	95%	29%	50%
AES_6	100%	100%	77%	90%	34%	71%
M0_4	100%	100%	99%	100%	71%	87%
M0_5	99%	99%	87%	99%	39%	70%
M0_6	99%	99%	46%	79%	40%	74%

- *OptRouterSV* is run on 100 clips for each test case.
- For minArea= 3x, all designs show close to 100% routing completion rate for both SV and non-SV cases.
- For MinArea = 5x, we observe 77% ~ 99% completion rates.
- There is no need for supervias in the MinArea = 3x case though need for routers to handle minimum area rule efficiently is exhibited.
- Dramatic improvement in Routability when 5x or 7x rules are used.

Supervia-Aware Chip-Level Legalizer

- Perturb metal polygons of the initial MinArea 1x DRC clean layout to enforce nX MinArea rule on non-stacked vias.

Objective

$$minimize \sum_i |l_i - l_i^{orig}| + |r_i - r_i^{orig}| + \lambda * \sum_i S_i$$

Minimize Perturbation while fixing design rules

Design Rule Constraints

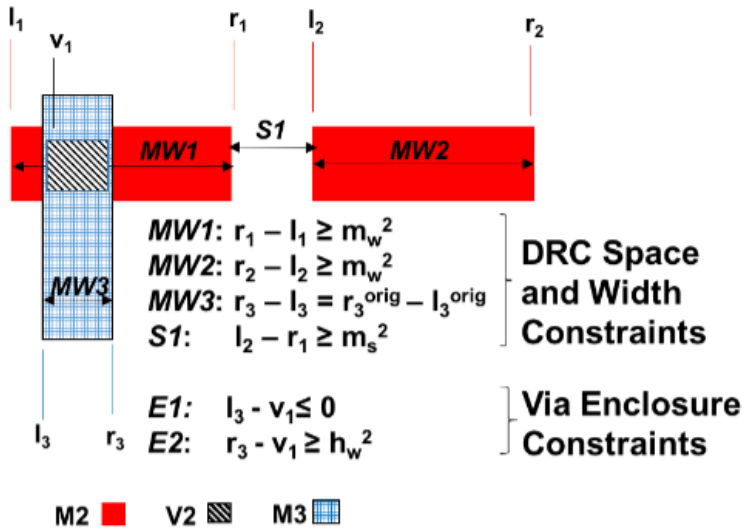
$$l_i - r_{i'} \geq m_s^{\gamma} \qquad \forall (w_i, w_{i'}), \gamma \in \Gamma$$
$$r_i - l_i \geq m_w^{\gamma} \qquad \forall \gamma \in \Gamma$$

The enforced design rules are minimum width and minimum space on metal layers.

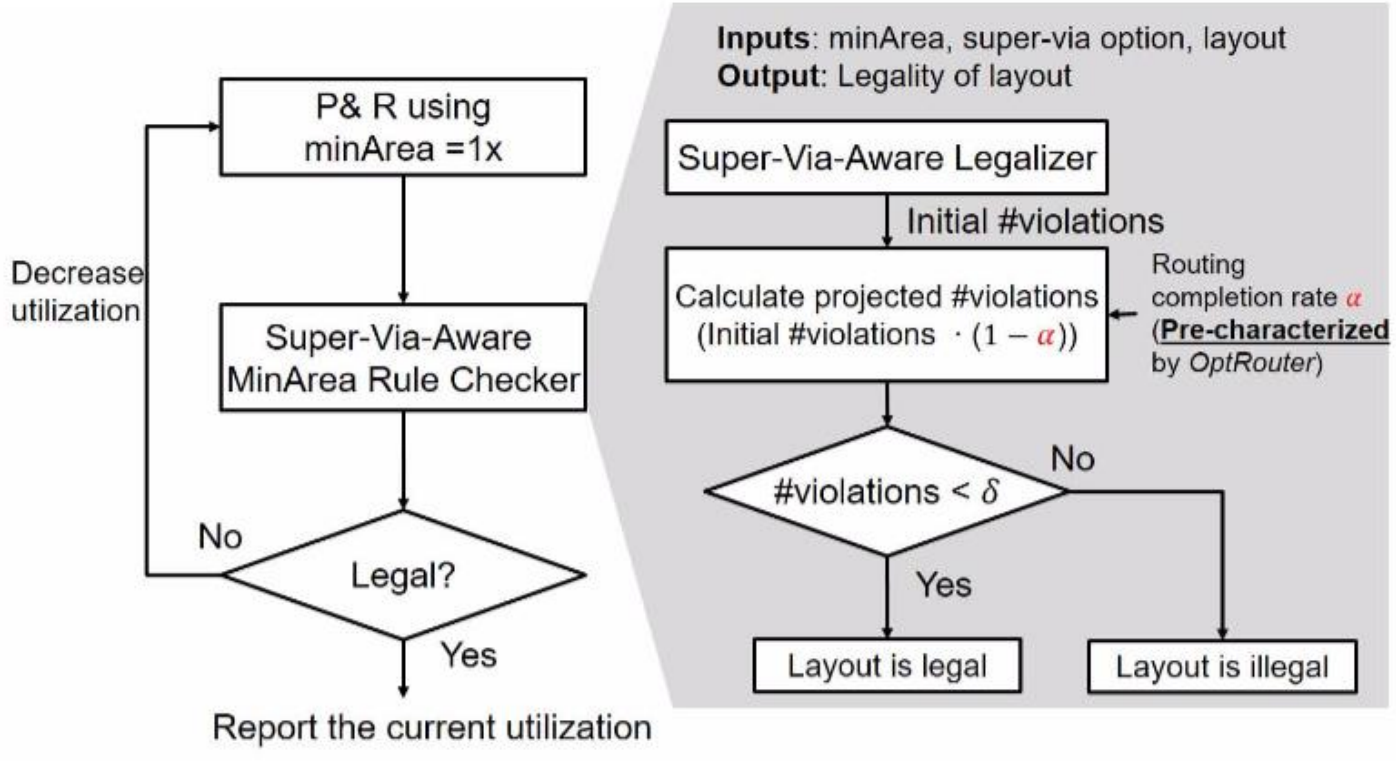
MinArea and Supervia Constraints

$$b_{j,j'} = 0 \implies r_i - l_i + S_i \geq m_l^{\gamma} \quad \forall w_i | w_i = land(v_j, v_j')$$
$$r_i - l_i + S_i \geq m_l^{\gamma} \qquad \forall w_i \in Q$$

MinArea is enforced for all polygons except stacked vias, those are treated as supervias



Chip-level Evaluation Flow



For Experiments using *Cadence Encounter v11.10*, we use the evaluation flow shown here.

For Experiments using *Cadence Innovus v 16.10*, we don't project the violations rather report the number of violations after the legalization step.

Chip-level Evaluation Results

Using *Cadence Encounter v11.10*

minArea	Testcase	supervia				Non-supervia			
		Util	#VioL	α	#VioP	Util	#VioL	α	#VioP
3x	AES_5	92%	0	1	0	92%	2074	1	0
5x	AES_5	92%	122	0.95	7	92%	2827	0.85	425
5x	AES_5	87%	123	0.95	7	87%	2714	0.85	408
5x	AES_5	83%	117	0.95	6	83%	2514	0.85	378
7x	AES_5	92%	1725	0.50	862.5	92%	5814	0.29	4128
7x	AES_5	87%	1582	0.50	791	87%	5329	0.29	3784
7x	AES_5	83%	1328	0.50	664	83%	5179	0.29	3678
3x	MIPS_4	96%	0	1	0	96%	1360	1	0
5x	MIPS_4	95%	61	0.96	3	95%	1719	0.87	224
5x	MIPS_4	91%	60	0.96	3	91%	1663	0.87	217
5x	MIPS_4	88%	64	0.96	3	88%	1649	0.87	215
5x	MIPS_4	83%	52	0.96	3	83%	1527	0.87	199
7x	MIPS_4	95%	856	0.77	197	95%	3223	0.50	1612
7x	MIPS_4	90%	729	0.77	168	90%	3076	0.50	1538
7x	MIPS_4	86%	758	0.77	175	86%	3014	0.50	1507
7x	MIPS_4	70%	427	0.77	99	70%	2576	0.50	1288
7x	MIPS_4	50%	410	0.77	95	50%	2162	0.50	1081
3x	M0_5	84%	0	1	0	84%	911	1	0
5x	M0_5	84%	55	0.99	1	84%	2102	0.87	274
5x	M0_5	78%	66	0.99	1	78%	1946	0.87	256
5x	M0_5	73%	55	0.99	1	73%	1743	0.87	227
5x	M0_5	60%	52	0.99	1	60%	1486	0.87	194
7x	M0_5	84%	963	0.71	278	84%	3906	0.41	2305
7x	M0_5	78%	887	0.71	258	78%	3672	0.41	2167
7x	M0_5	73%	782	0.71	227	73%	3280	0.41	1936
7x	M0_5	60%	642	0.71	186.6	60%	2766	0.41	187
7x	M0_5	50%	623	0.71	181.6	50%	2673	0.41	1578

Results of Supervia-aware chip-level evaluation flow. VioL denotes # violations after legalization, VioP denotes projected #violations

Testcase	minArea	Supervia		Non-supervia	
		Threshold1	Threshold2	Threshold1	Threshold2
AES_5	3x	92%	92%	92%	92%
AES_5	5x	92%	92%	79%*	79%*
AES_5	7x	<50%	70%	<50%	<50%
MIPS_4	3x	96%	96%	96%	96%
MIPS_4	5x	96%	96%	83%	96%
MIPS_4	7x	96%	96%	<50%	<50%
M0_5	3x	84%	84%	84%	84%
M0_5	5x	84%	84%	68%*	84%
M0_5	7x	60%	84%	<50%	<50%

Projected Utilization Improvements with supervia, Threshold1 = 200 violations; Threshold2 = 500 violations

Chip-level Evaluation Results

Using *Cadence Innovus v16.10 and Supervia aware Legalizer*

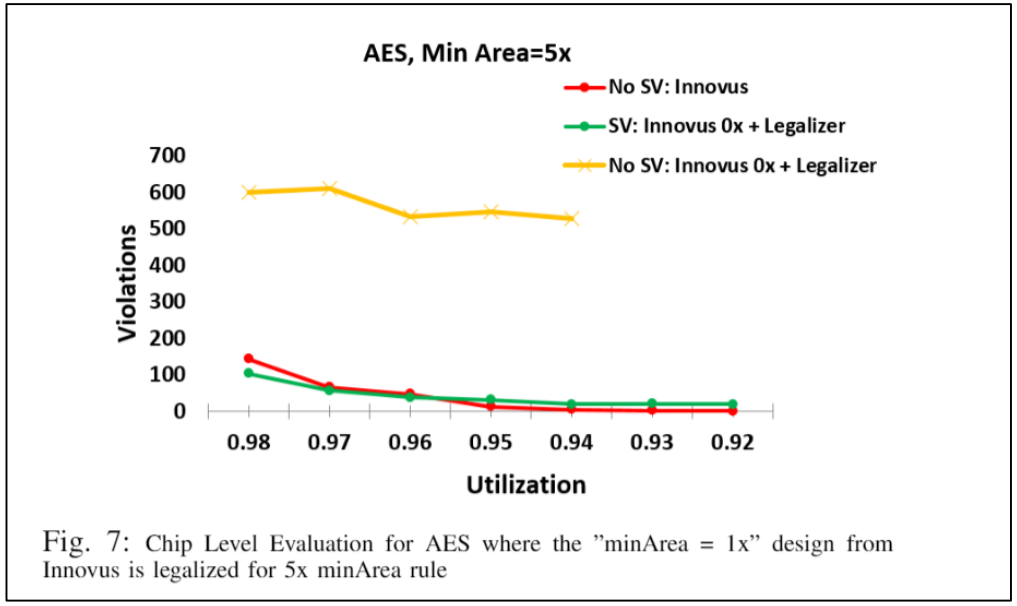


Fig. 7: Chip Level Evaluation for AES where the "minArea = 1x" design from Innovus is legalized for 5x minArea rule

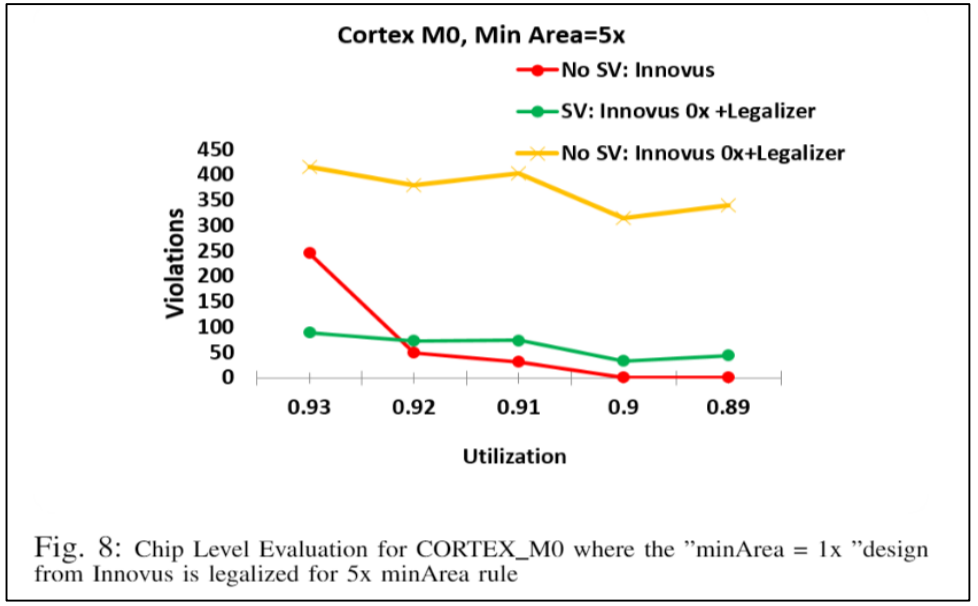


Fig. 8: Chip Level Evaluation for CORTEX_M0 where the "minArea = 1x "design from Innovus is legalized for 5x minArea rule

- Supervia aware legalization results in lower number of DRC violations than Innovus 5X only for a very small span of utilization
- About 2% density benefit can be achieved using Supervia for CORTEX_M0

Conclusions

- Super-Via showed benefit in the following cases
  - Highly congested routing areas
  - Clips with large number of vias
  - Large value of minimum area rule (E.g. 5x+)

- In the average designs, recent P&R tools can handle minimum area rule reasonably well
  - Benefit of Super-Via is not dramatic in digital logic chips

- In case of highly congested designs→ Super-Via-aware routers will be needed
  - Post-PR legalization not enough
  - Optimal Router required

Possible Applications of Interest

- **STT-RAM** based memory cell design where the memory cells are placed in the BEOL stack and Supervia can be used to provide access connection directly from the FEOL contact layer to the logic cells *[imec17]*

- Supervia reduces one barrier layer in a double height via stack. Thus, it decreases overall via resistance.

On-chip power distribution network is a potential application, since reduced via width is resulting in increased resistance in advanced technology nodes.

*[**imec17**]* Appeltans, Raf et.al. “The effect of patterning options on embedded memory cells in logic technologies at iN10 and iN7”, Proc. SPIE, 2017, pp. 101480G-101480G-13