O(n) Layout-Coloring for Multiple-Patterning Lithography and Conflict-Removal Using Compaction

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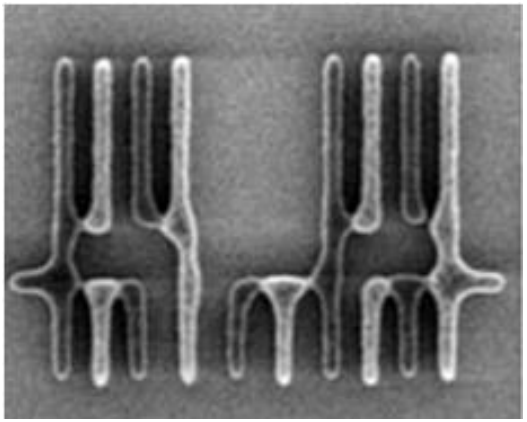
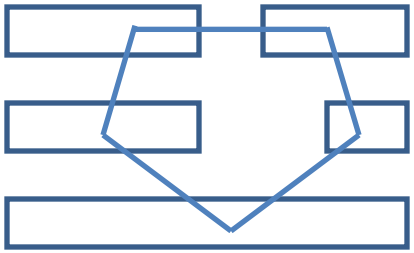
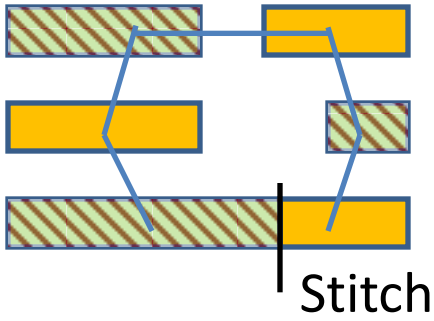
Multiple-Patterning Lithography

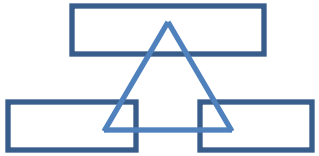


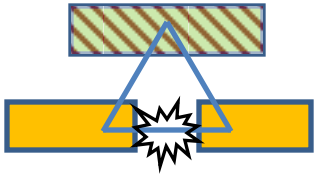
C. Mack, IEEE Spectrum 08





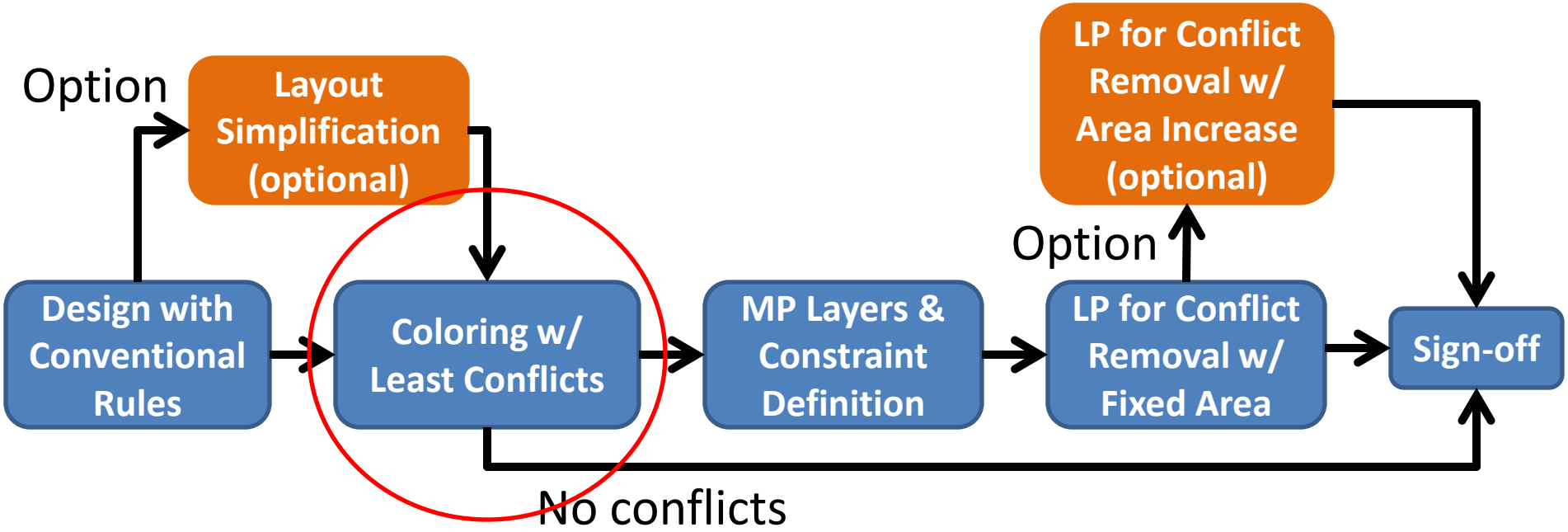
Native conflict → needs layout change





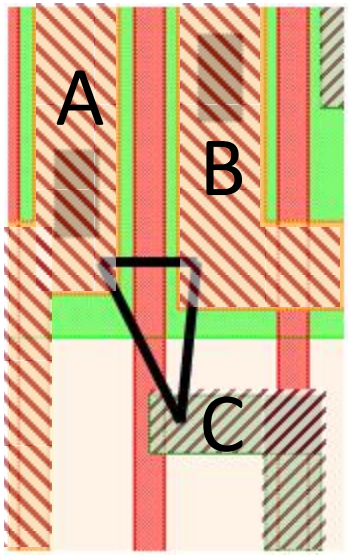
- Delays in EUV → MP is inevitable for sub 20nm tech
  - DP/TP in LELE, SADP
- Biggest challenge is coloring conflicts
- E.g., DP in LELE process

Overview of the Framework

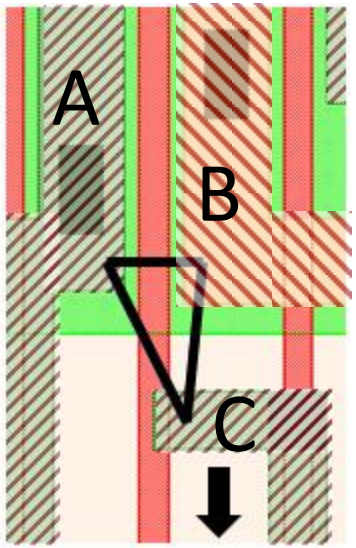


- Fast linear time coloring
- LP-based compaction for conflict removal
  - Simultaneously fixes all conflicts without creating new conflicts

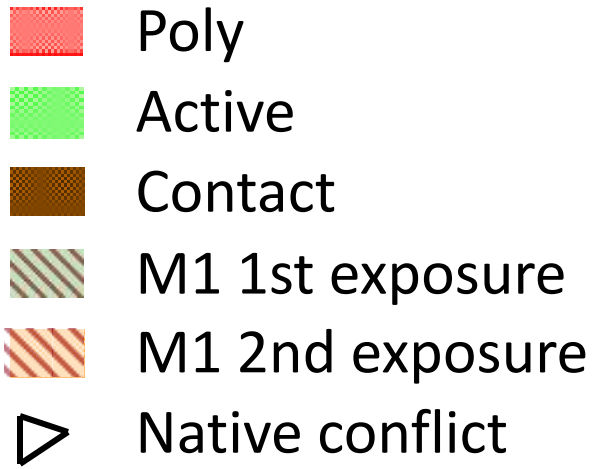
Preferred Coloring



Bad coloring



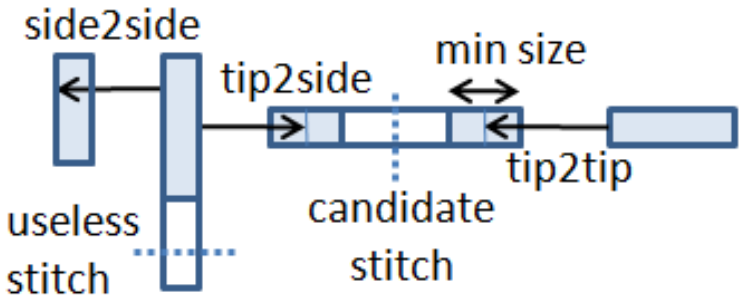
Good coloring



- Coloring of native conflicts affects efficiency of conflict removal
- Give preference for opposite coloring for certain violations over others → label violations critical vs. less-critical
  - E.g., horizontal spacing violation more critical than vertical or diagonal in case of vertical poly orientation

O(n) Coloring

Projection

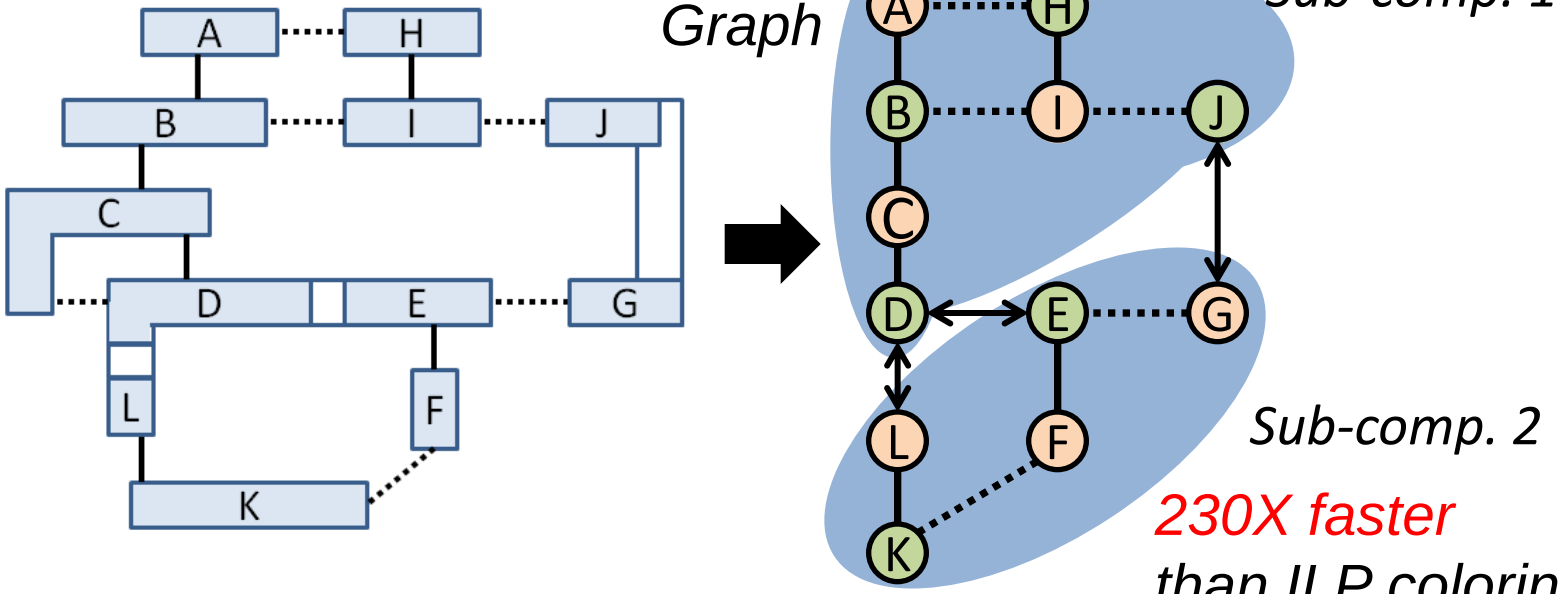


Violating → coloring matters

Non-violating → coloring doesn't

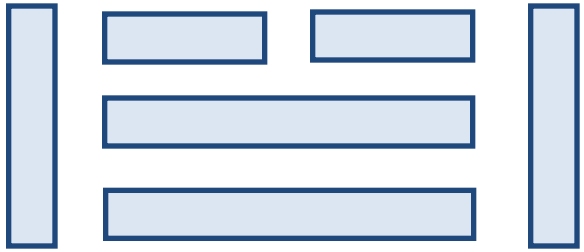
Stitches → non-viol b/w violating

Conflict Graph



230X faster than ILP coloring

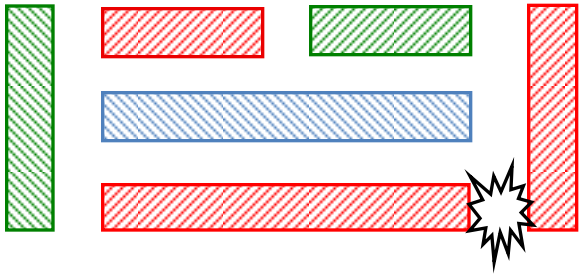
Triple Patterning – Extending 2-Coloring to 3-Coloring



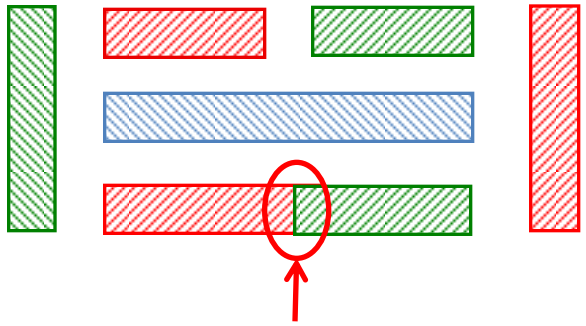
Projection → all parts violating → no stitches

No 3-Coloring Solution!

Valid coloring not possible



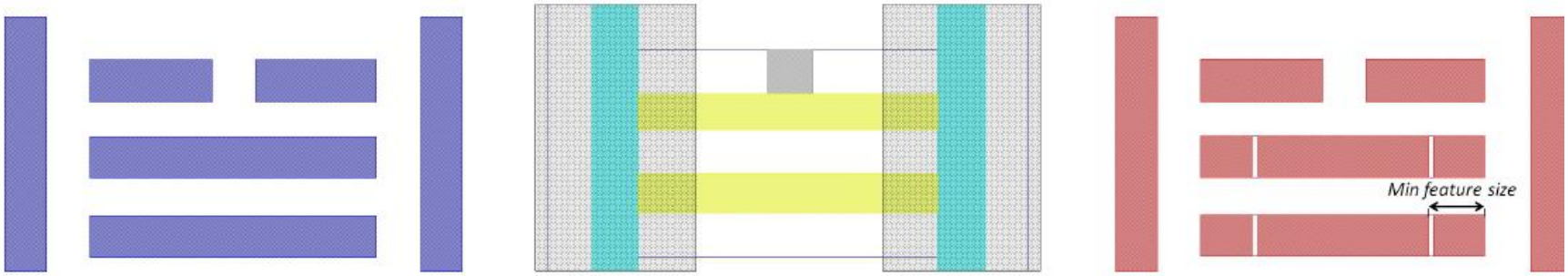
Valid coloring with TP stitch



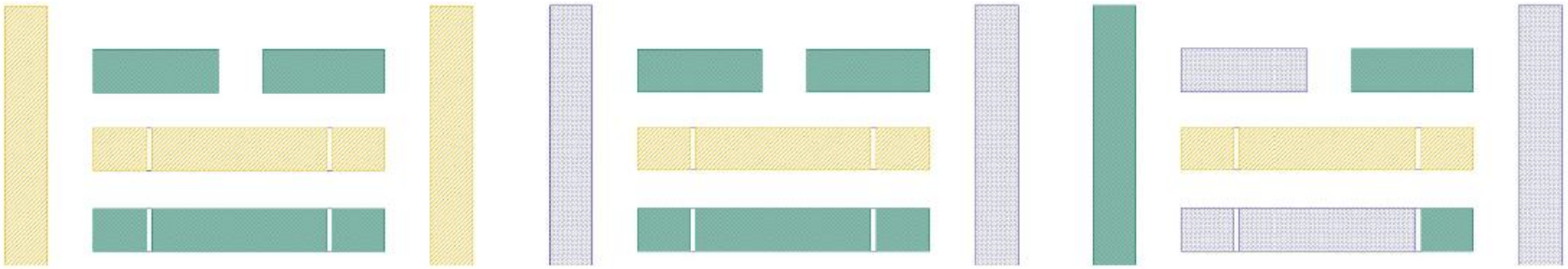
Unseen candidate stitch

- Common 2-coloring cannot be extended to 3-coloring
  - *3-coloring stitches can be almost anywhere!*

TP Coloring Example



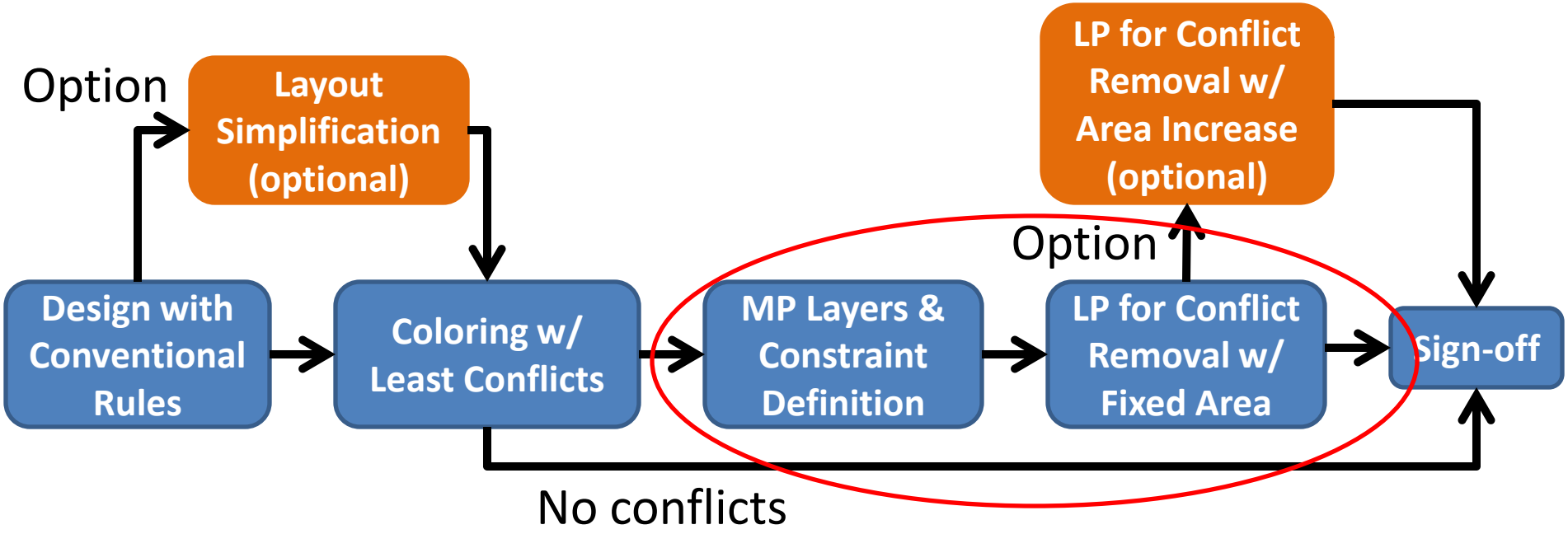
(a): Layout (b): Projection (c): Violating parts



(d): C0/C1 coloring (e): C0/C2 coloring (f): C1/C2 coloring

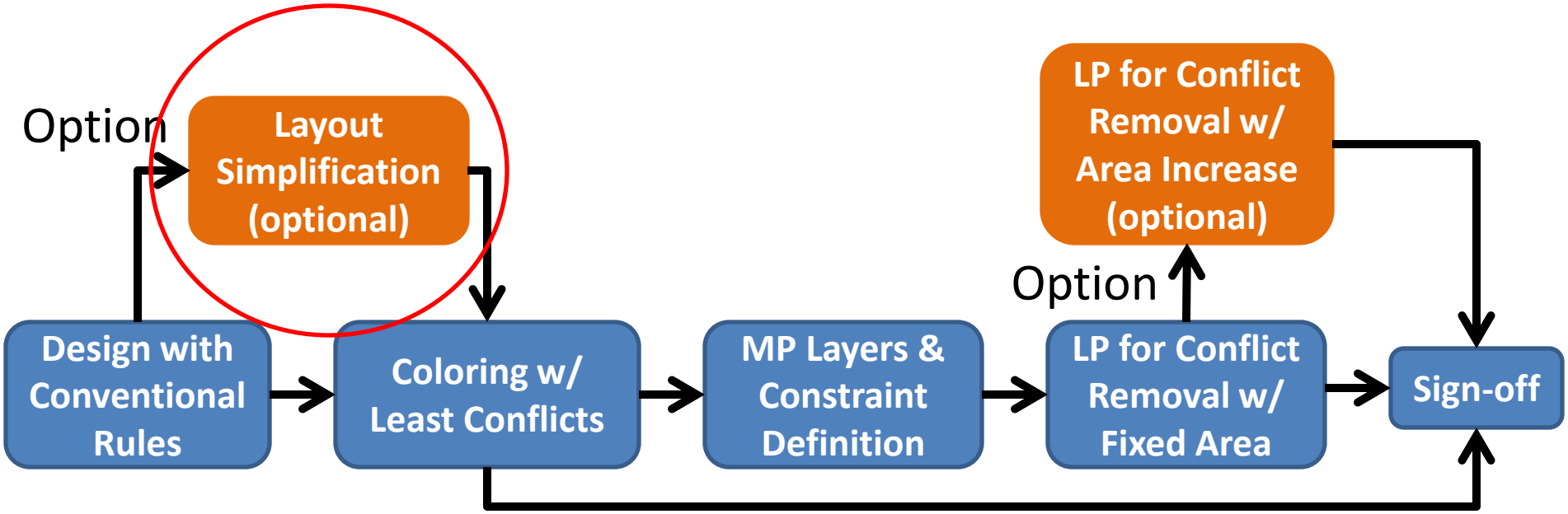
- Leverage TP Stitch Capability → Stitch at S2S violating parts
- Color violating parts w/ C0/C1-C0/C2-C1/C2 coloring cycle
  - Use existing infrastructure of DP coloring
- Works well but not for complex layouts → simplifications needed

Conflict-Removal Using Compaction

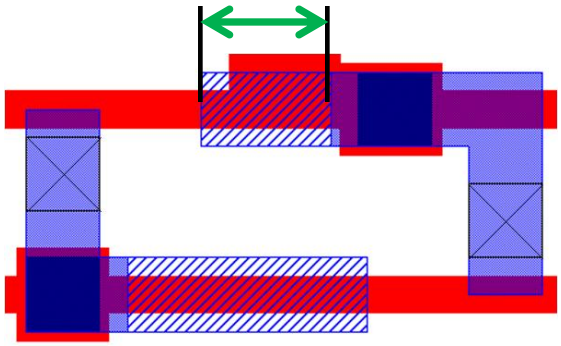


- Color → define DRs between DP layers (e.g., M1A/M1B)
  - Same-color spacing, ≠ color spacing, M1A/M1B overlap
  - Overhang rules with top/bottom layers (union M1A M1B)
- Compaction → Full legalization across all layers concurrently

Sacrificing Unnecessary Layout Features

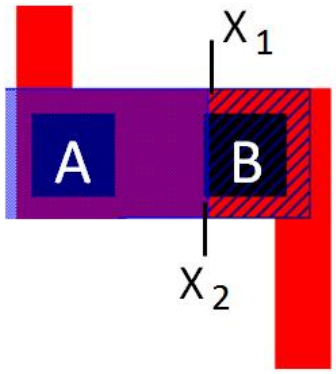


Recommended rule



Pin Segments

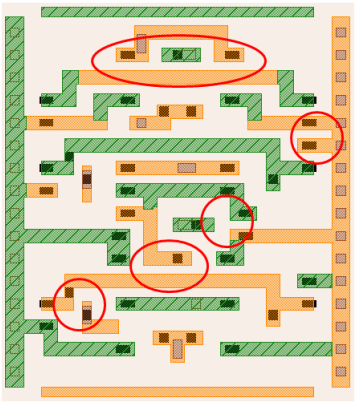
No conflicts



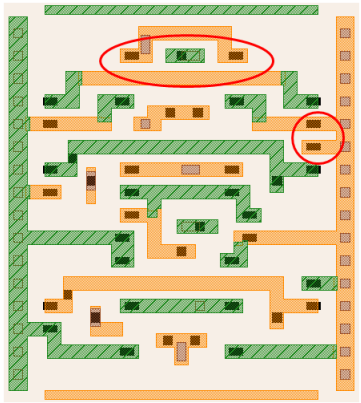
Redundant Contacts

Poly
New M1
Removed M1
Via 1
X_1 New M1 edge x location
X_2 Contact edge x location

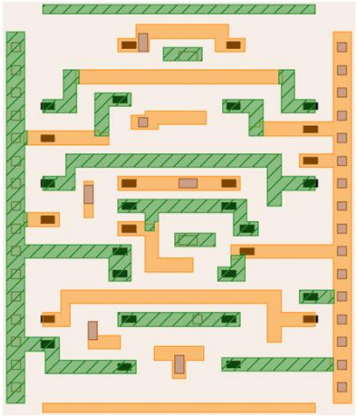
Conflict Removal Results



Original
5 conflicts



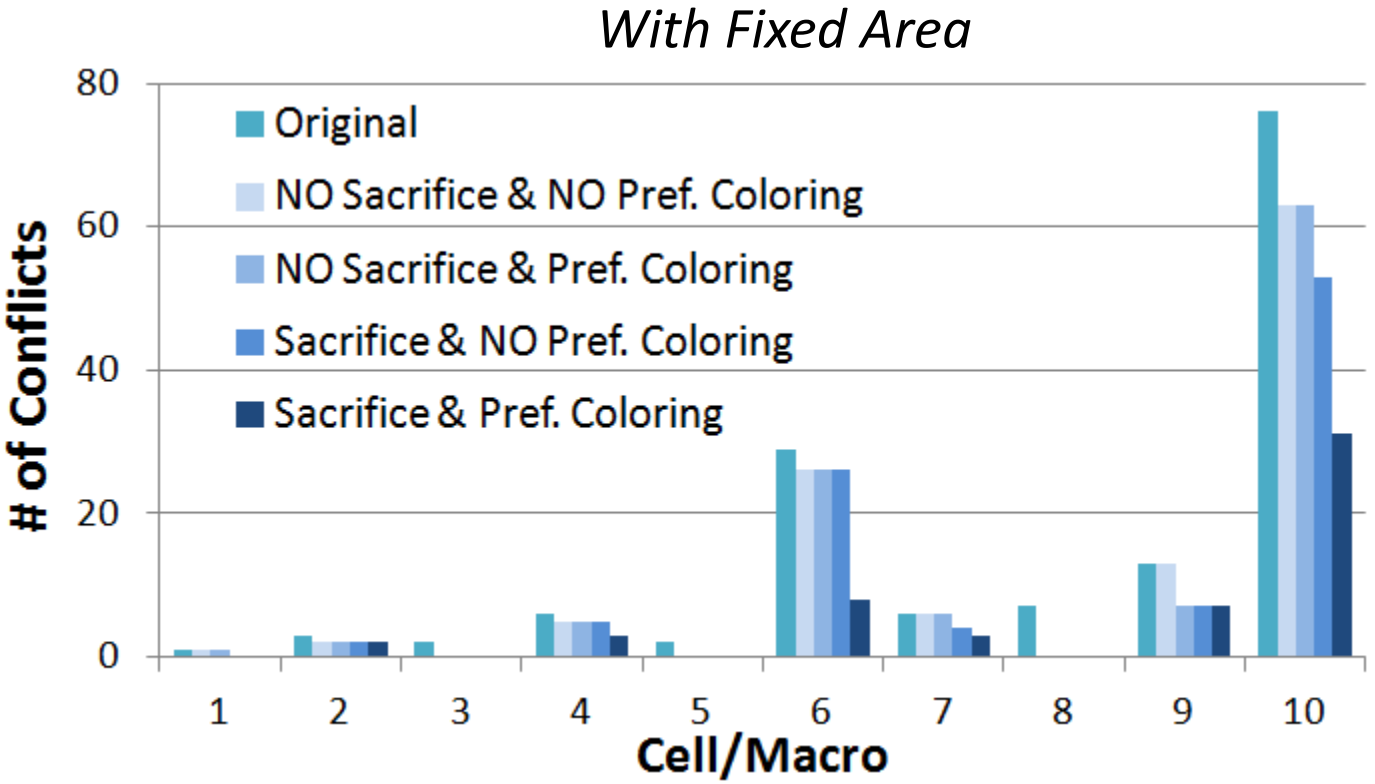
Same area,
2 conflicts



No conflicts, 6.2% area increase

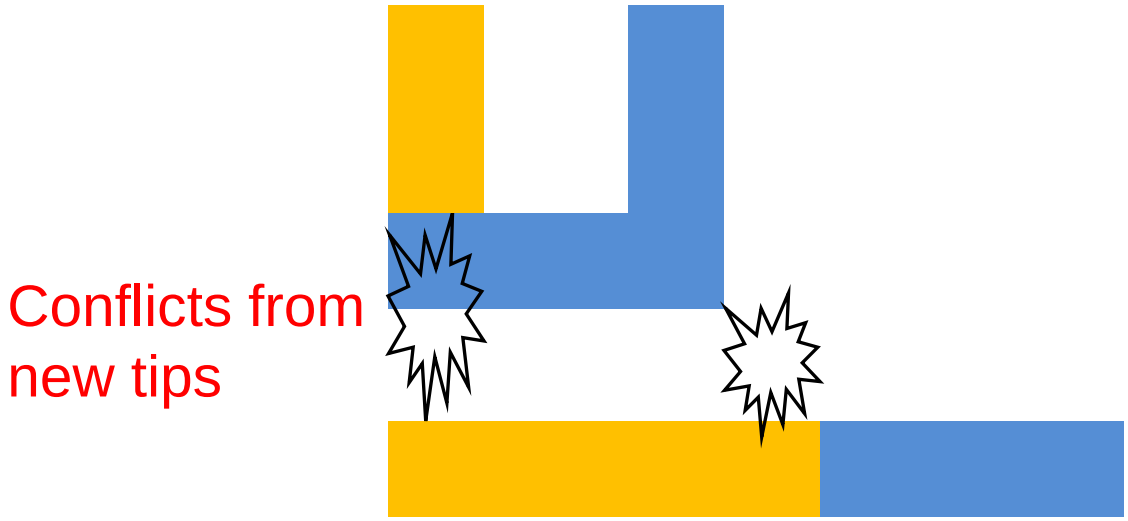
- DP-compatible cells
  - No area overhead for simple cells
  - Modest area overhead (at most 9%) for complex cells and macros
  - Few sacrificed redundant contacts (CA)
- Less than 1 min in real time for largest macro (460 trans.)

Effects of Sacrifice and Preferred Coloring



- Need both enhancement methods
- If enhancements not applied → 2X more conflicts in final layout

Final Notes



- Problems with Newly Created Tips
  - One way → use pessimistic projection → non-optimal
  - Less of a problem when using compaction-based legalization
- Methodology applicable for SADP, only need
  - A layout-coloring method
  - A set of design rules for SADP-compatible layout

Thank you

Questions during poster session