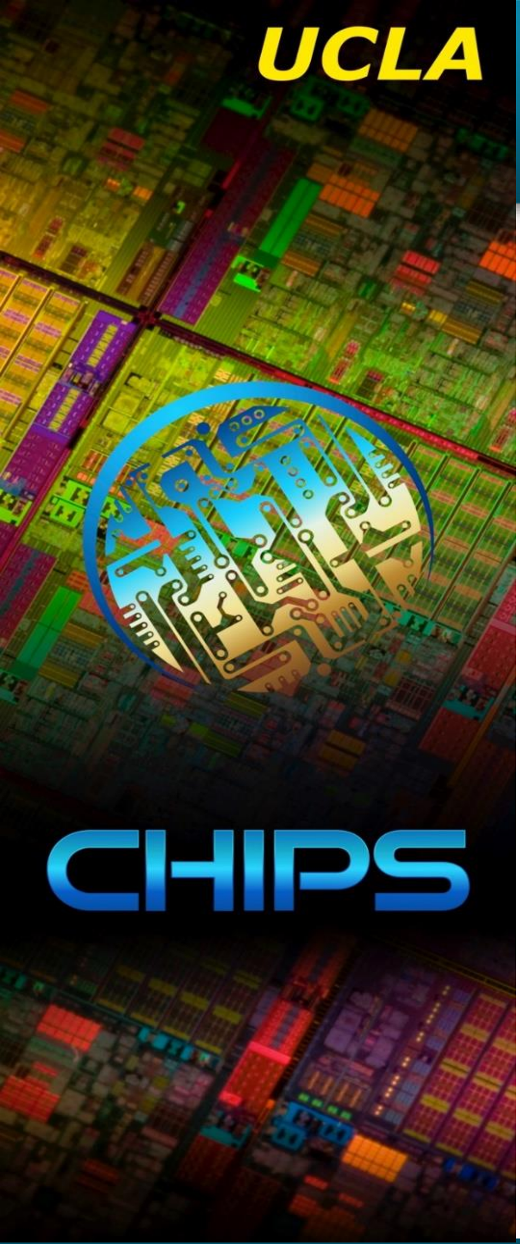

Latency, Bandwidth and Power Benefits of the **S**imple **U**niversal **P**arallel int**ER**face (SuperCHIPS) Integration Scheme

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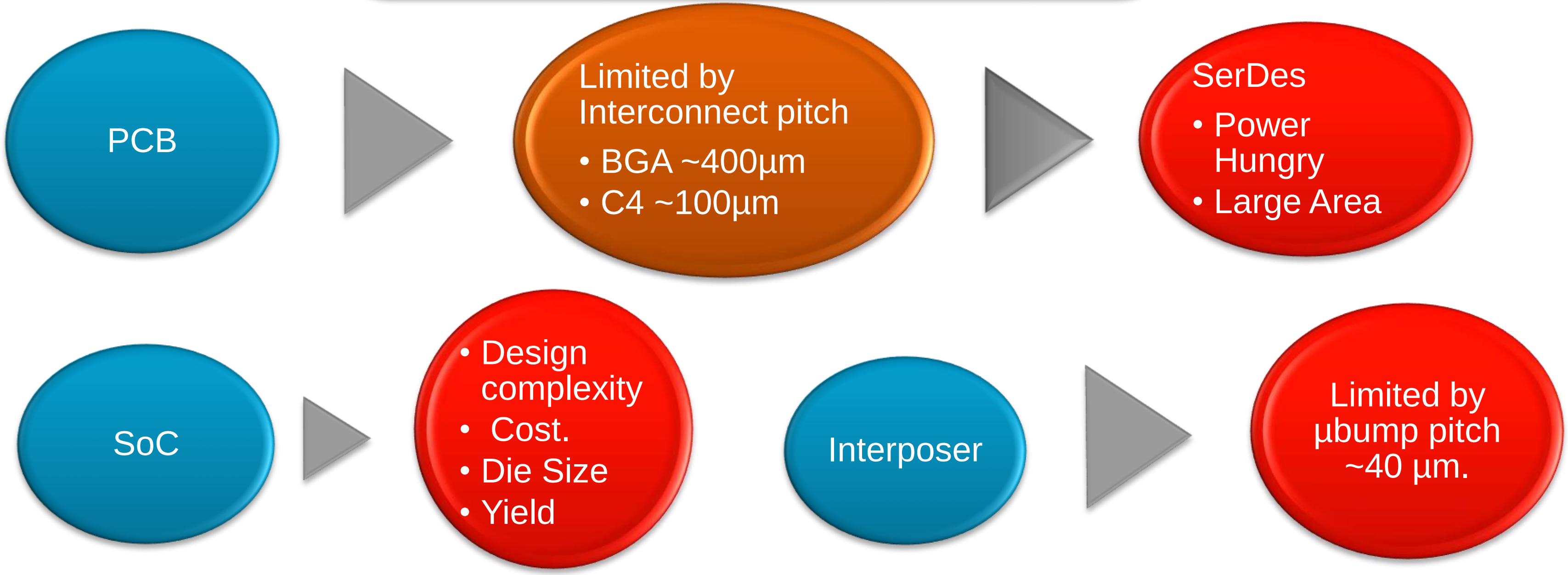
Outline

- Motivation
- **S**imple **U**niversal **P**arallel int**ER**face (SuperCHIPS) Protocol
  - SuperCHIPS Fine Pitch Interconnect (FPI) Scheme
  - **Si**licon **I**nterconnect **F**abric (Si-IF)
- Interconnect Modelling
  - PCB vs Si-IF links
  - Superior Transfer Characteristics for High Speed Data Transfer
  - Signal Integrity Analysis
- Benefits of SuperCHIPS protocol
  - Si-IF vs Conventional PCB
- Experimental Results
- Conclusion

Motivation

Today's Bandwidth



PCB

Limited by Interconnect pitch
- BGA ~400µm
- C4 ~100µm

SerDes
- Power Hungry
- Large Area

SoC

- Design complexity
- Cost.
- Die Size
- Yield

Interposer

Limited by µbump pitch ~40 µm.

- High communication Bandwidth & low Power consumption ?
- Fine pitch interconnects operating at lower speed for lower energy per bit and reduced area per channel.

SuperCHIPS Protocol

Direct metal-metal bonding

Fine Pitch Interconnects <10µm
- More Data links

Higher Bandwidth

Eliminate Die level Packaging

Reduce inter-die spacing <100µm

Short wirelength
- Low Channel loss

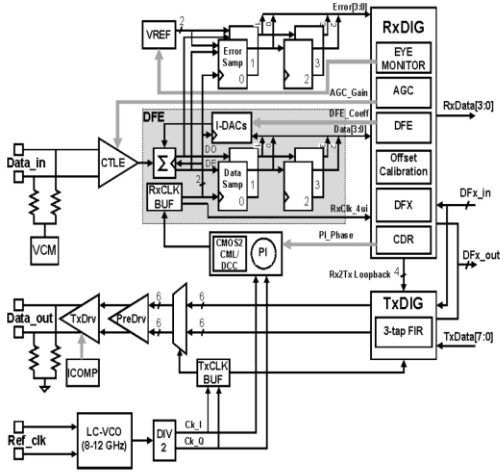
Low Latency

Reduce Driver Complexity
- Reduce Size

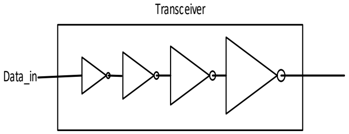
Eliminate SerDes

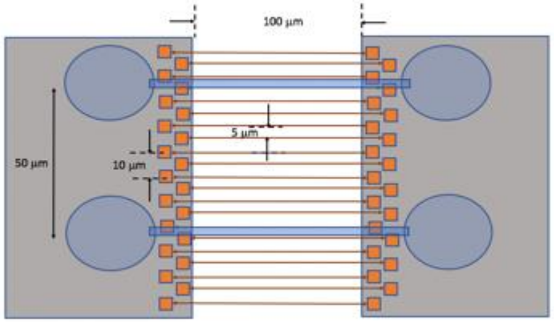
Reduce I/O power

PCB: SerDes



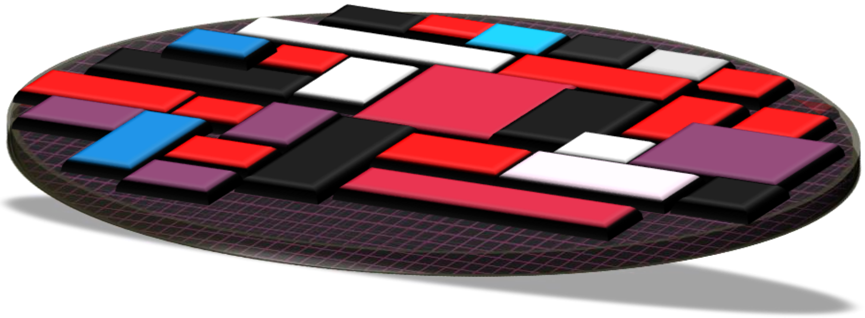
SuperCHIPS: Simple Inverter





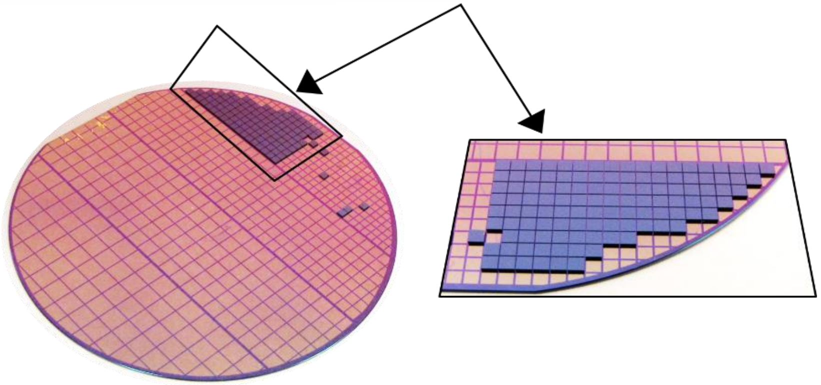
SuperCHIPS Fine Pitch Interconnect (FPI) Scheme

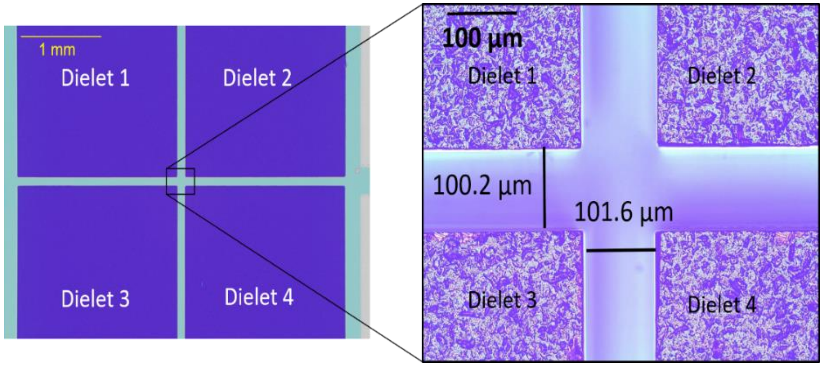
- Die-to-Wafer Bonding
  - Metal-metal Thermal Compression Bonding (TCB)
- SuperCHIPS FPI Scheme
  - Silicon Interconnect Fabric (Si-IF)
  - Small Dielets (0.5 - 5 mm edge length)
  - Fine pitch (2 - 10 µm) interconnects
  - Inter-dielet spacing (50 - 100 µm)



Silicon Interconnect Fabric (Si-IF)

- Thermomechanical Properties
  - Rigid and Mechanically robust substrate.
  - Minimize thermomechanical mismatch.
  - Good heat dissipation.
- Electrical Properties
  - Fine traces: (1 – 5 µm).
  - Fine pitch interconnects: (2 – 10 µm).
  - Up to 4 levels of dual damascene wiring.

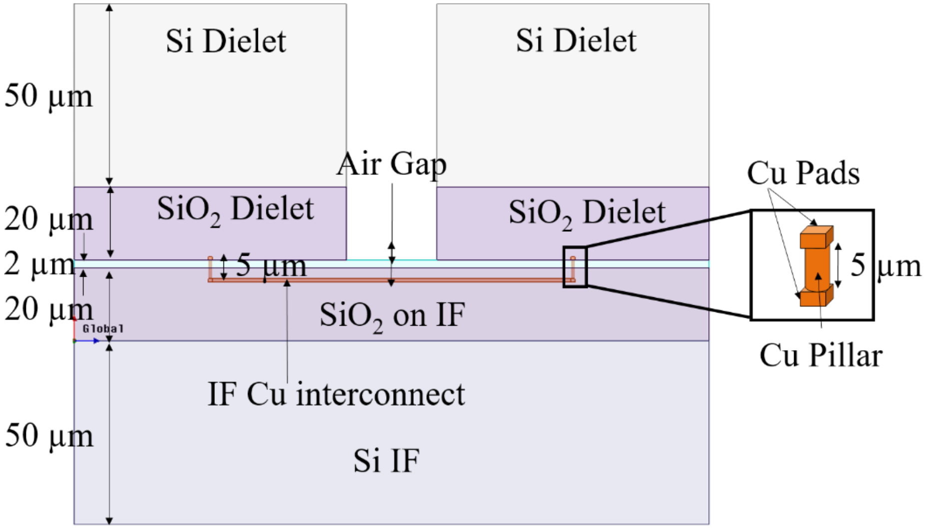




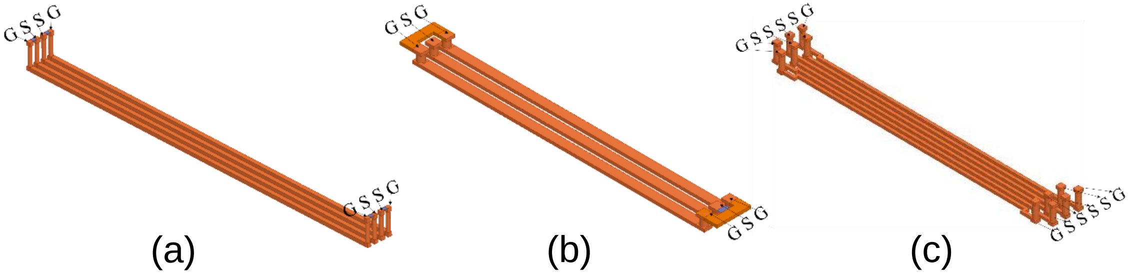
A. A. Bajwa, et.al, “Fine Pitch Die-to-Si Interconnections using Thermal Compression Bonding”, ECTC (2017).
Friday, June 2, 8:00 am. Southern Hemisphere II.

Interconnect Modelling

- 3D interconnect models simulated in ANSYS HFSS.
- BOEL top metal layer dimensions for links
  - 1 µm width, 1.5-10 µm pitch
- Direct Cu-Cu bonding with no intermetallic.
- Different configurations for signal transfer.



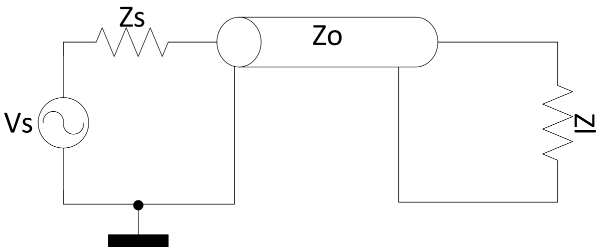
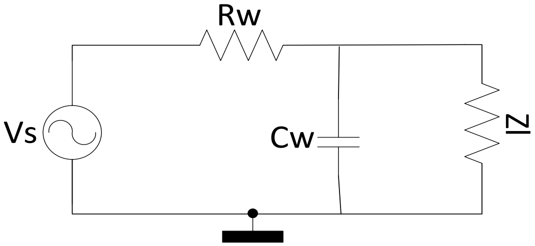
Model to simulate link characteristics



(a) (b) (c)

(a) GSSG config. (b) GSG config. (c) GSSSSG config.

PCB vs Si-IF links

PCB links	Si-IF links
• Long channels (several mm) – High parasitic inductance. – RLC link behavior.	• Short channels (<500 µm) – Low parasitic inductance. – RC link behavior.
• Transmission Line Model – Signal Reflections & Matching 	• RC Line Model – No signal reflections 
• Inter Symbol Interference – Large Transceiver ~0.81mm^2 * – Energy/bit: >23pJ/bit. • Synchronous data transfer	• No Inter Symbol Interference – Simple inverter driver ~0.05µm^2 – Energy/bit: <0.3pJ/bit. • Can be Asynchronous

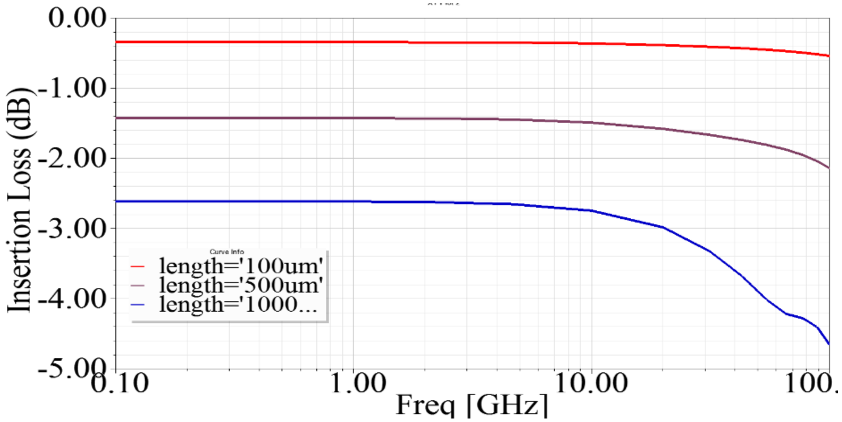
* R. Navid et al., "A 40 Gb/s Serial Link Transceiver in 28 nm CMOS Technology," JSSC 2015.

Reduced Link Parasitics

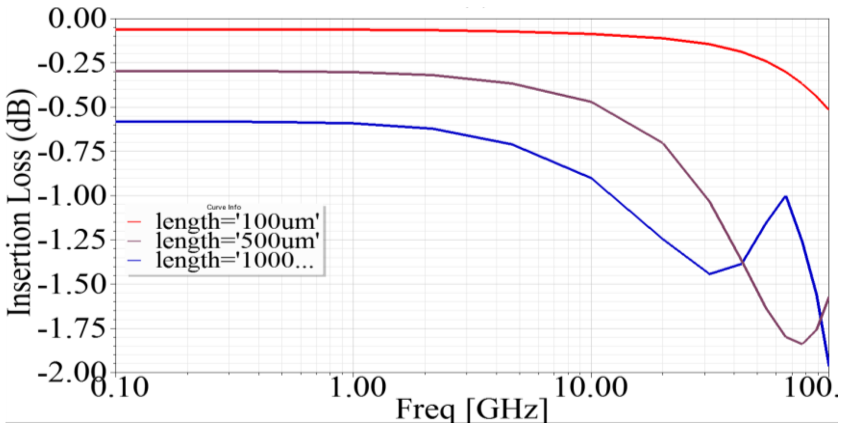
- Ansys Q3D extractor model.
- Low Parasitic Inductance
  - RC link behavior
- Low Parasitic Capacitance
  - Low latency and power.
- Channel loss <-2dB for 500 µm wires even at 100 GHz.

Interconnect pitch/ length	***R @1GHz* (Ω)***	***L (nH)***	***C (fF)***
2 µm/ 100 µm	2.09	0.1	17.3
10 µm/ 100µm	1.89	0.1	8.54

*Accounting for skin depth



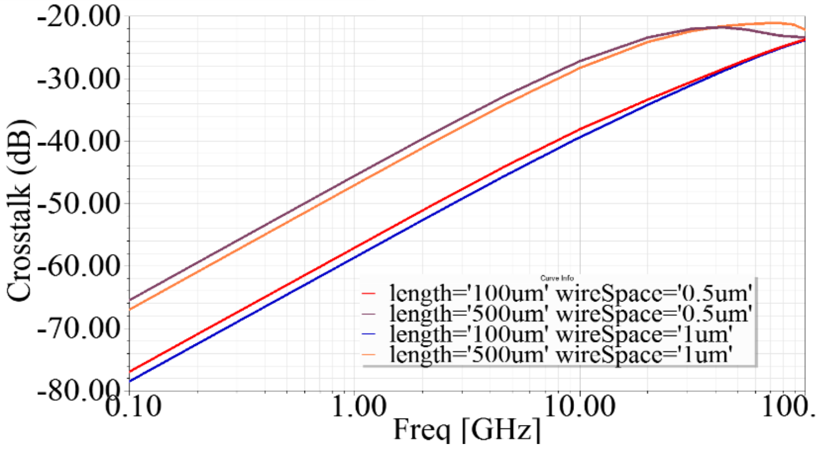
Insertion Loss for 2 µm interconnect pitch.



Insertion Loss for 10 µm interconnect pitch.

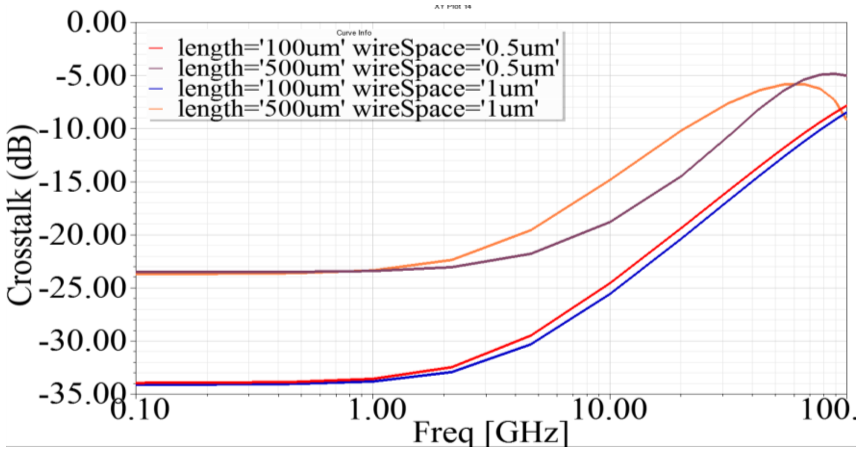
Low Cross-talk

- Excellent dielectric isolation of SiO2.
- Lower Cross-talk than typical acceptable value of -12dB.



NEXT for signals without shared ground

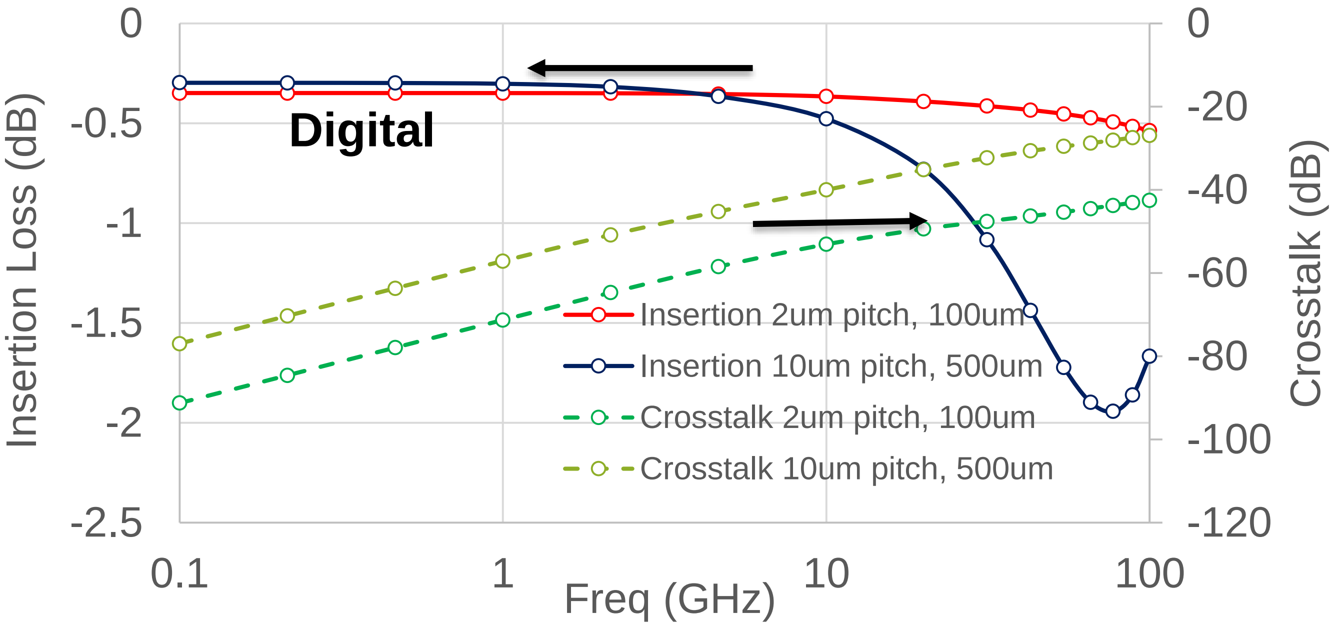
Cross-talk	Without Shared Ground	With Shared Ground @10GHz
Near End Cross-talk (NEXT)	<-20dB	<-15dB
Far End Cross-talk (FEXT)	<-20dB	<-20dB



NEXT for signals with shared ground

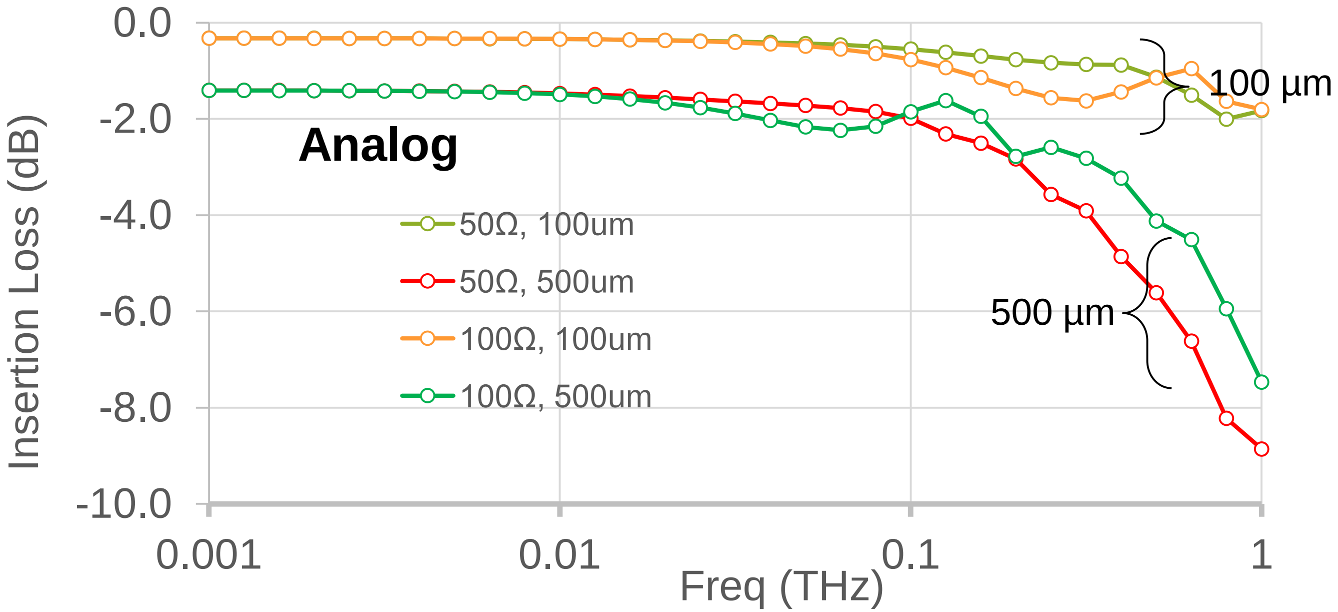
Superior Transfer Characteristics for High Speed Data Transfer

- Digital signals (0.1-100 GHz) transfer with loss <-2dB for short channels (< 500 µm).
- Cross-talk is <-15dB for digital signal transfer.
- Can achieve Data-rates of >20Gbps/channel.



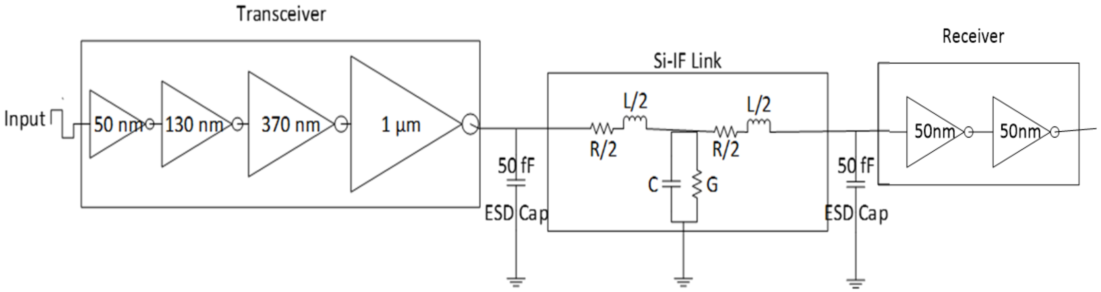
Low Attenuation for THz frequencies

- Short wires of <100 µm.
  - RC behavior. Characteristic Impedance not defined.
  - Attenuation: < 3dB even for THz signals.
- Achievable termination > 100 Ω.

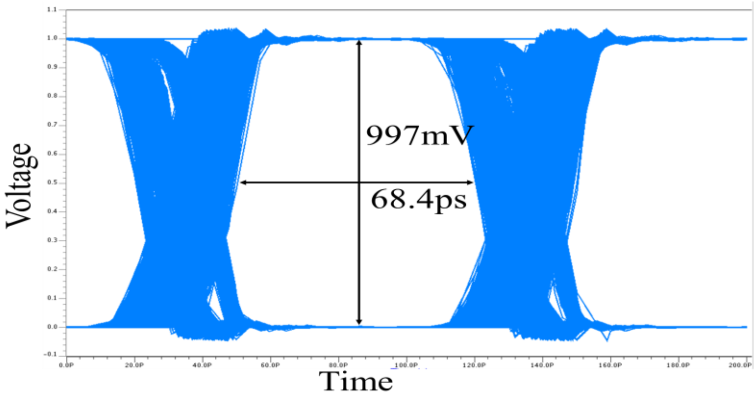


Signal Integrity Analysis

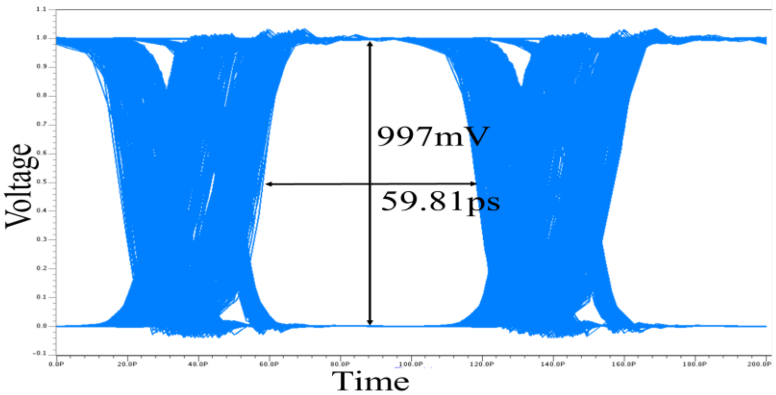
- Simple tapered inverter I/O driver. Eliminate SerDES.
- Latency and power dominated by ESD cap.
- 10GHz signal
  - eye opening: 997mV
  - eye width:
    - 2 µm- 68.4ps
    - 10 µm- 59.81ps



Schematic of circuit use for signal integrity analysis.



Eye-diagram of 2 µm pitch interconnect



Eye-diagram of 10 µm pitch interconnect

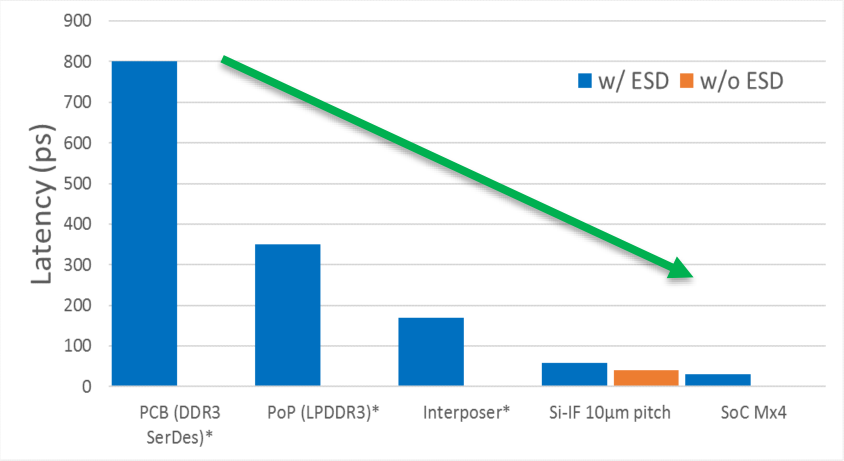
Si-IF vs Conventional PCB

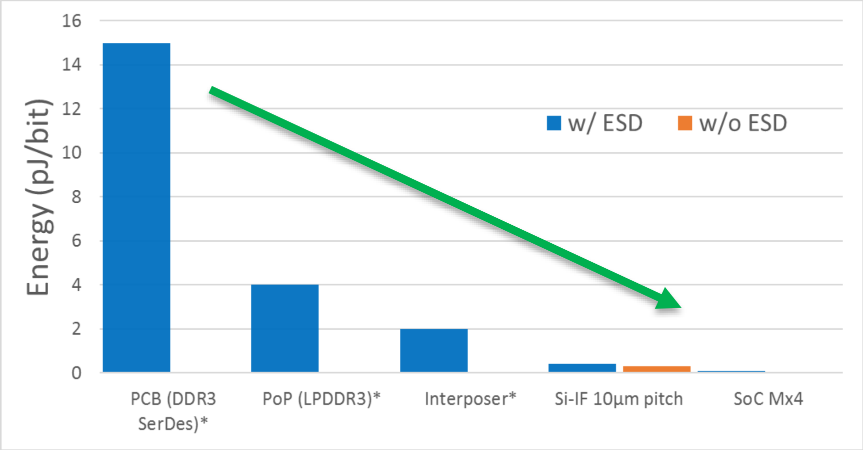
Interconnect pitch/protocol		***10 µm on Si IF Super-CHIPS***	***50 µm on Si Interposer DDR3***	***400 µm on FR4 PCB/ SerDes***
Dielet Size (mm^2)		10-100	25-600	25-625
No of signal links		600-2,000	100-1,000	100-500
Inter-die distance (µm)		<500	<5,000	10,000
Overall Latency (ps)	No ESD	40.22	300[23]	~1,000
	ESD	58.8		
Max data-rate/link (Gbps)	No ESD	13	1.6[24]	40[37]
	ESD	4.21		
Energy per bit (pJ/b)		<0.4	9.48[24]	23.2[37]
Max Bandwidth per mm (Gbps/mm)	No ESD	1,300	32	100
	ESD	421		
Total I/O power (W)		2.13-6.74	6-15	46-230

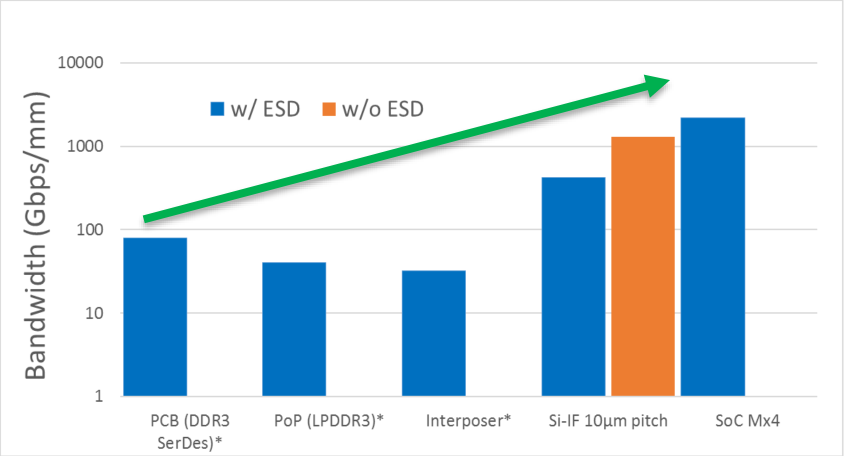
[23] H. Kalargaris, et. al, "Interconnect design tradeoffs for silicon and glass interposers," (NEWCAS), 2014.
[24] M. A. Karim, et. al," Power comparison of 2D, 3D and 2.5D interconnect solutions and power optimization of interposer interconnects" ECTC 2016.
[37] R. Navid et al., "A 40 Gb/s Serial Link Transceiver in 28 nm CMOS Technology," JSSC 2015.

Benefits of SuperCHIPS

- Inter-dielet distance: 10-20x ↓
- I/O pins compared to BGA: 15-80x ↑
- Latency: 13-27x ↓
- Energy per bit: 20-80x ↓
- Bandwidth per mm: 30-120x ↑



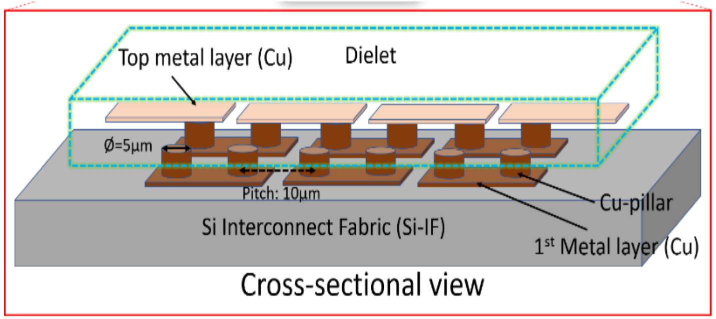


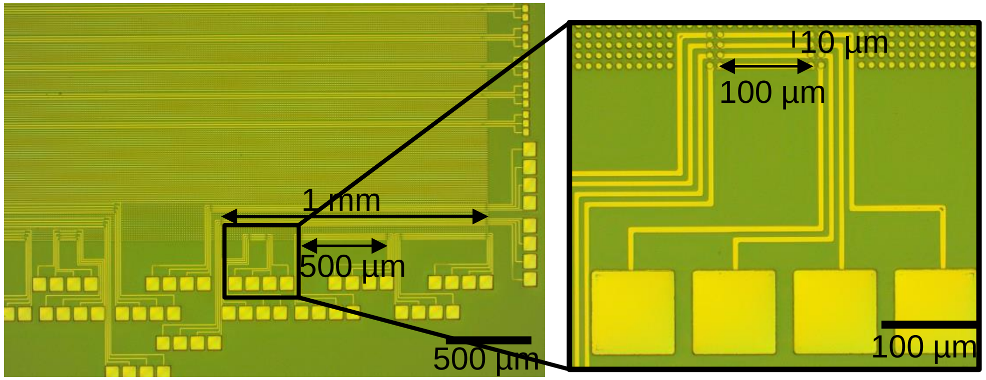


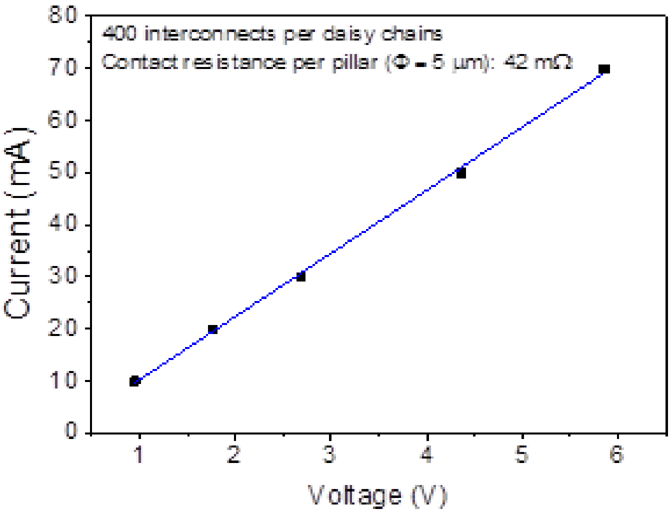
*M. A. Karim, et. al," Power comparison of 2D, 3D and 2.5D interconnect solutions and power optimization of interposer interconnects" ECTC 2016.

Experimental Results

- DC results-
  - Demonstrated continuity with 400 interconnects per daisy chain with 99% yield.
  - Contact resistance: 42 mΩ.
- AC results-
  - High freq measurements in progress.







A.Bajwa,et.al,“Fine Pitch Die-to-Si Interconnections using Thermal Compression Bonding”, ECTC 2017.

Conclusion

- SuperCHIPS protocol shows SoC-like performance with technology heterogeneity and flexibility.
- Channel losses are less than 2dB for digital data transfer of greater than 20Gbps/channel.
- Latencies are 27x smaller compared to PCB.
- Fine Pitch interconnects and shorter channels achieve 120x improvement in Bandwidth per mm.
- 80x Lower power due to elimination of SerDes.
- Reduces cost of design and validation by IP reuse.

Acknowledgement

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- Members of the UCLA CHIPS consortium for their support in this work.

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THANK YOU

Any Questions?

BACK up

The 67th Electronic Components and Technology Conference

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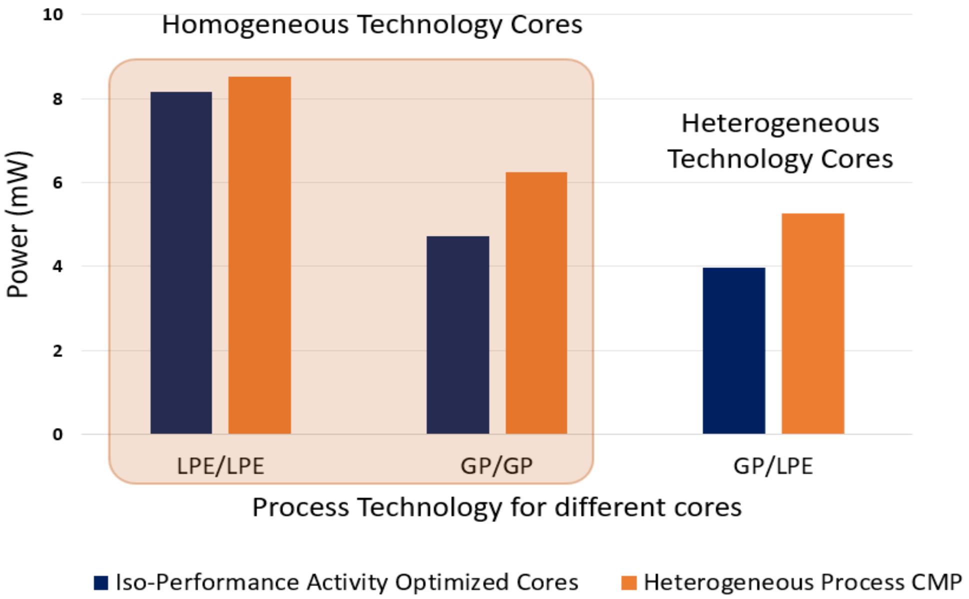
CENTER FOR HETEROGENEOUS INTEGRATION AND PERFORMANCE SCALING

Application of SuperCHIPS to Hexa-core CORTEX M0

- Hexa-core CORTEX M0 architecture.
  - 2 cores for high throughput.
  - 4 cores for higher energy efficiency.
- Monolithic vs Heterogenous technologies
  - 65nm General Purpose (GP): High performance.
  - 65nm Low Power Early (LPE): Energy efficiency.
  - 15% and 37% energy savings.



Design: CortexM0	***Power in mW***		
Activity Factor	***0.001***	***0.01***	***0.1***
GP+GP: nominal/nominal	0.262	0.526	3.8
GP+LPE: nominal/nominal	0.174	0.546	7.44
LPE+LPE: nominal/nominal	0.086	0.564	11.8