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Mask Assignment and Synthesis of DSA-MP Hybrid Lithography for sub-7nm Contacts/Vias

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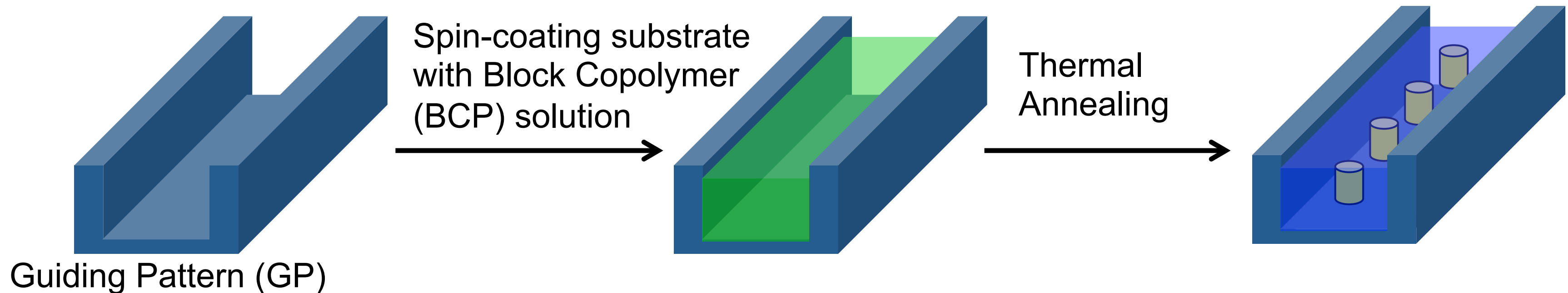
http://impact.ee.ucla.edu

Motivation

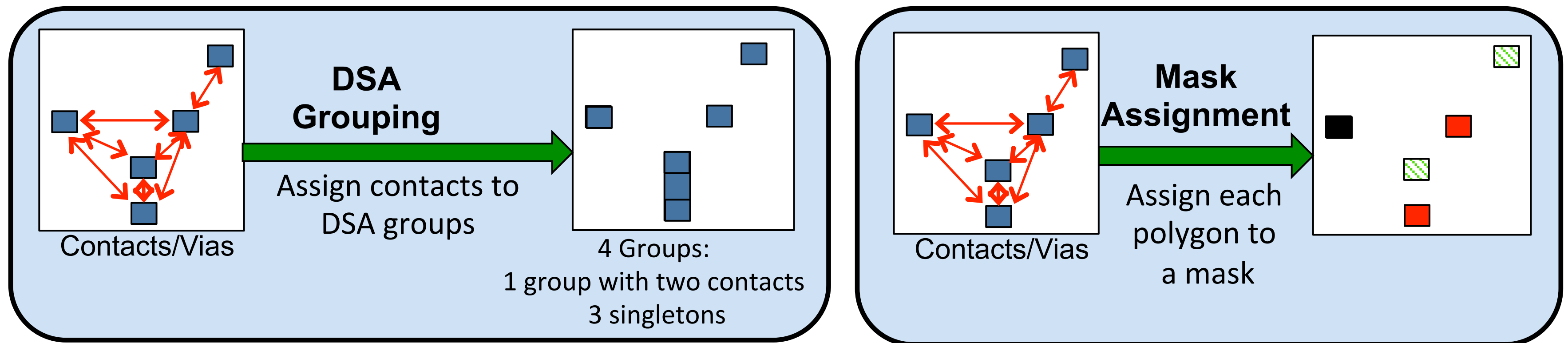
- Directed Self Assembly (DSA) is a strong candidate for future technology nodes



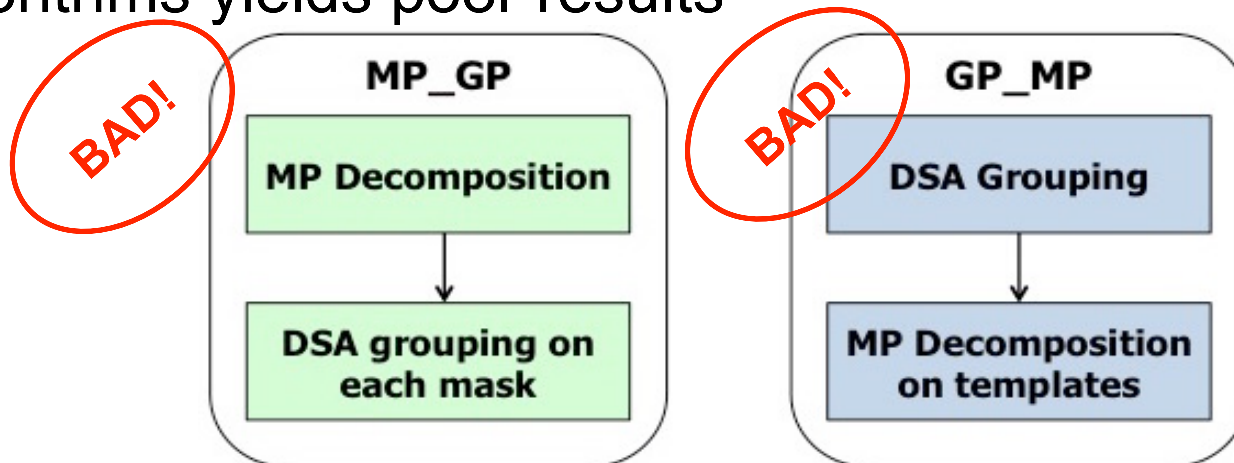
- **BUT** Pure DSA can not achieve 7nm node or beyond
  - Because resolution required for GP can not be delivered by 193i lithography
  - Challenges in finding BCPs which can achieve that small pitch

- Integration of **DSA** with **Multiple Patterning (MP)** is attractive for sub-7nm
  - Reduce number of masks → less costly process
  - Potentially more flexibility in polygon sizes

DSA Grouping and Mask Assignment

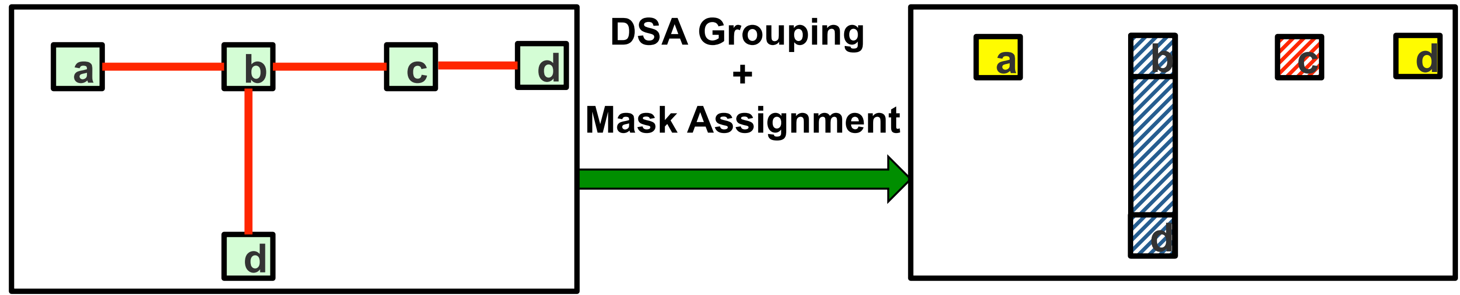


- Previous work *(Badr et al; SPIE'15)* showed that cascading existing DSA grouping and MP decomposition algorithms yields poor results



This Work

Objective of this work

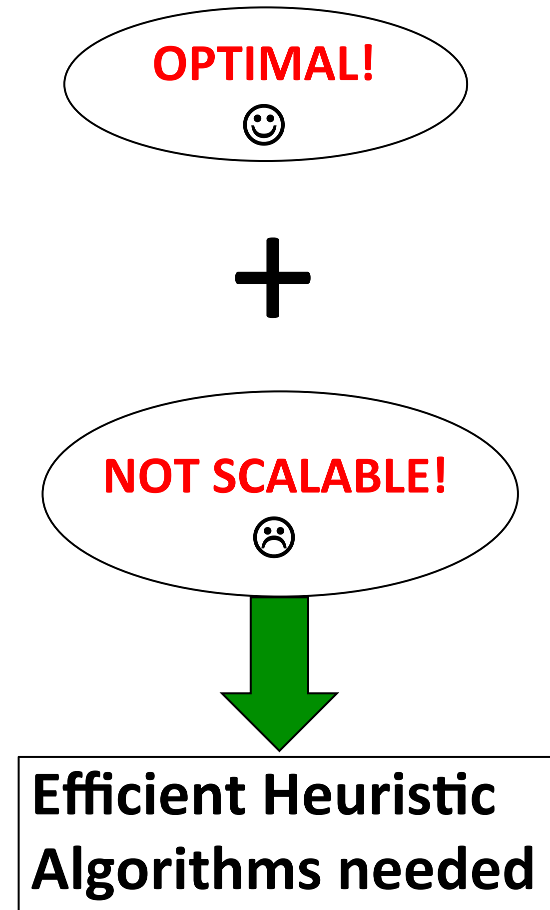


Contribution

Optimal ILP ← Benchmark against ← **Graph-based Heuristic**

Integer Linear Programming (ILP) Formulation

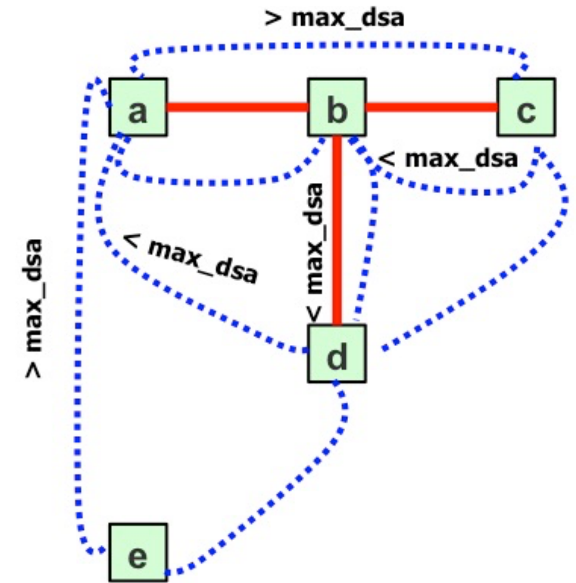
- Objective: minimize number of conflicts
  - A conflict is when two contacts with inter-distance < **litho_dist** are
    - on **same mask** and
    - **not in same DSA group**
- Constraints [Simplified]:
  - Two "close" contacts are assigned to different masks or same DSA group if possible
  - Number of contacts in each group ≤ max_g



- ILP works for DP, TP, QP, and any number of masks that is power of two.

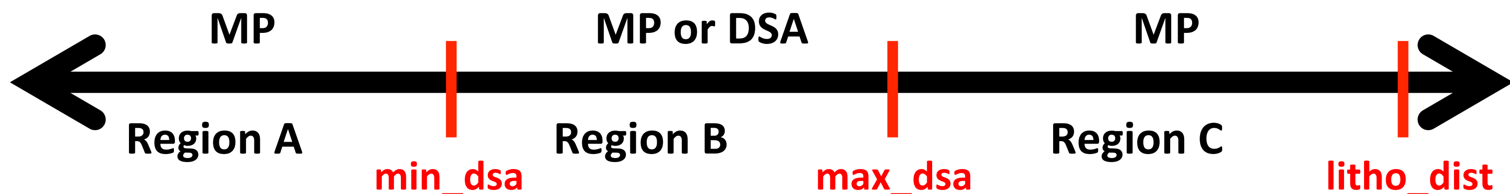
Hybrid Graph Representation

1. **Spacing Edge**: between every pair of contacts within *litho_dist*
2. **Grouping Edge**: between every pair of neighboring contacts that can be DSA-grouped
   - *min_dsa* ≤ distance ≤ *max_dsa*
   - Collinear, on same y or x axis
     - To have 193i-manufacturable templates



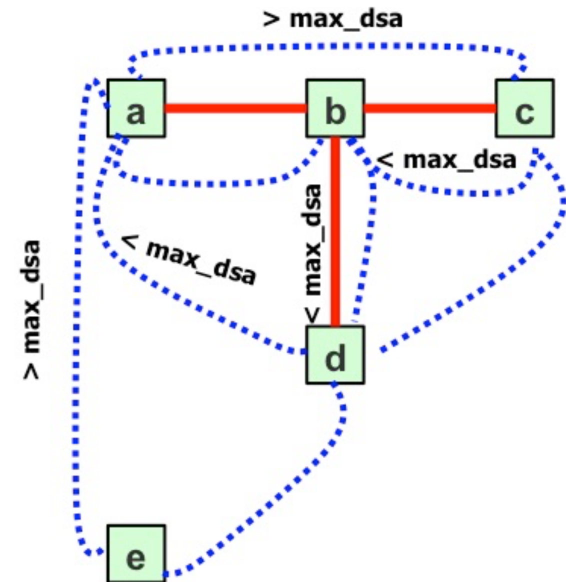
Blue: Spacing Edge
Red: Grouping Edge

Ranges of Distance between two polygons where spacing violation can be resolved by MP or DSA



Proposed Heuristic

- Maximize chance of DSA grouping ➔maximize possibility of eliminating conflicts
- Find max number of grouping edges with no common nodes

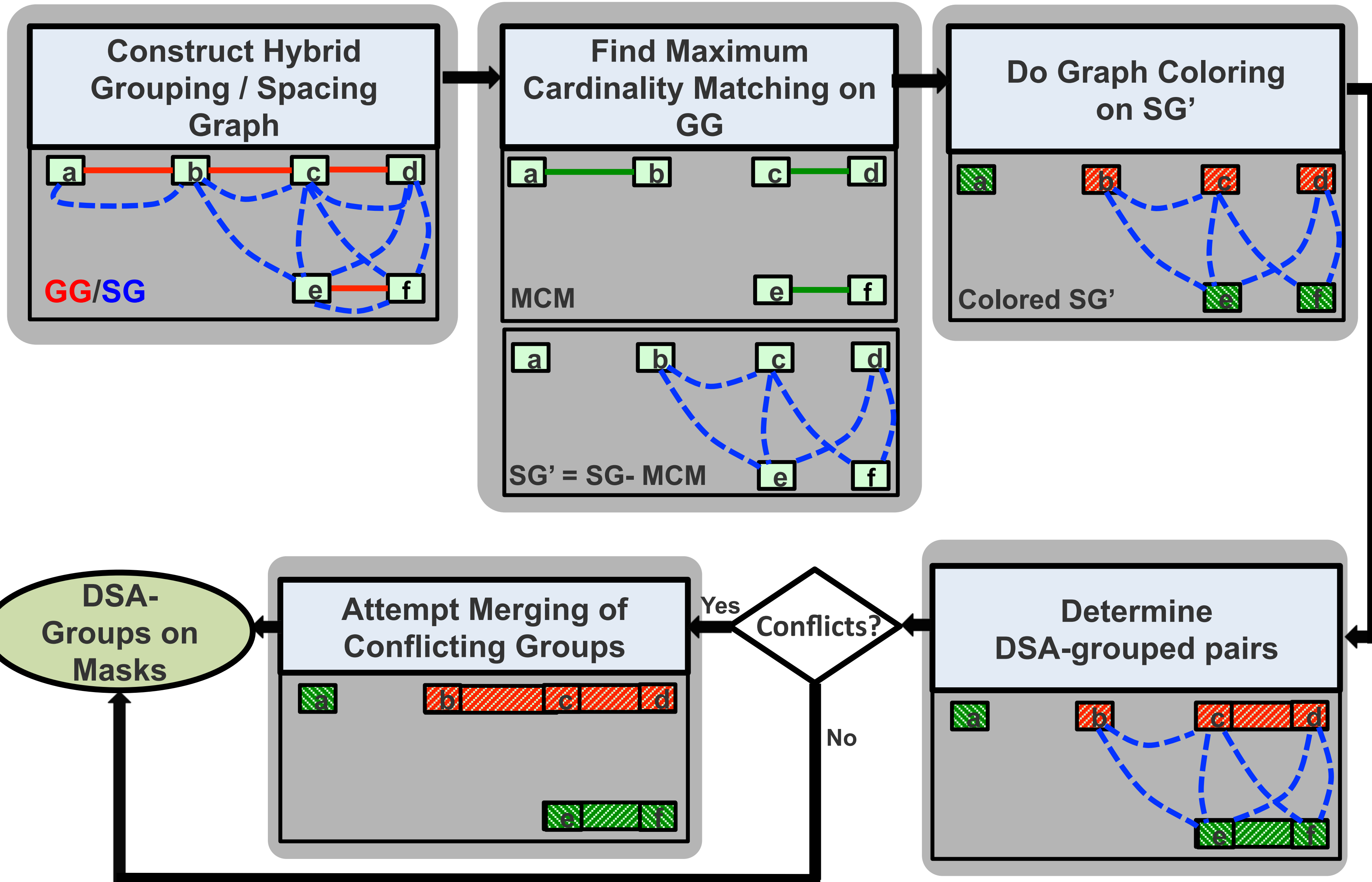


Blue: Spacing Edge
Red: Grouping Edge

Maximum Cardinality Matching (MCM)

Can be solved in polynomial time!

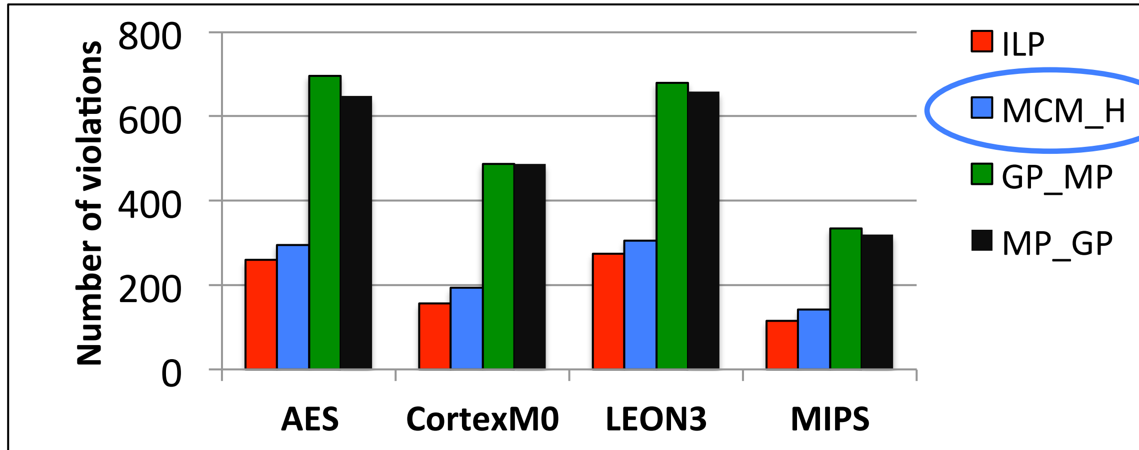
Proposed Heuristic Algorithm: MCM_H



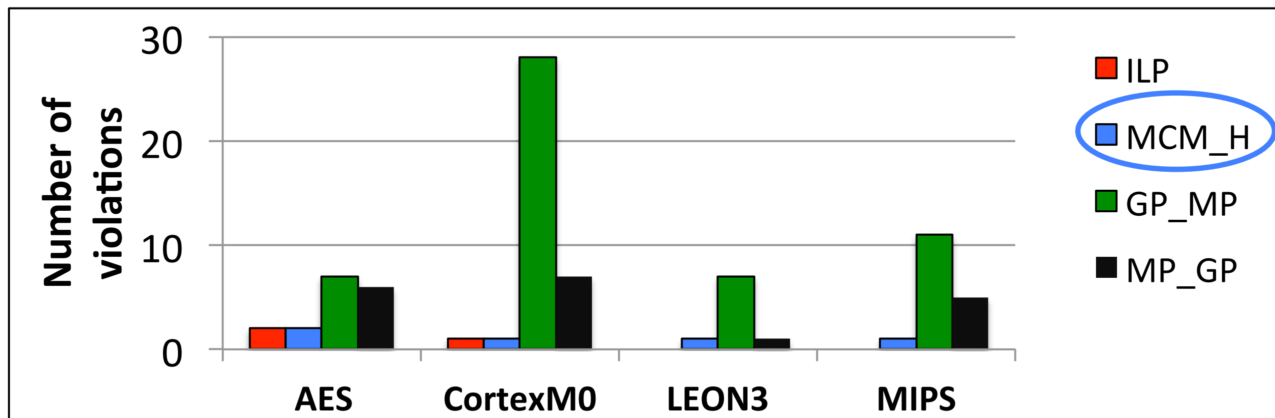
Results

Test case	Number of Vias
AES	48123
CortexM0	35255
LEON3	93474
MIPS	34784

N=2 (DP)



N=3 (TP)



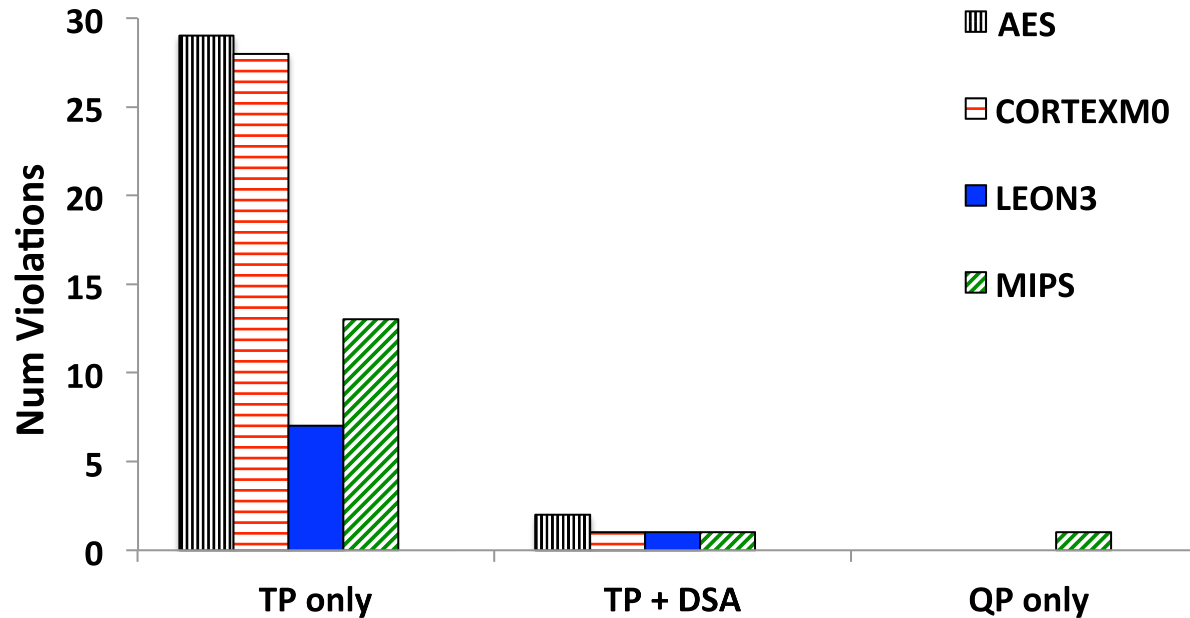
MCM_H is ~200x faster than ILP. (Max runtime on our test cases is 13s.)

MCM_H has 16.3% more violations than ILP.

MCM_H has 56% fewer violations than sequential approaches (GP_MP & MP_GP)

Can we really reduce one mask?

Number of violations with TP only, TP+DSA using MCM_H and QP only



Conclusion

- We proposed optimal ILP formulation to solve the simultaneous DSA grouping + MP decomposition problem for a hybrid DSA-MP process.
- We presented an efficient graph-based heuristic (MCM_H).
- MCM_H produces 16.3% more violations than ILP, but is ~200x faster.
- MCM_H produce 56% fewer violations than naïve sequential approaches which cascade grouping and decomposition.

Future Work

- Explore different MP+DSA integration schemes.
- Allow more flexible grouping enabled by EUV or more restricted due to Sidewall image transfer e.g. SAQP.

THANK YOU!

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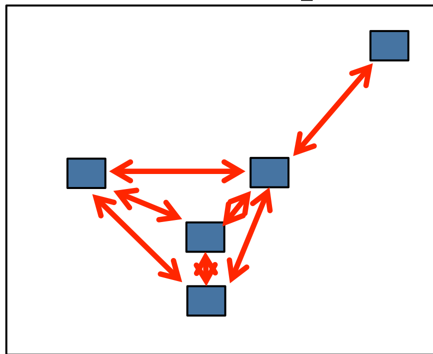
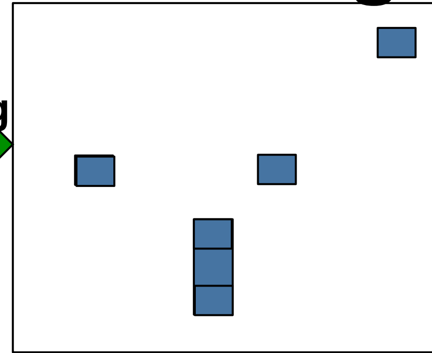
BACKUP

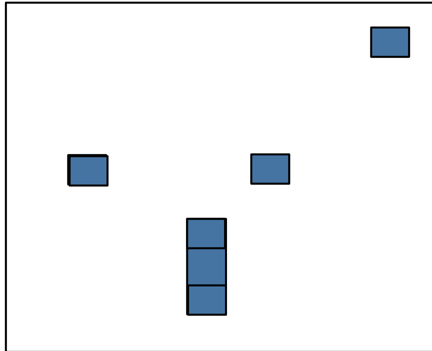
DSA Grouping and Mask Assignment


Contacts/Vias

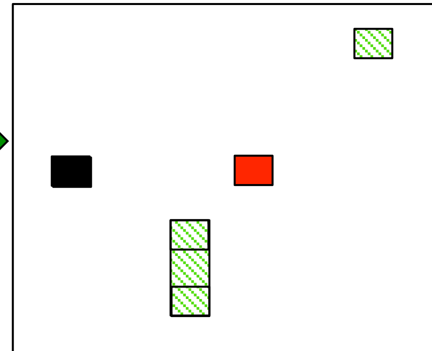
DSA Grouping

Which contacts are printed using the same template

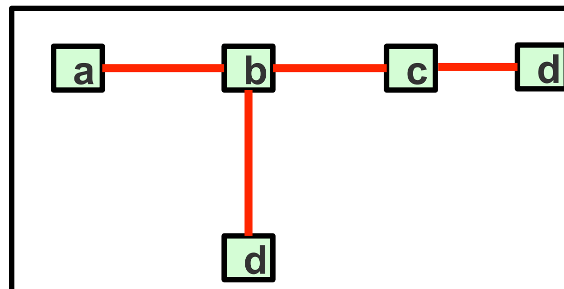

4 Groups: 1 group with two contacts and 3 singletons



Mask Assignment

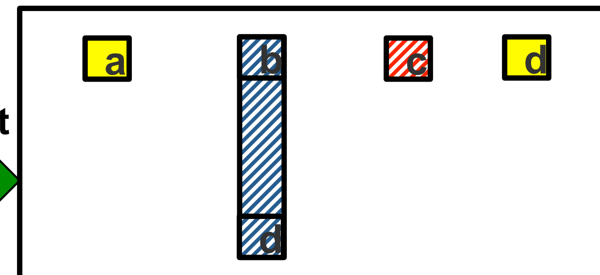


Objective of this work



Contacts/Vias

DSA Grouping + Mask Assignment



Hybrid DSA-MP Process

Important Parameters and Rules

N
Number of masks

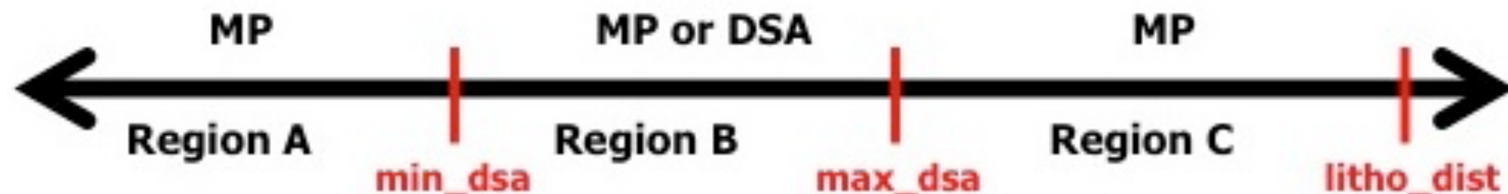
litho_dist
Min allowed space on a mask

min_dsa
Min distance between two contacts in a DSA groups

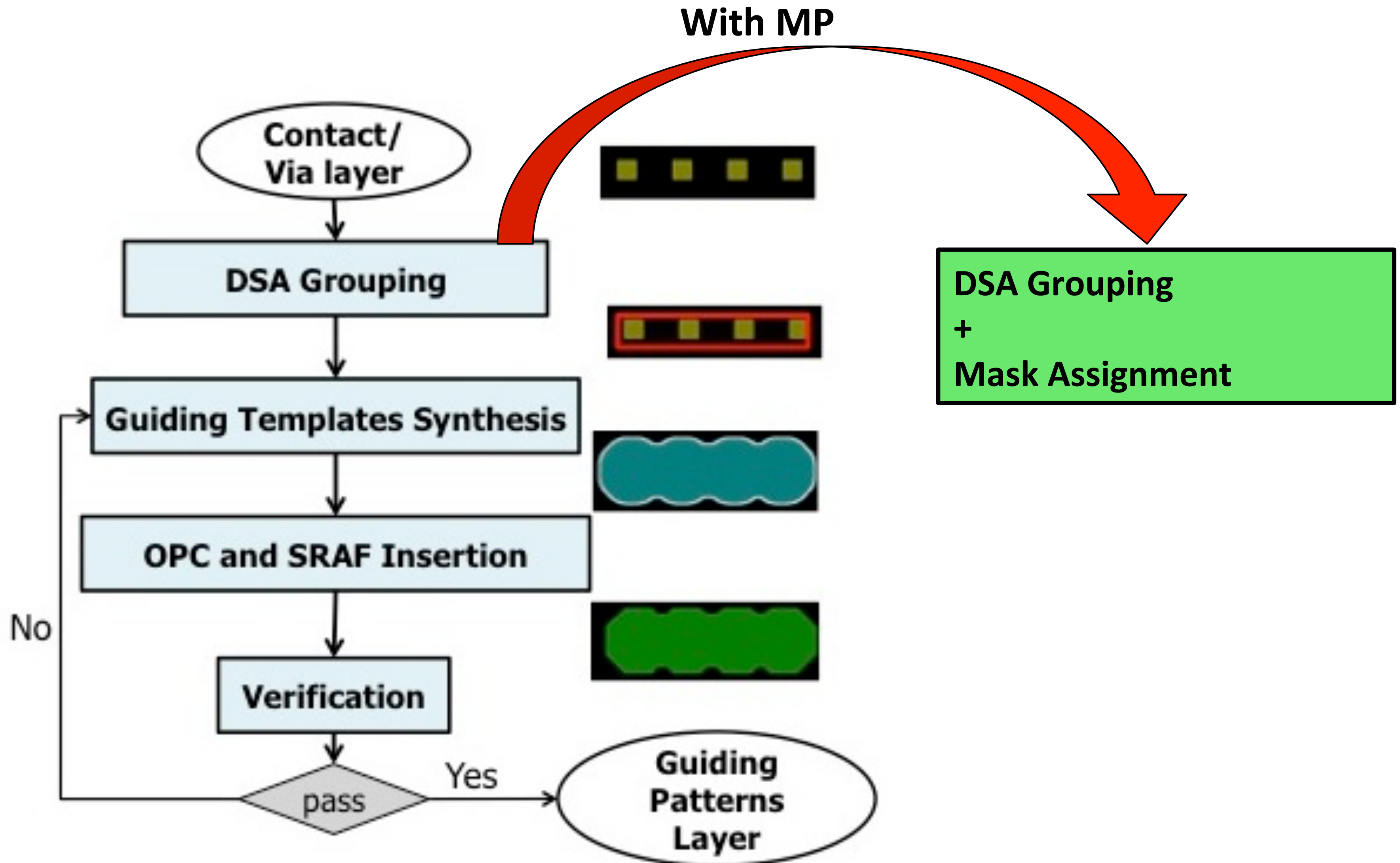
max_dsa
Max distance between two neighboring contacts in one DSA group

max_g
Maximum number of contacts in a single DSA group

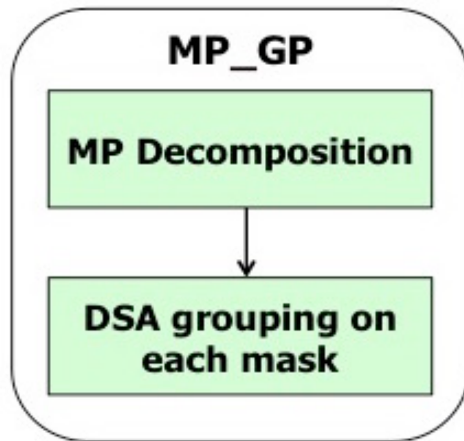
Ranges of Distance between two polygons where spacing violation can be resolved by MP or DSA

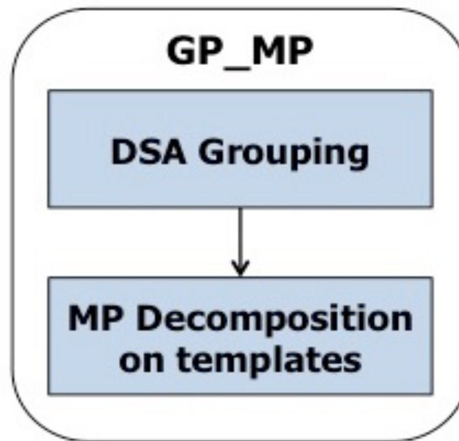


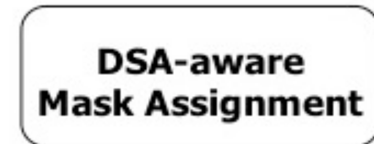
CAD flow for DSA

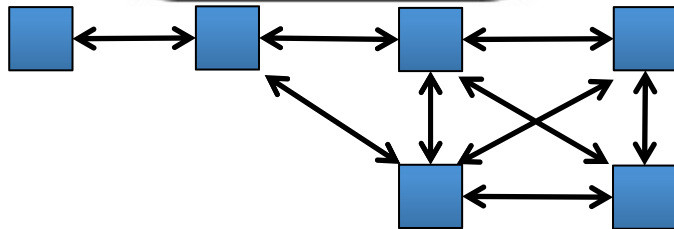


Alternative Flows

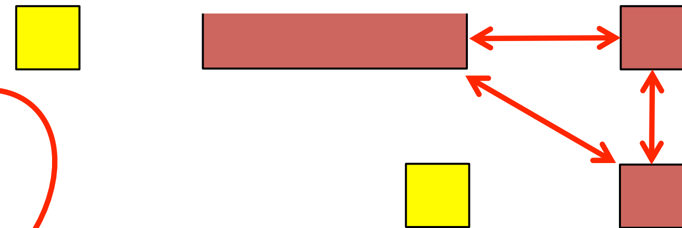




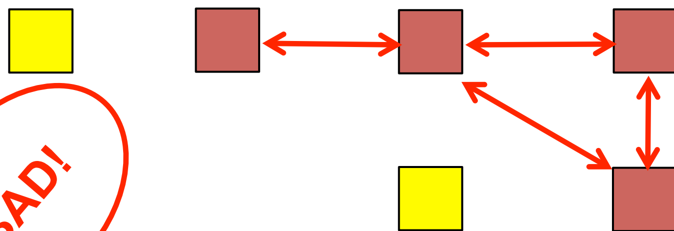




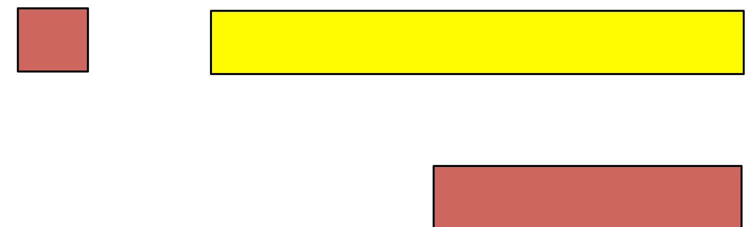
Original Snippet.



Result of MP_GP, N=2.
The marker shows a spacing violation.



Result of GP_MP, N=2.
The marker shows a spacing violation.



Conflict-free
Grouping & Decomposition, N=2.

Experiments and Results

- Test cases have been synthesized, placed and routed using commercial 45nm SOI libraries, then scaled and sized
- Used via1 layer. After scaling: min space=21nm, via width=14nm
- Implemented in C++, using Boost library, OpenAccess
- Used Calibre Multi-patterning tool

Number of vias in test cases

Test case	Number of Vias
AES	48123
CortexM0	35255
LEON3	93474
MIPS	34784

Parameters used in experiments

min_dsa	20
max_dsa	42
litho_dist	66
max_g	2
contact width	14
L_0	34
N	2 (DP) and 3(TP)