A Cost-Driven Lithographic Correction Methodology Based on Off-the-Shelf Sizing Tools

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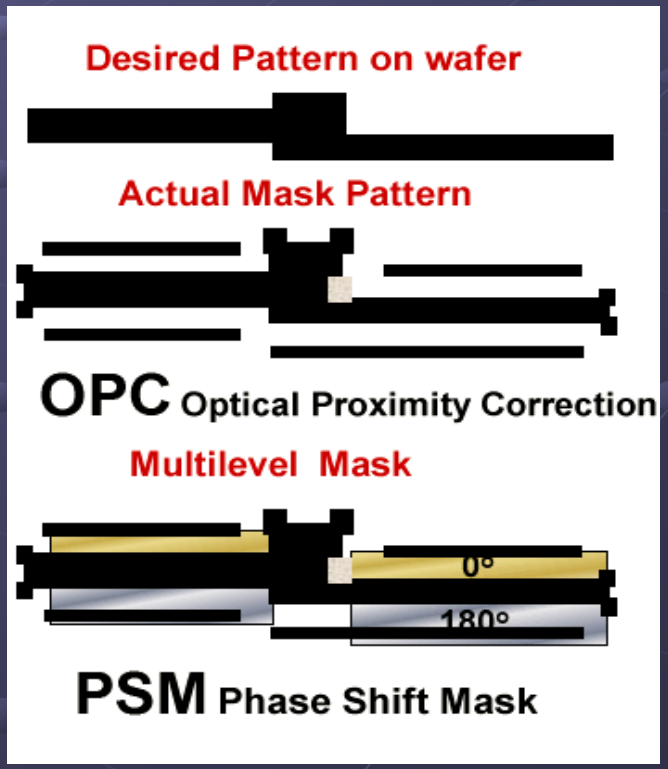
Outline

- Trends in Mask Cost
- Design for Value
- MinCorr: The Cost of Correction Problem
- Generic Cost of Correction Methodology
- MinCorr: Parallels to Gate Sizing
- Experiments and Results
- Conclusions and Ongoing Work

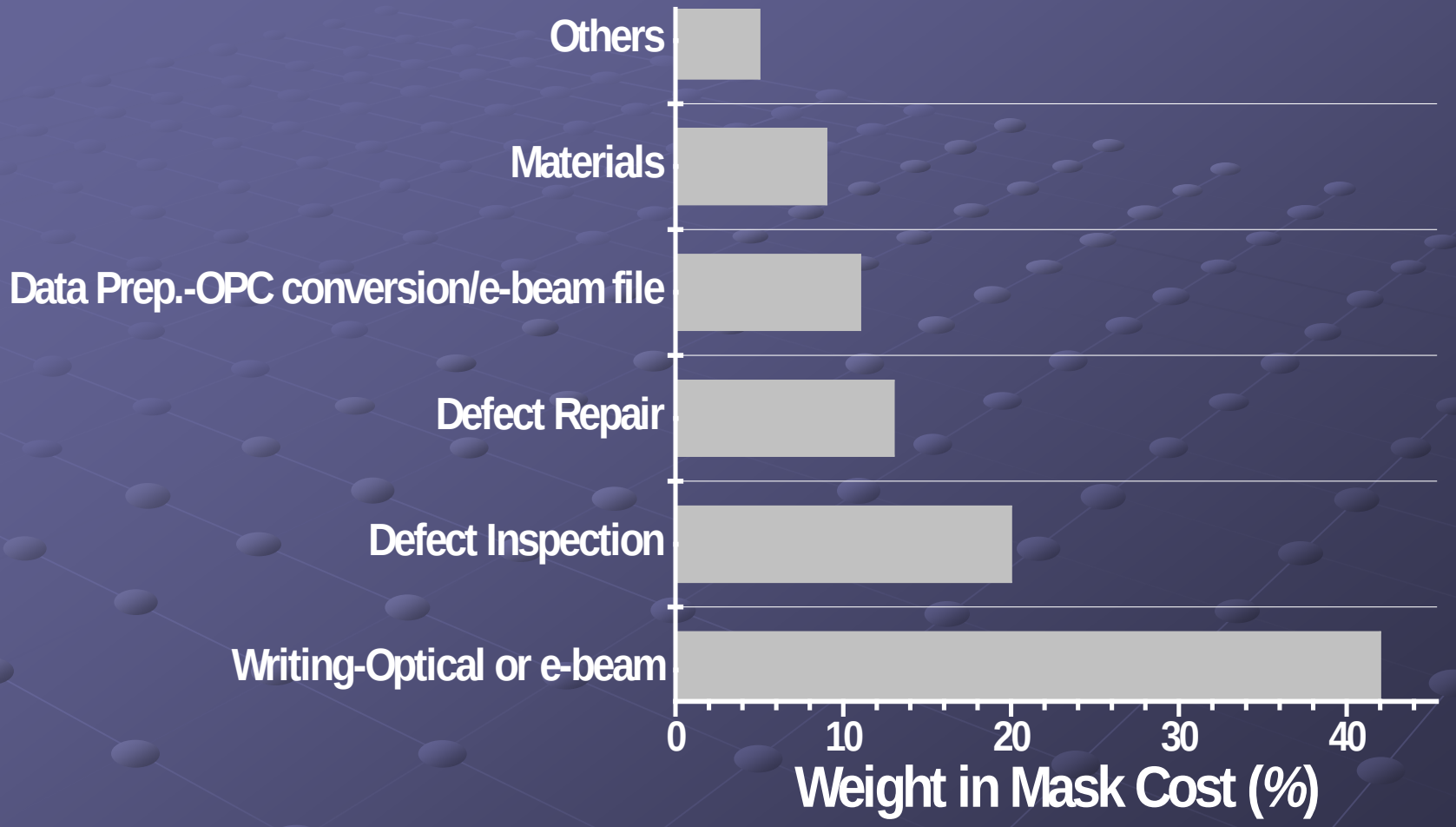
Stringent CD Requirements

Year	2001	2004	2007
Technology Node	130nm	90nm	65nm
MPU Gate Length	90nm	37nm	25nm
Gate CD Control(3σ)	5.3nm	3.0nm	2.0nm

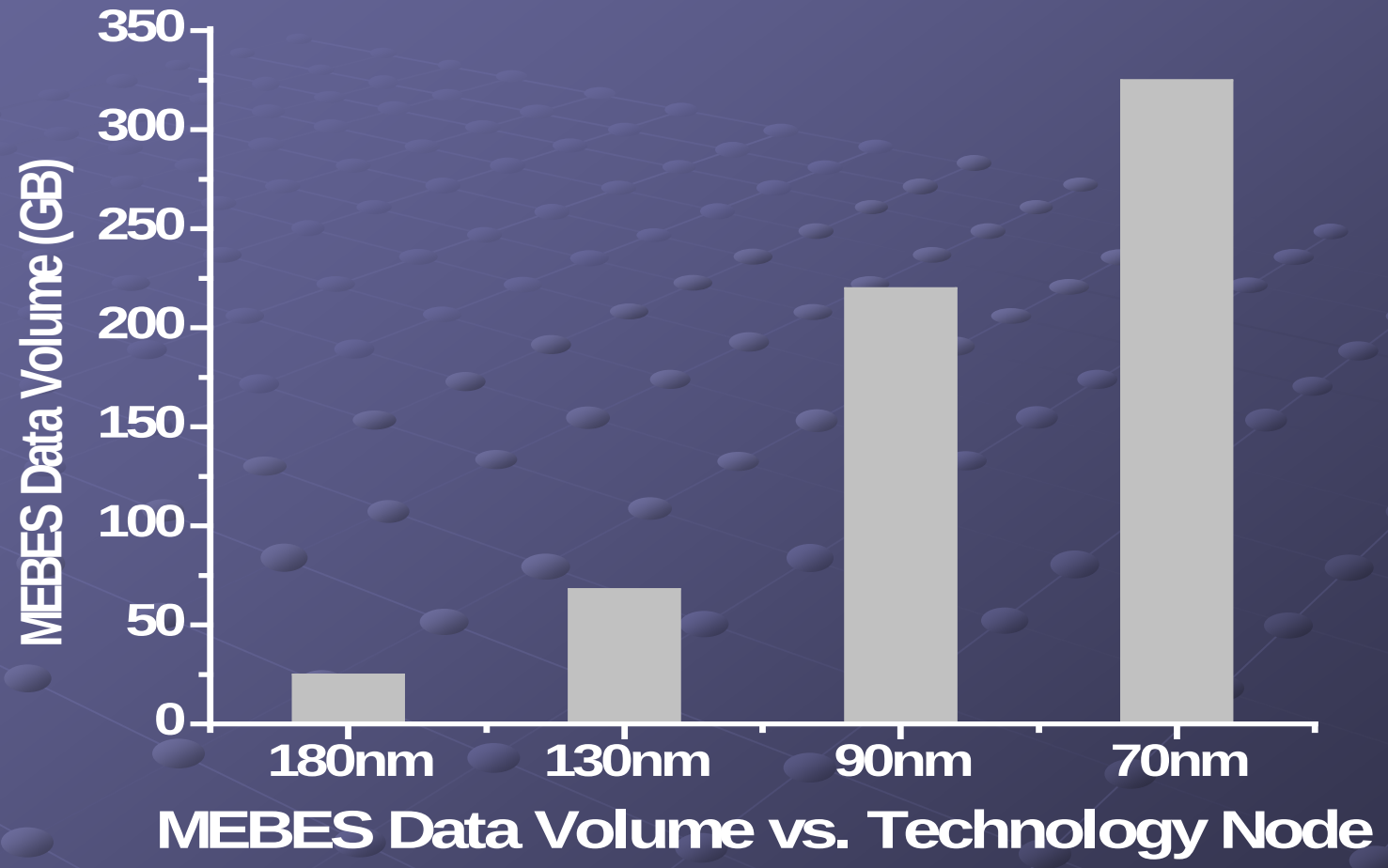
- ITRS predicts aggressive CD control as a critical issue
- Resolution Enhancement Techniques (RETs) such as Optical Proximity Correction (OPC) and Phase Shift Mask (PSM) used



Mask Cost Components



Mask Data Volume



Large data volume ⇒ Long mask write times ⇒ Increase in mask cost

Trends in Mask Cost

- RETs increase mask feature complexities and hence mask costs
  - No. of line edges increase by 4-8X after OPC
    ⇒ (for vector scanning) increased mask write time
  - “Million dollar mask set” in 90nm (Sematech, 2000)
- Average mask set produces only 570 wafers
  - → amortization of mask cost is difficult
- Mask writers work equally hard to perfect critical and non-critical shapes
  - Errors found in either during mask inspection will cause the mask to be discarded
  - RET and mask write are function-oblivious!

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Design for Value*

- Mask cost trends → **Design for Value (DFV)** methodologies

Design for Value Problem:

Given

- Performance measure *f*
- Value function *v(f)*
- Selling points f_i corresponding to various values of *f*
- Yield function *y(f)*

Maximize **Total Design Value = Σ_i $y(f_i)*v(f_i)$**

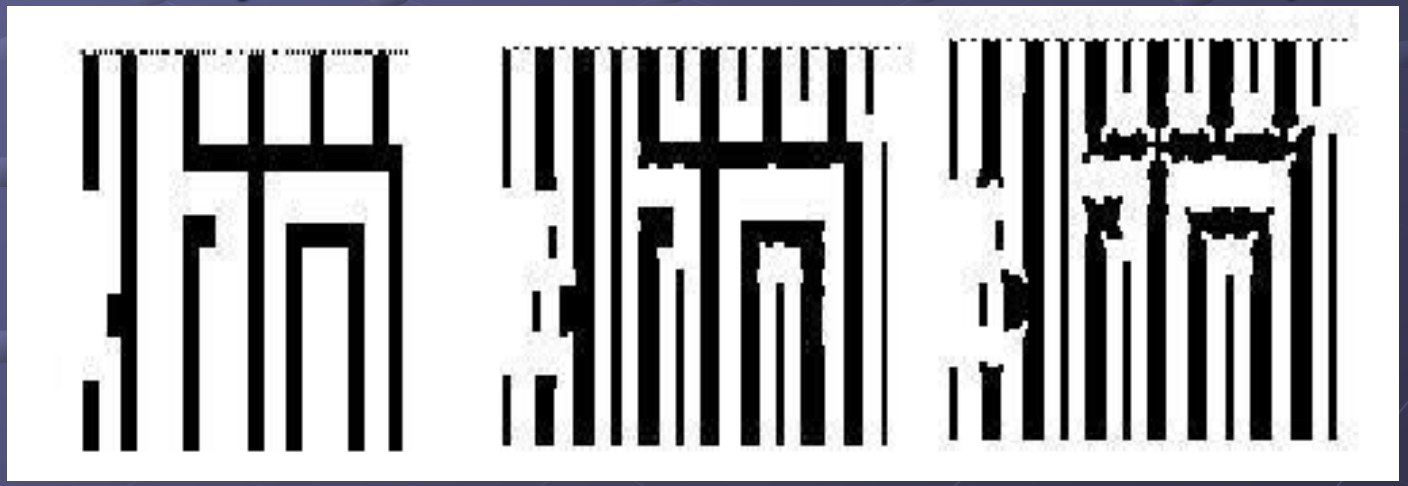
[or, Minimize Total Cost]

- Probabilistic optimization regime

* See "Design Sensitivities to Variability: Extrapolation and Assessments in Nanometer VLSI", *IEEE ASIC/SoC Conference*, September 2002, pp. 411-415.

DFV At Process Level

- Inject concept of function into mask flow
- Selective OPC
  - Various levels of OPC depending on timing and yield criticality of features
  - Obtain desired level of parametric yield
- Printability: some min level of OPC is required



No OPC Medium OPC Aggressive OPC

* Figure courtesy: Kurt Wampler, ASML Mask Tools, Inc.

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Performance Measure = Delay

- *Selling point delay* = circuit delay which achieves desired level (say 99%) of parametric yield
- Goal: Achieve selling point delay with minimum cost of RET's (OPC)

MinCorr: The Cost of Correction DFV Problem

Given: Admissible levels of correction for each layout feature and the corresponding delay impact (mean and variance)

Find: Level of correction for each layout feature such that a prescribed selling point delay is attained

Objective: Minimize total cost of corrections

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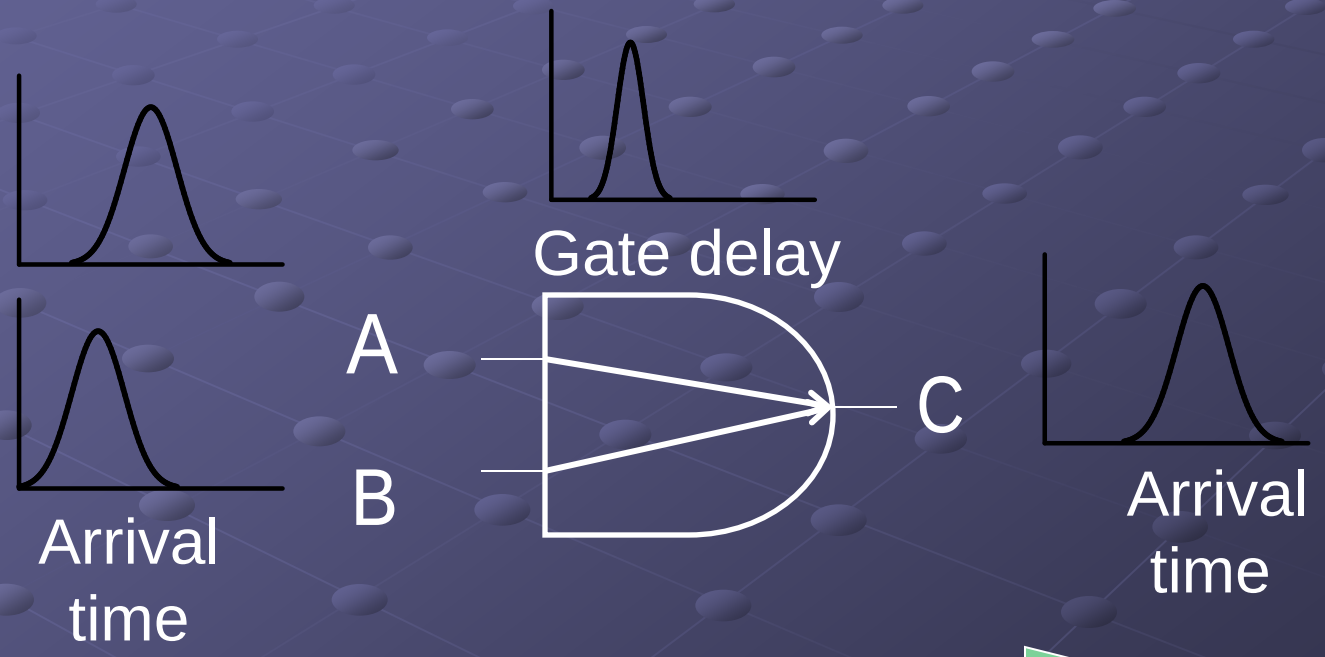
Statistical Timing Analysis

Statistical STA (SSTA) provides PDFs of arrival times at all nodes

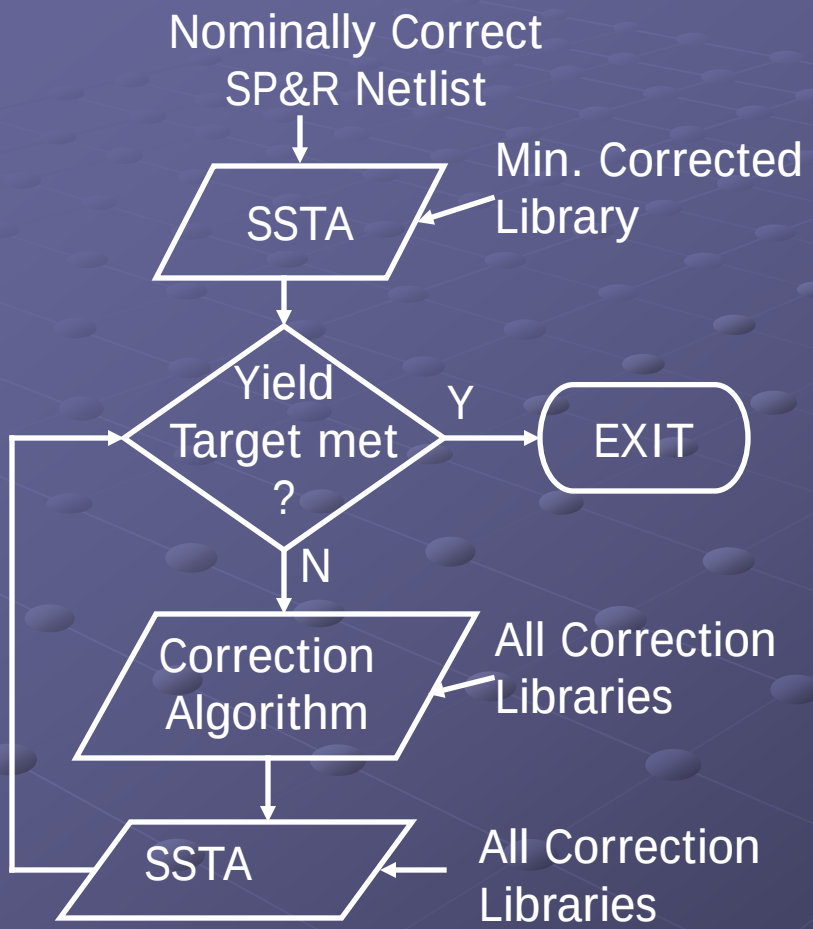


Variation Aware Library Model

- Capacitance and delay values replaced by (μ,σ) pair
- Sample variation aware .lib

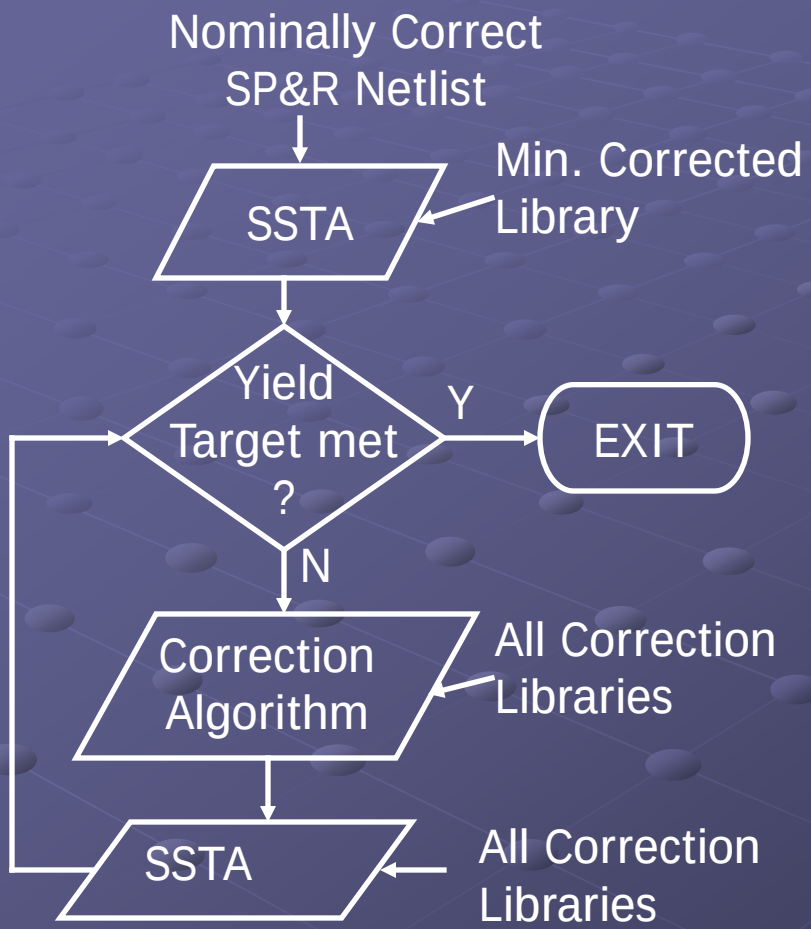
```
pin(A) {
   direction : input;
   capacitance : (0.002361,0.0003);
 }
…
timing() {
      related_pin : "A";
      timing_sense : positive_unate;
      cell_rise(delay_template_7x7) {
        index_1 ("0.028, 0.044, 0.076");
        index_2 ("0.00158, 0.004108, 0.00948");
        values ( \
          “(0.04918,0.001), (0.05482,0.0015), (0.06499,0.002)",
….
```

Generic Cost of Correction Methodology



- Statistical STA (SSTA) provides PDFs of arrival times at all nodes
- Assume variation aware library models (for delay) are available

Generic Cost of Correction Methodology



- Statistical STA (SSTA) provides PDFs of arrival times at all nodes
- Assume variation aware library models (for delay) are available
- Statistical STA currently has runtime and scalability issues

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MinCorr: Parallels to Gate Sizing

- Assume
  - Gaussian-ness of distributions prevails
    - $\Rightarrow \mu + 3\sigma$ corresponds to 99% yield
  - Perfect correlation of variation along all paths
    - $\Rightarrow$ Die-to-Die variation
    - $\Rightarrow \mu_{1+2} + 3\sigma_{1+2} = \mu_1 + 3\sigma_1 + \mu_2 + 3\sigma_2$
- Resulting linearity allows propagation of $(\mu+3\sigma)$ or 99% (selling point) delay to primary outputs using standard Static Timing Analysis (STA) tools

MinCorr: Parallels to Gate Sizing

MinCorr

~~*Gate Sizing*~~ *Problem:*

costs of correction

delay ($\mu+k\sigma$)

Given allowed ~~areas~~ and corresponding ~~delays~~ of each cell,

minimize total ~~die area~~ subject to a ~~cycle time~~ constraint

cost of OPC

selling point delay

Gate Sizing	≡	**MinCorr**
Cell Area	≡	Cost of correction
Nominal Delay	≡	Delay ($\mu+k\sigma$)
Cycle Time	≡	Selling point delay
Die Area	≡	Total cost of OPC

Components of MinCorr Sizing

- A yield-aware library that captures
  - Delay mean and variance for each library master for each level of correction
  - Relative cost of OPC for each master corresponding to each level of correction
- Use standard off-the-shelf logic synthesis tool to perform sizing
  - Can use well-tested sizing methods
  - Practical runtimes
  - Can handle interesting variants, e.g., cost-constrained selling point delay minimization

MinCorr: Yield Aware Library Characterization

- Mask cost is assumed proportional to number of layout features
- Monte-Carlo simulations, coupled with linear interpolation, are used to estimate delay variance given the CD variation
- We generate a library similar to Synopsys .lib with ($\mu+3\sigma$) delay values for various output loads
  - Cost modeled by relative figure count multiplied by the number of transistors in the cell
  - Gate input capacitance variation with CD considered

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Experiments and Results

- Synopsys Design Compiler used as the synthesis tool to perform “gate sizing”
- Figure counts, critical dimension (CD) variations derived from Numerical Technologies OPC tool*
- Use a restricted TSMC 0.13 μm library
  - 7 cell masters: BUF, INV, NAND, NOR
- Approach tested on small combinational circuits
  - alu128: 8064 cells
  - c7552: 2081 cell ISCAS85 circuit
  - c6288: 2769 cell ISCAS85 circuit

*Courtesy Dipu Pramanik, NTI

Emulating An SSTA Tool

1. Generate 500 random delay values for each library master from the Gaussian distribution $N(\mu,\sigma)$
2. Generate 500 random input capacitance values perfectly correlated with corresponding random delay values
3. Generate 500 .libs having these random delay and capacitance values
4. *Monte Carlo Primetime*: Run STA tool 500 times, each time with a different .lib to obtain a delay distribution

Comparison With SSTA

- SSTA emulated by running Synopsys Primetime 500 times with 500 randomly generated .libs
- Monte Carlo Primetime is run with *independently* varying library masters but all instances of same master perfectly correlated
  $\Rightarrow$ Die-to-Die (DTD) with some component of Within-Die (WID) variation modeled
- Our ($\mu+3\sigma$) propagation approach is accurate for DTD variation but pessimistic in presence of WID variation

Comparison With SSTA

Testcase	OPC Level	SSTA ($\mu+3\sigma$) (ps)	Our Approach ($\mu+3\sigma$) (ps)
alu128	Aggressive	5.083	5.28
	Medium	5.116	5.36
	No	5.181	5.57
c7552	Aggressive	2.414	2.49
	Medium	2.436	2.54
	No	2.477	2.64
c6288	Aggressive	5.113	5.29
	Medium	5.150	5.38
	No	5.221	5.58

Note: ***pessimism*** and ***fidelity***

Yield Library Generation

Type of OPC	Ldrawn (nm)	3σ of Ldrawn	Figure Count	Delay (μ, 3σ) for NAND2X2
Aggressive	130	5%	5X	(64.82, 2.14)
Medium	130	6.5%	4X	(64.82, 2.80)
No OPC	130	10%	1X	(64.82, 4.33)

Sample Result of Library Generation

- Three levels of OPC considered
- Input slew dependence ignored
- Interconnect variation ignored

Cost Savings with MinCorr Sizing

Design	Normalized Cost	Normalized Selling Point Delay
alu128	5.0 (Aggressive OPC)	0.9644
	4.0 (Medium OPC)	0.9739
	1.0 (No OPC)	1.0000
	1.0657	0.9644
	1.0119	0.9976
c7552	5.0	0.9432
	4.0	0.9621
	1.0	1.0000
	1.4639	0.9432
	1.2079	0.9848
c6288	5.0	0.9480
	4.0	0.9642
	1.0	1.0000
	4.1530	0.9480

Cost Savings with MinCorr Sizing

- Small (~5%) selling point delay variation between max- and min-corrected versions of design (5X difference in cost)
- Sizing-based optimization achieves 17-79% reduction in OPC cost without sacrificing parametric yield

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Conclusions

- Function-aware OPC can reduce total cost of OPC while still meeting cycle time and yield constraints
- Can modify conventional performance optimization methods to solve the **MinCorr** problem;
  - We use an off-the-shelf synthesis tool to achieve up to 79% cost reduction compared to aggressive OPC, without increasing selling point delay
- Small change in yield going from no to aggressive OPC suggests that OPC may be a manufacturability issue rather than yield issue

Ongoing Work

- SSTA based correction flow
- Apply selective OPC at granularities other than gate-level (incl. radius of influence effects)
- Alternative MinCorr solution approaches based on transistor sizing and cost-based delay budgeting methods
- Include interconnect variation in the analysis
- Make the yield library input slew time aware

Ongoing Work

- Current sizing approach models Die-to-Die variation accurately but ignores Within-Die (WID) component
- SSTA with WID
  - Randomly perturbed SDF files
  - Monte Carlo Primetime
  - Ability to model arbitrary distributions of variations

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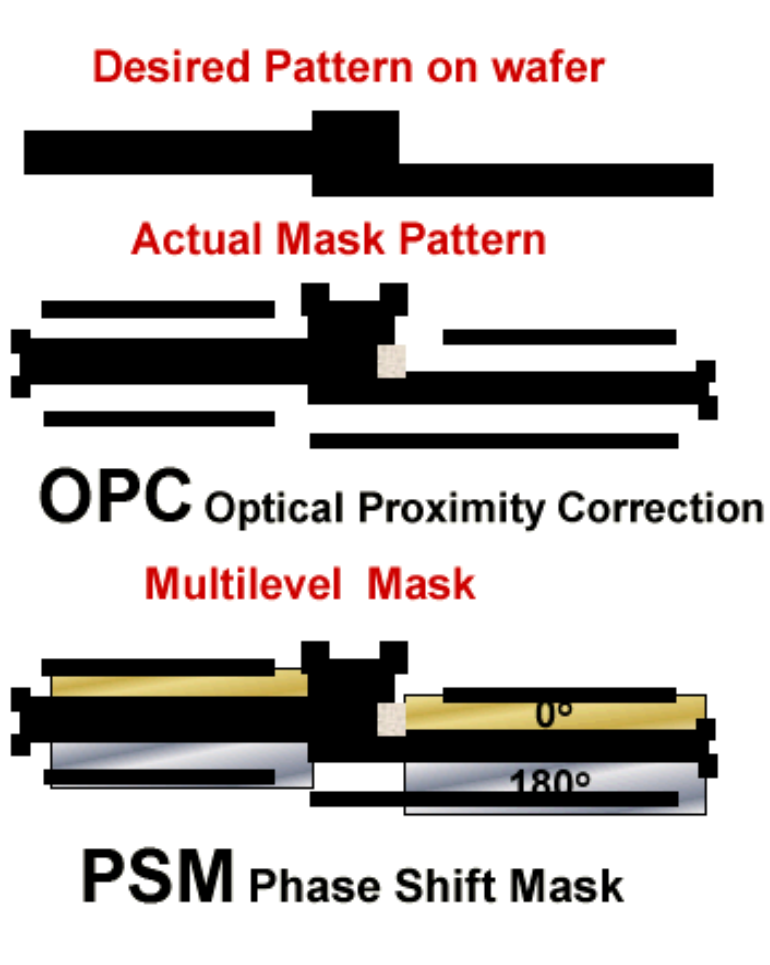
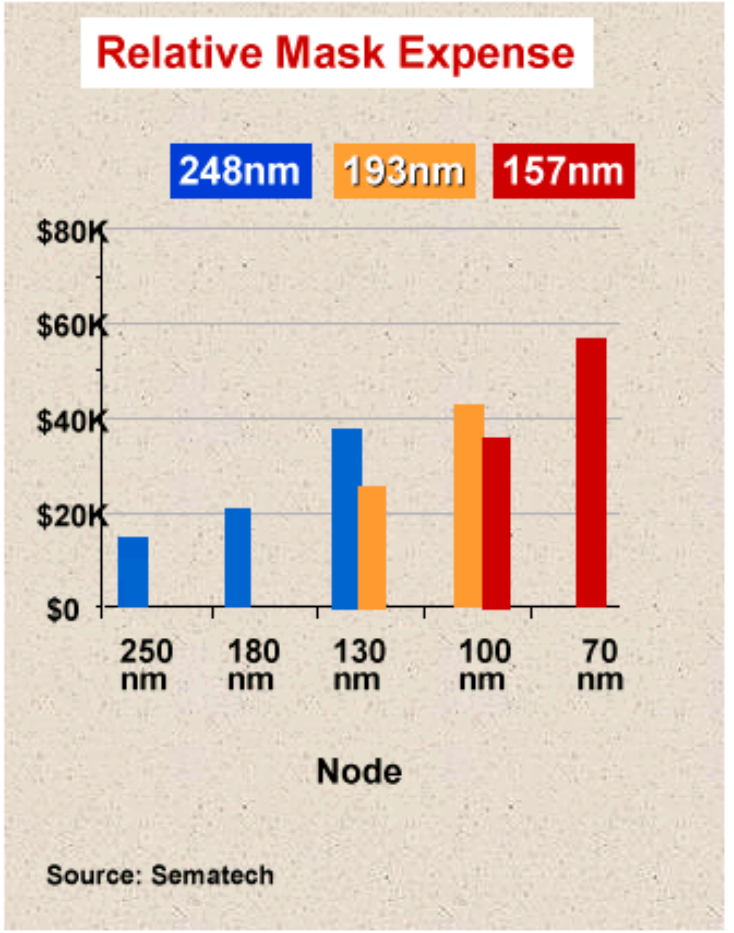
Trends in Mask Cost





"$1M mask set" in 100nm

OPC Overhead

- OPC increases figure count and mask complexity
  - No. of line edges increase by 4-8X after OPC

  ⇒ (for vector scanning) increase in mask write time
- *Rule Based OPC*
  - All rectangles identically corrected
- *Model Based OPC*
  - Enhancement to a feature made based on its geometry and local environment
- OPC fracturing tools view layout as function-oblivious GDSII ⇒ overcorrection

Toward A Min Cost of Correction Methodology

- Many layout features not timing critical → they can tolerate more process variation
- Less-aggressive OPC → lower costs (reduced figure counts, shorter mask write times, higher yields)
- Printability → certain min level of OPC is required
- *Selling point delay* = circuit delay which achieves desired level (say 99%) of parametric yield