Comprehensive Defect Avoidance Solution for Mitigating EUV Mask Defects

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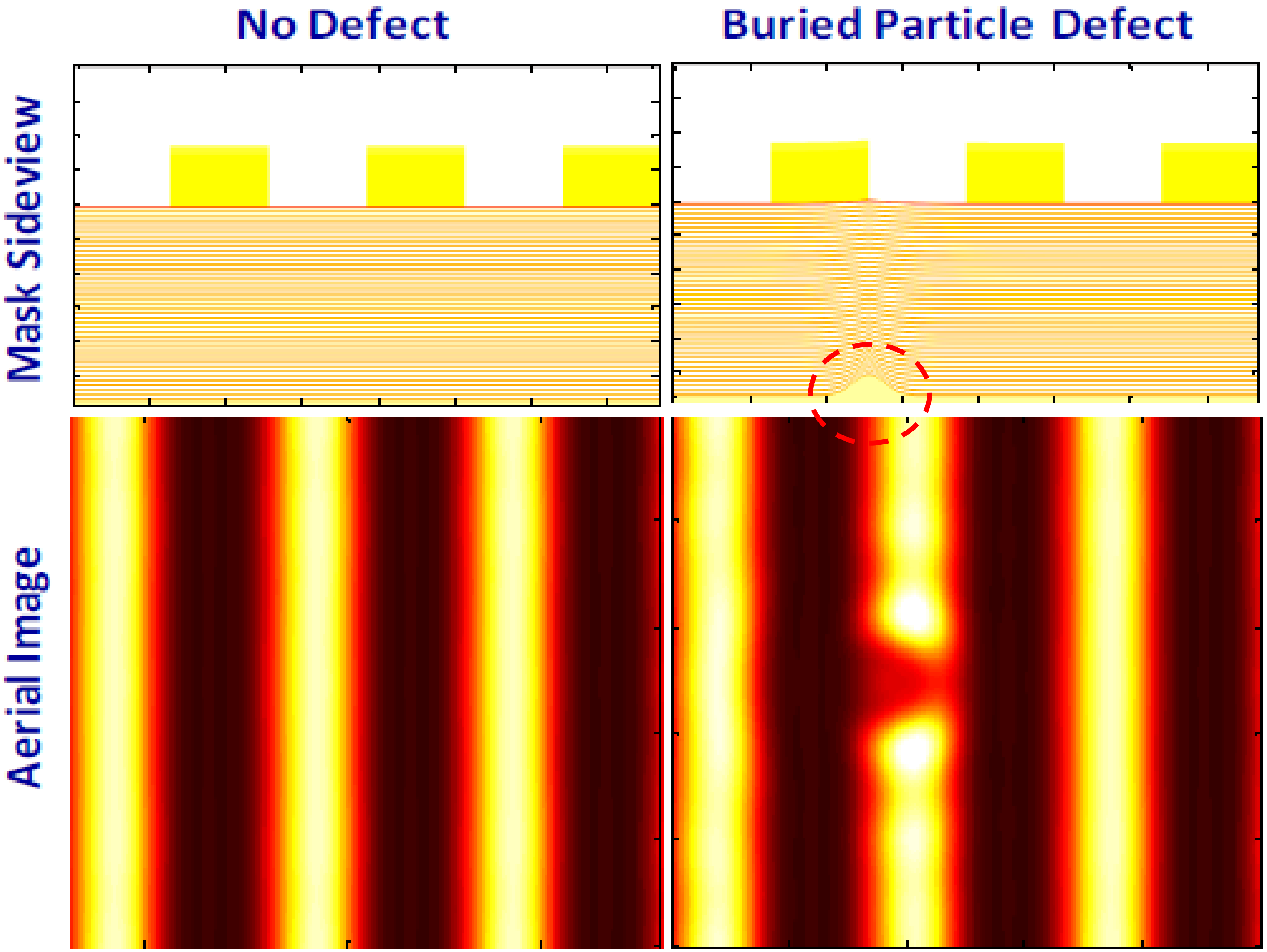
IMPACT+
integrated modeling process and computation for technology

Outline

- **EUV Mask Defect Mitigation and it's Limitations**
- Proposed Defect Avoidance Method
- Experimental Results

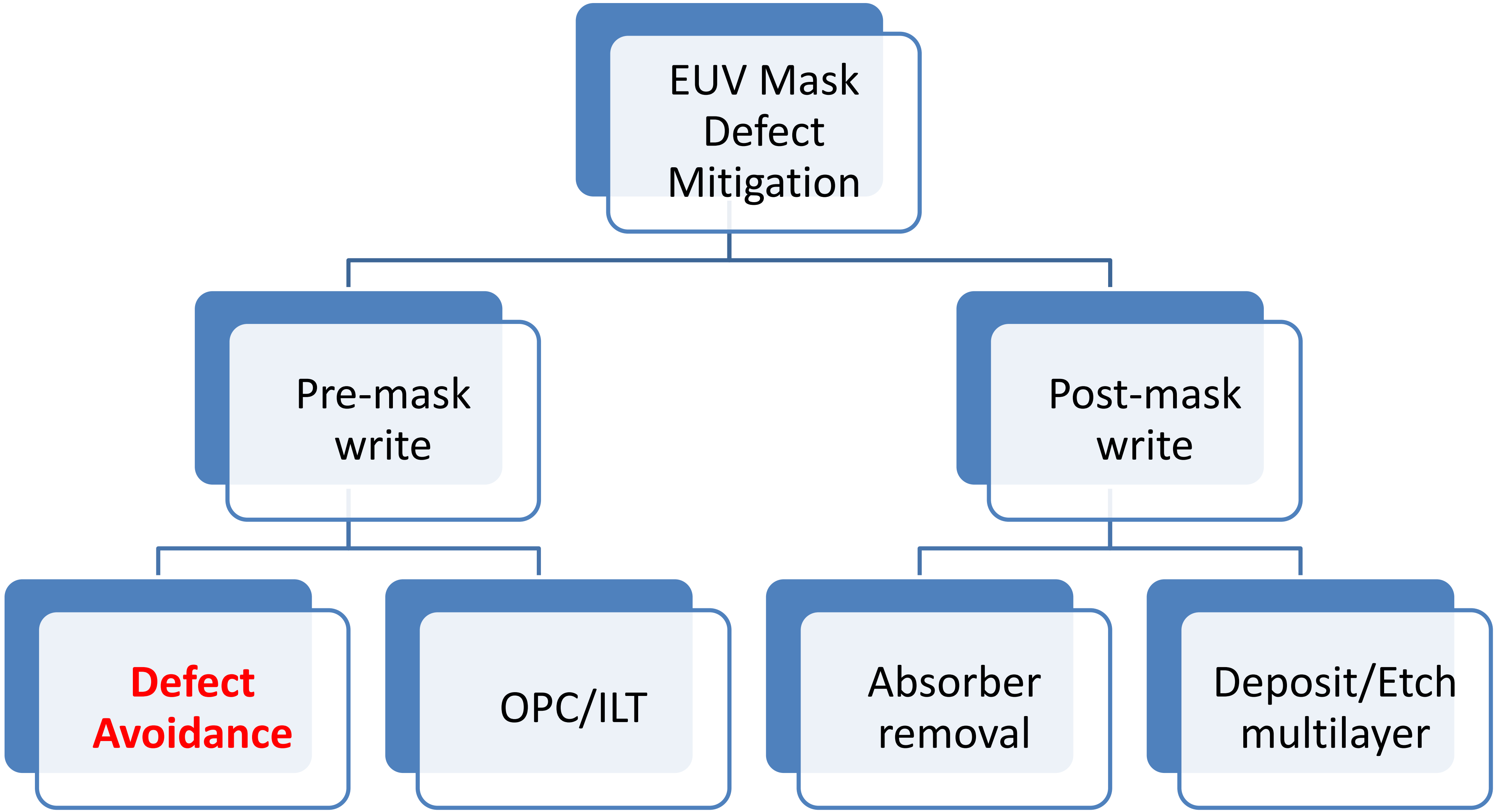
EUV Mask Blank Defects



Source: Clifford and Neureutheur, SPIE 2010

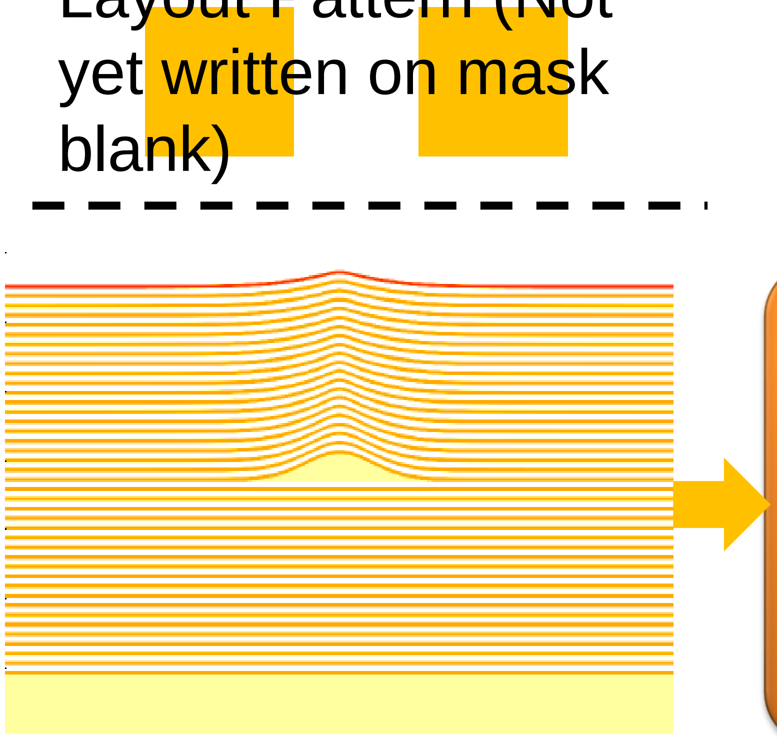
- **3.5nm high defect can cause 20nm CD change**
- Caused mainly due to substrate imperfections
- Current defectivity level of 10-50 defects per mask of size > 50nm width
- Many defects missed by inspection tool
- Repair expensive

Classification of EUV Mask Defect Mitigation Strategies

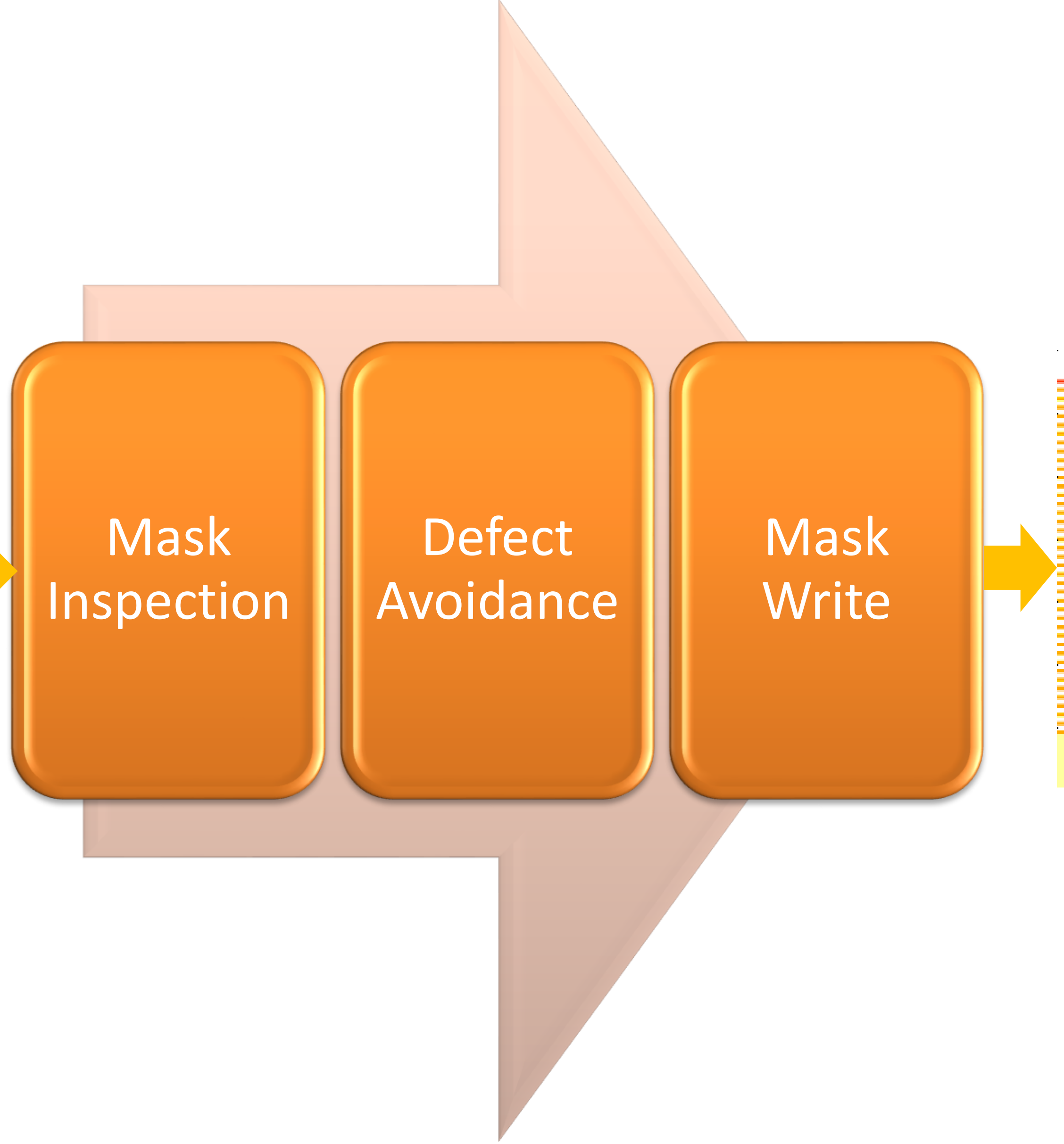


Defect Avoidance Based EUV Mask Defect Mitigation

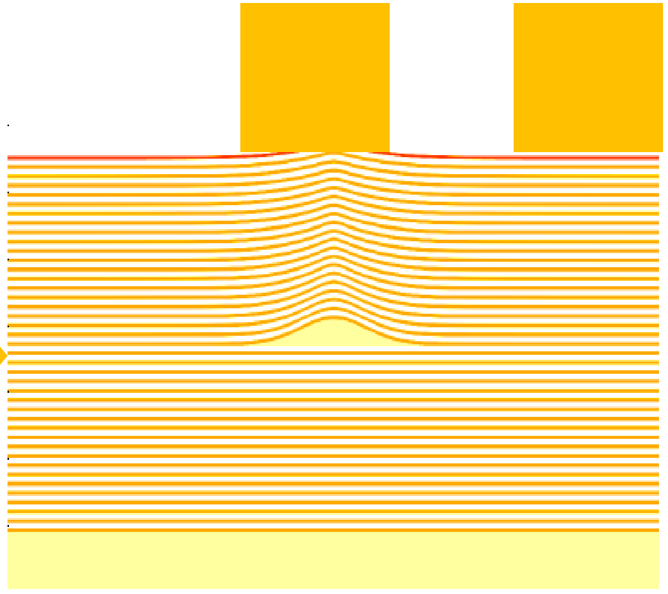
Layout Pattern (Not yet written on mask blank)



Mask Blank with buried defect

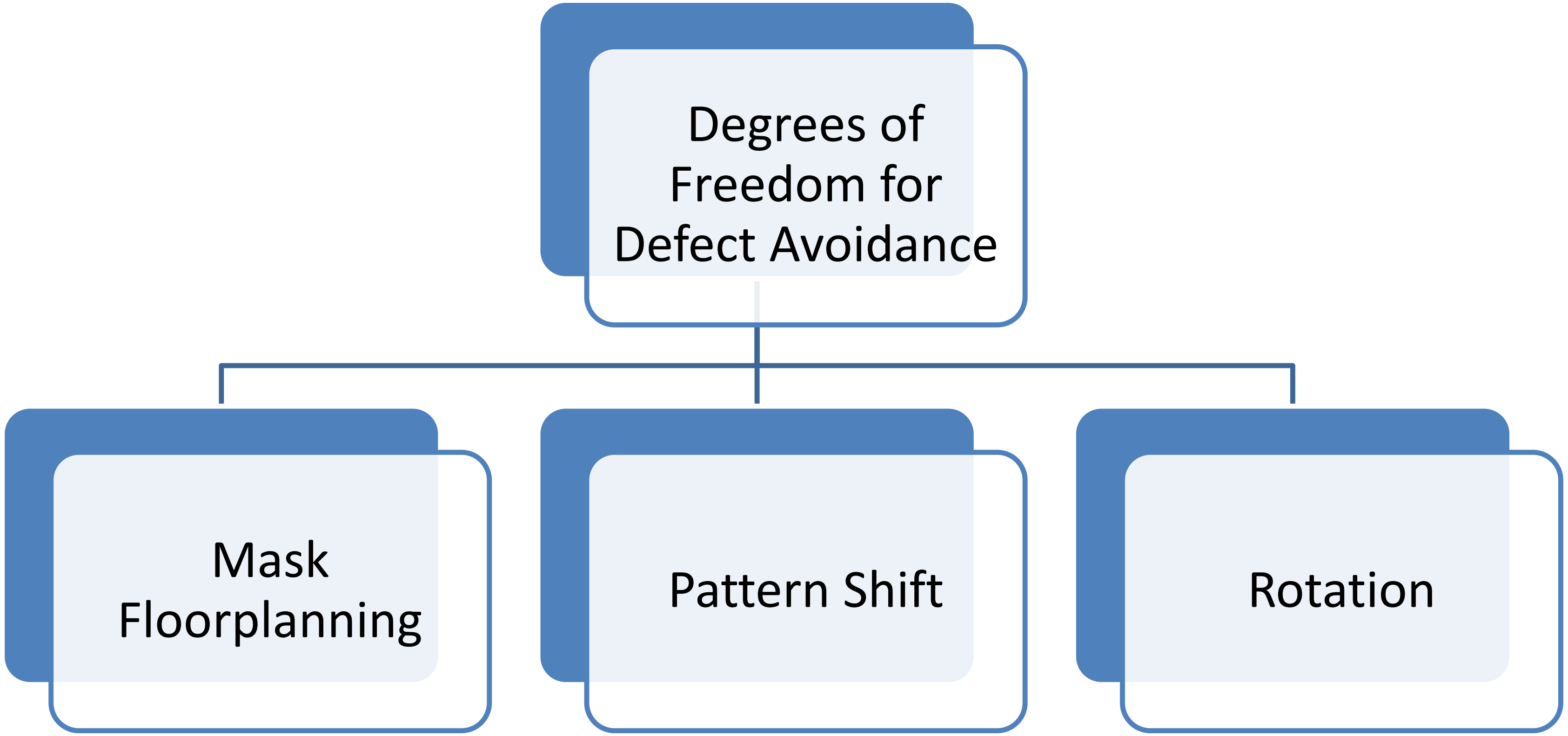


Defect covered by absorber

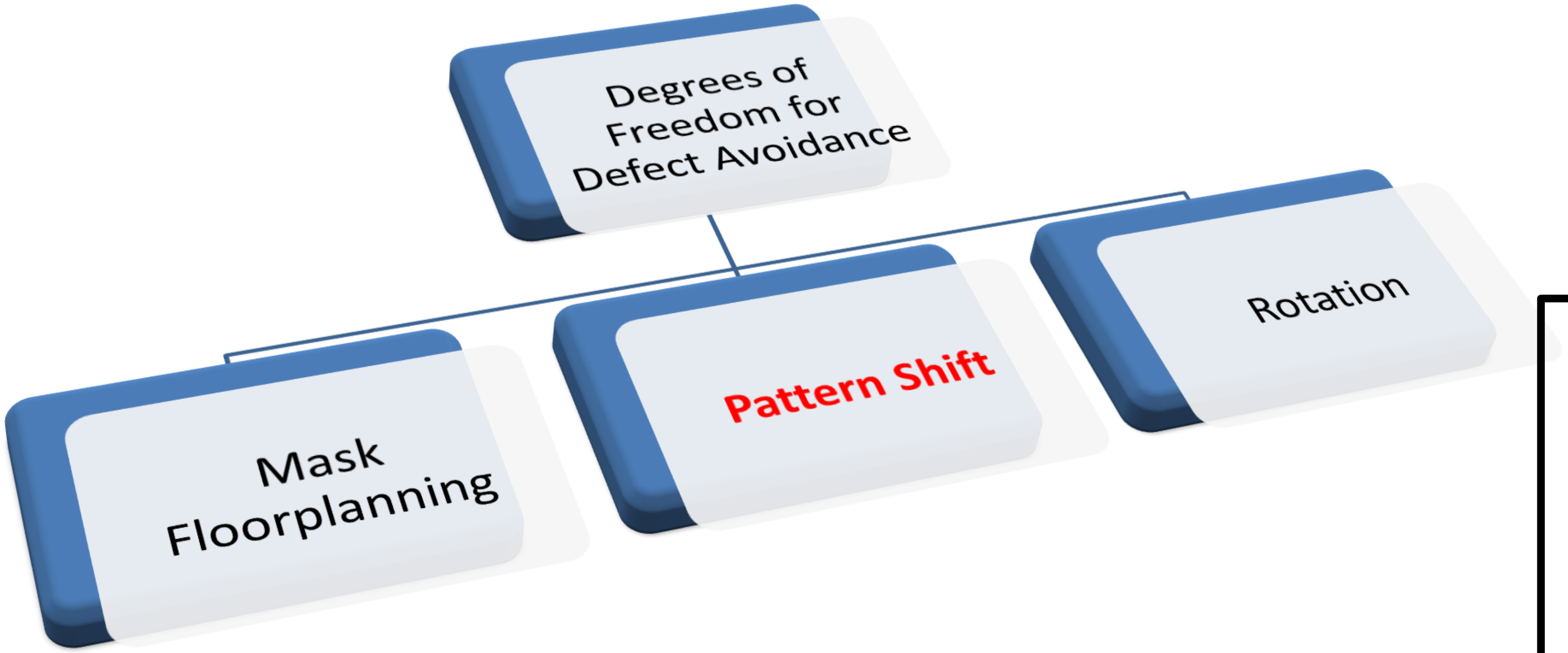


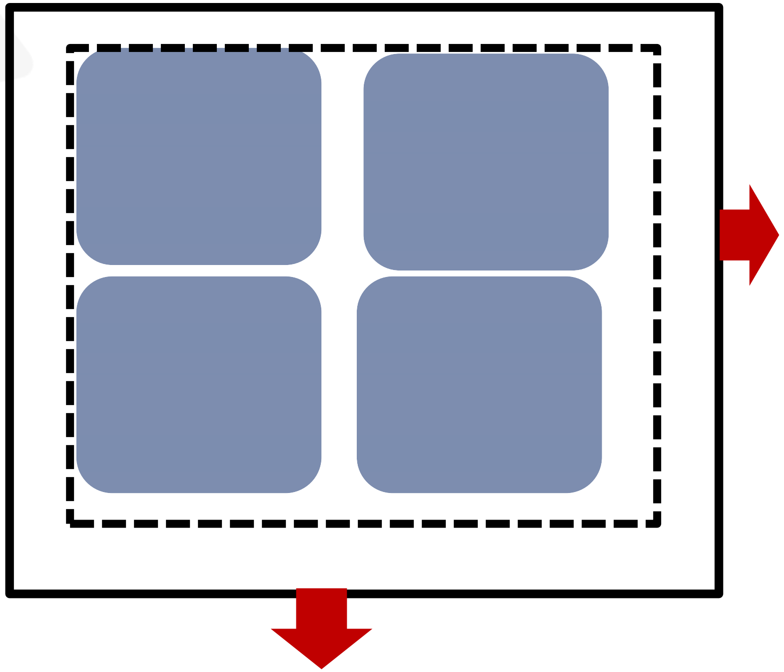
Alternate option is to place it away from any layout feature

Flexibility of Defect Avoidance Methods



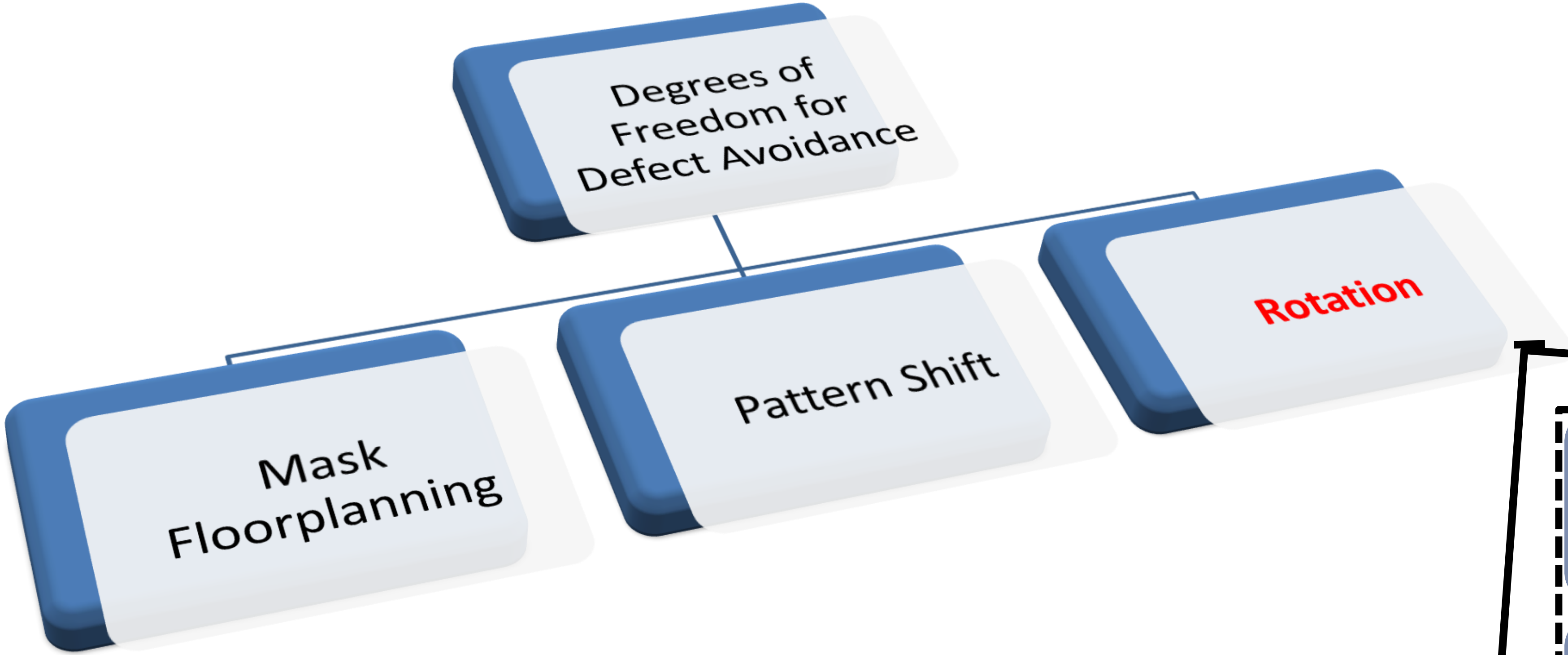
Flexibility of Defect Avoidance Methods: Pattern Shift

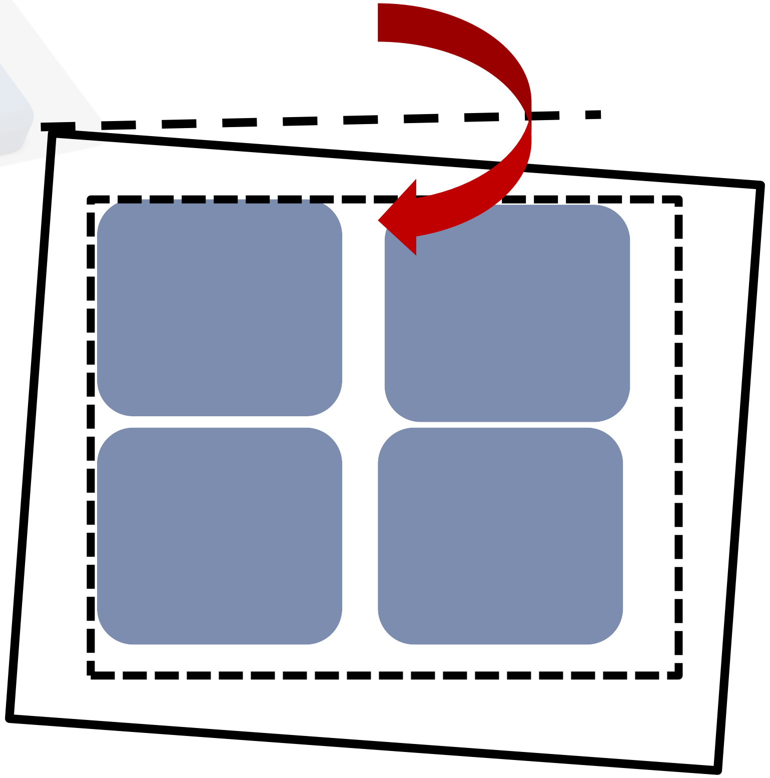




Move the entire mask blank (relative to mask pattern) in X-Y direction

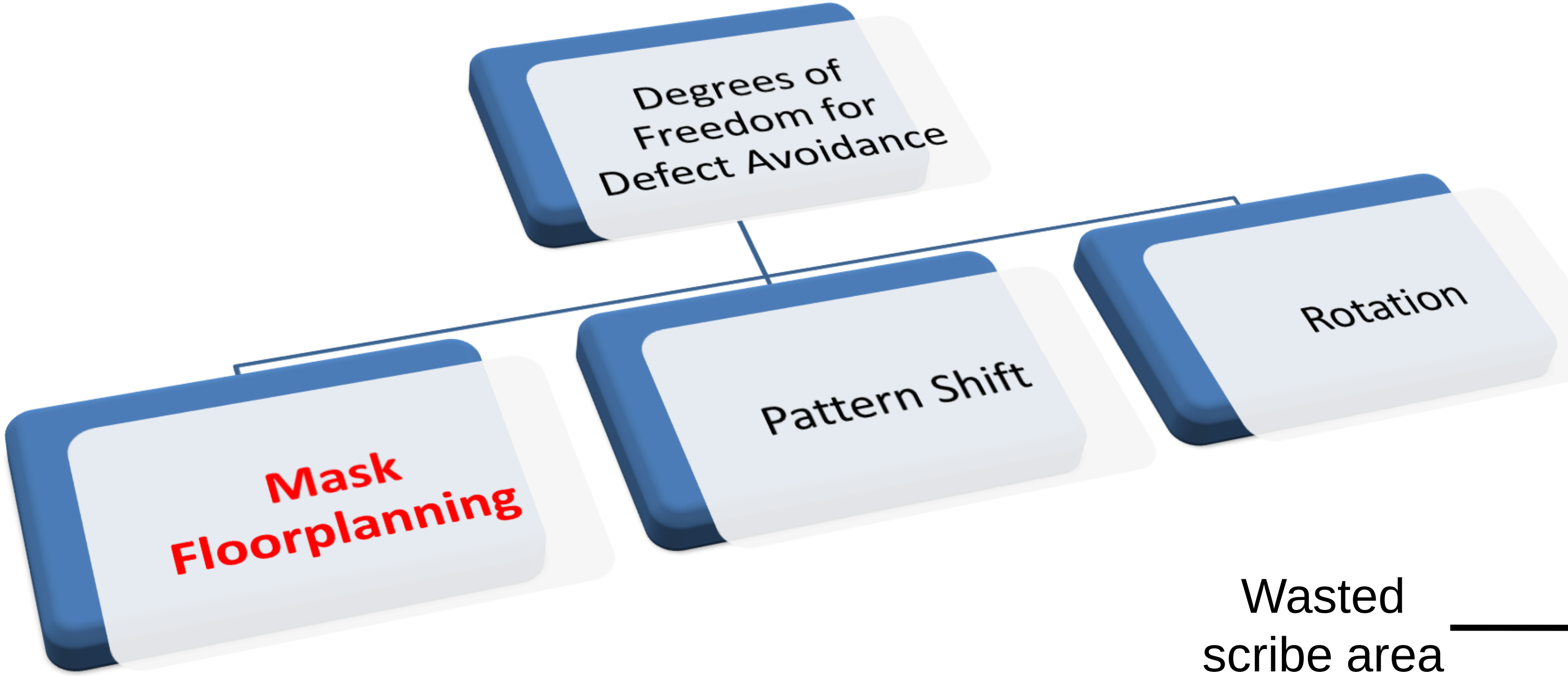
Categories of Defect Avoidance Methods: Rotation

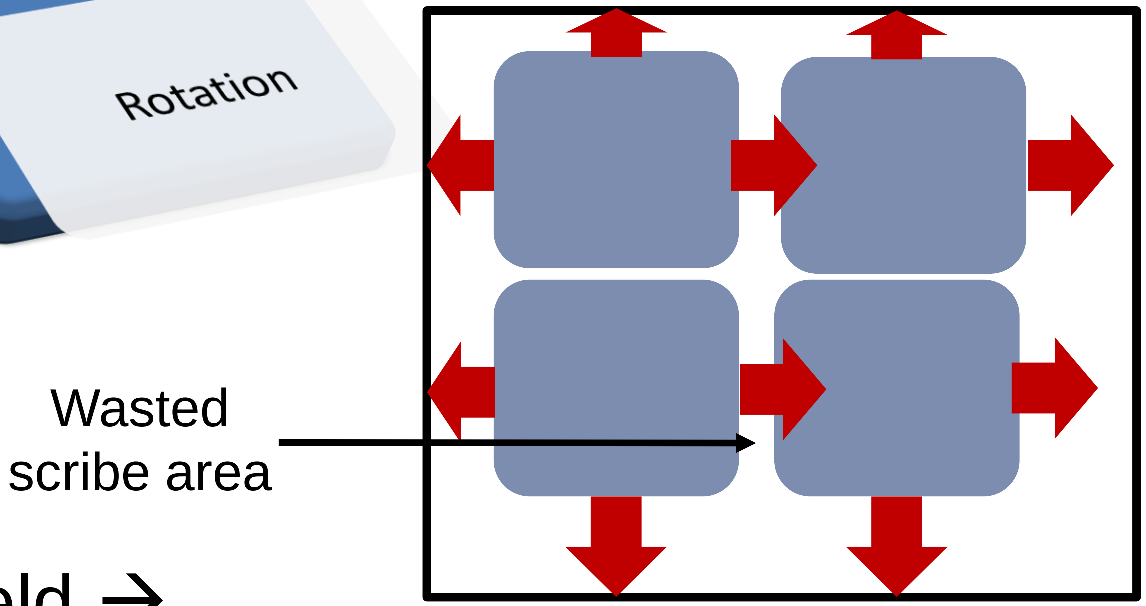




Rotate the mask blank (relative to mask pattern)

Flexibility of Defect Avoidance Methods: Mask Floorplanning





Move each die copy inside the mask field →
Different layers of same design must be moved together

Prior Defect Avoidance Methods

- Simulated Annealing Based Floorplanning [IEEE TSM'13]
  - Shift die copies in grid-line based on CD cost metric
  - Cannot handle arbitrary angle rotation
  - Makes discrete jumps instead of exploring continuous space
- Prohibited Region based Pattern Shift + Rotation [ASP-DAC'12, ICCAD'12, JVST'12]
  - Constructs prohibited rectangles and then finds minimum overlap location
  - Limited to small-angle rotation, cannot handle floorplanning
  - Prohibited rectangle construction pessimistic at corners of absorber
- **Need a method that can systematically explore all degrees of freedom for defect avoidance**

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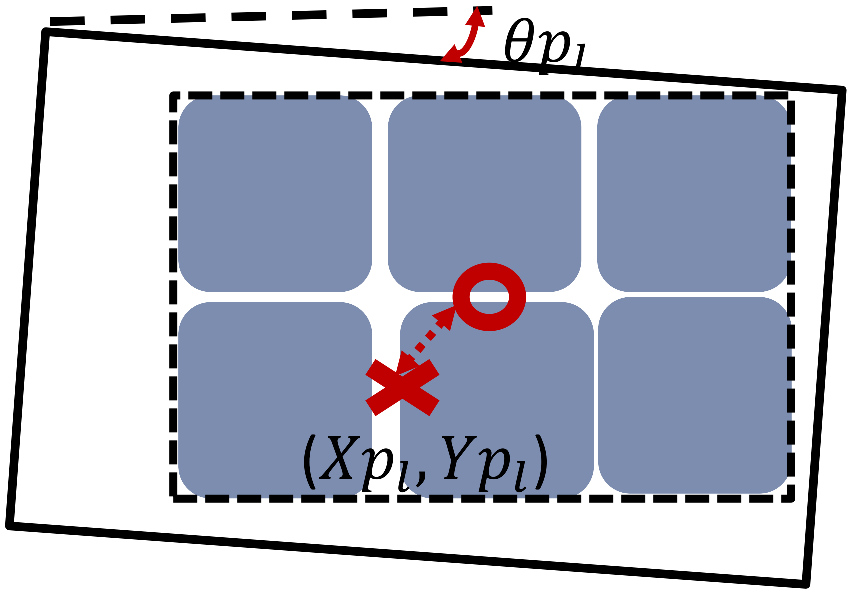
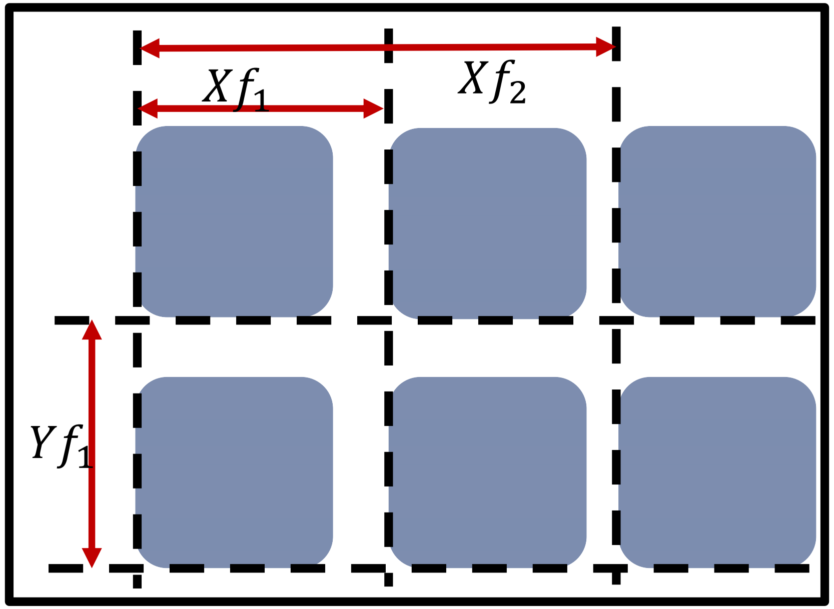
Problem Formulation: Pattern Shift and Rotation Optimization Variables

- For each EUV layer l of given design, define three variables: $Xp_l, Yp_l, \theta p_l$

- For each row (r) and column (c) relative to bottom left coordinate of field define Xf_c & Yf_r





Find the value of $Xp_l, Yp_l, \theta p_l, Xf_c$ & Yf_r such that CD impact of every defect-layout edge pair is less than CD tolerance

Spatial Constraints

1. Reticle Boundary Constraints → Entire mask pattern inside usable reticle area

$$\pm Xp_l \pm \frac{W_F}{2}\theta p_l \le \frac{W_M - W_F}{2}$$

$$\pm Yp_l \pm \frac{H_F}{2}\theta p_l \le \frac{H_M - H_F}{2}$$

2. Field Boundary Constraints → All die copies within field

$$Xf_{C-1} + W_D \le W_F \qquad Yf_{R-1} + H_D \le H_F$$

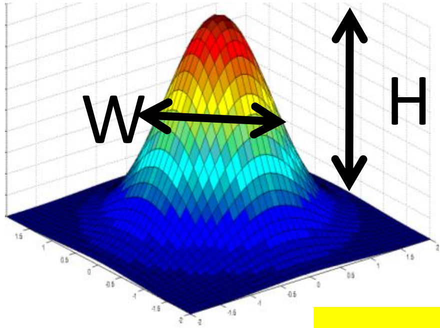
3. Die Overlap Constraints → Die copies must not overlap

$$Xf_c - Xf_{c-1} \ge W_D \qquad Yf_r - Yf_{r-1} \ge H_D$$

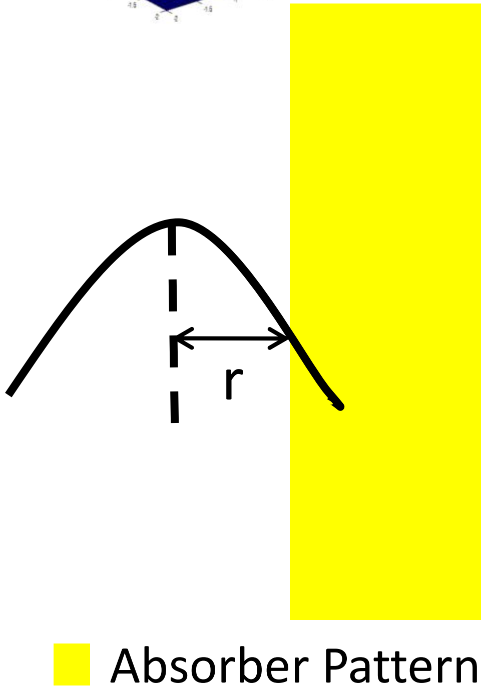
4. Maximum Rotation Constraint

$$\theta_{min} \le \theta p_l \le \theta_{max}$$

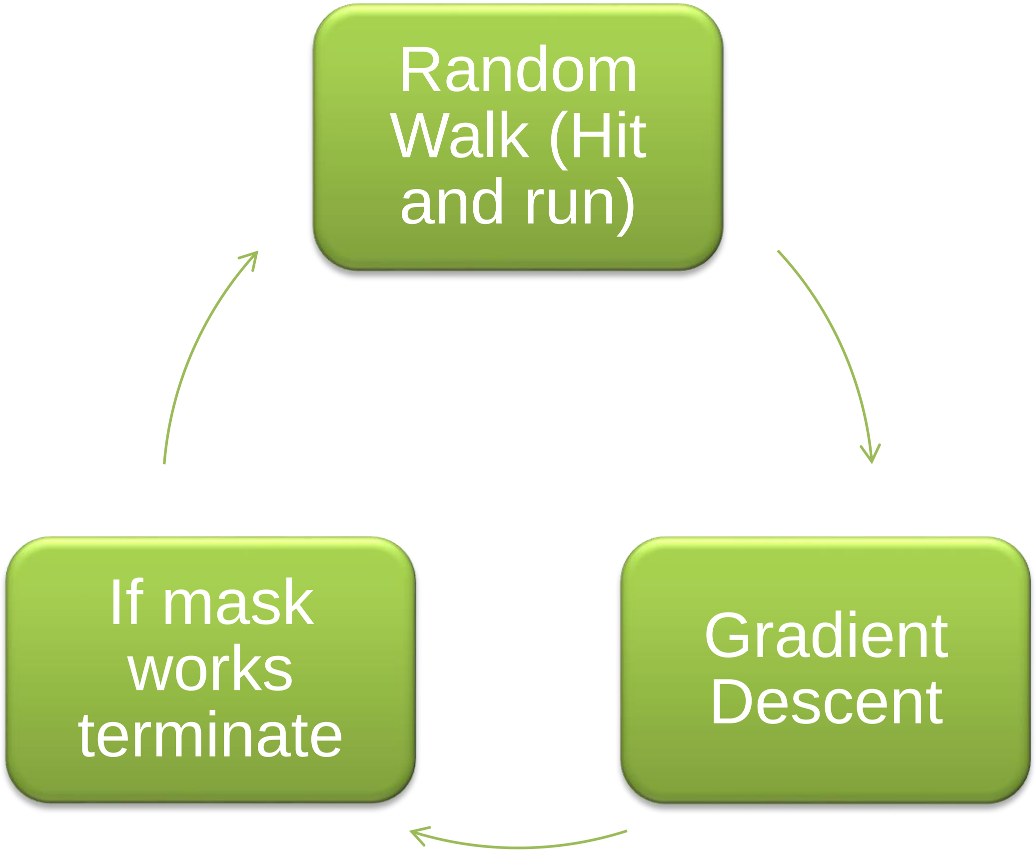
Modeling CD Impact of Defects

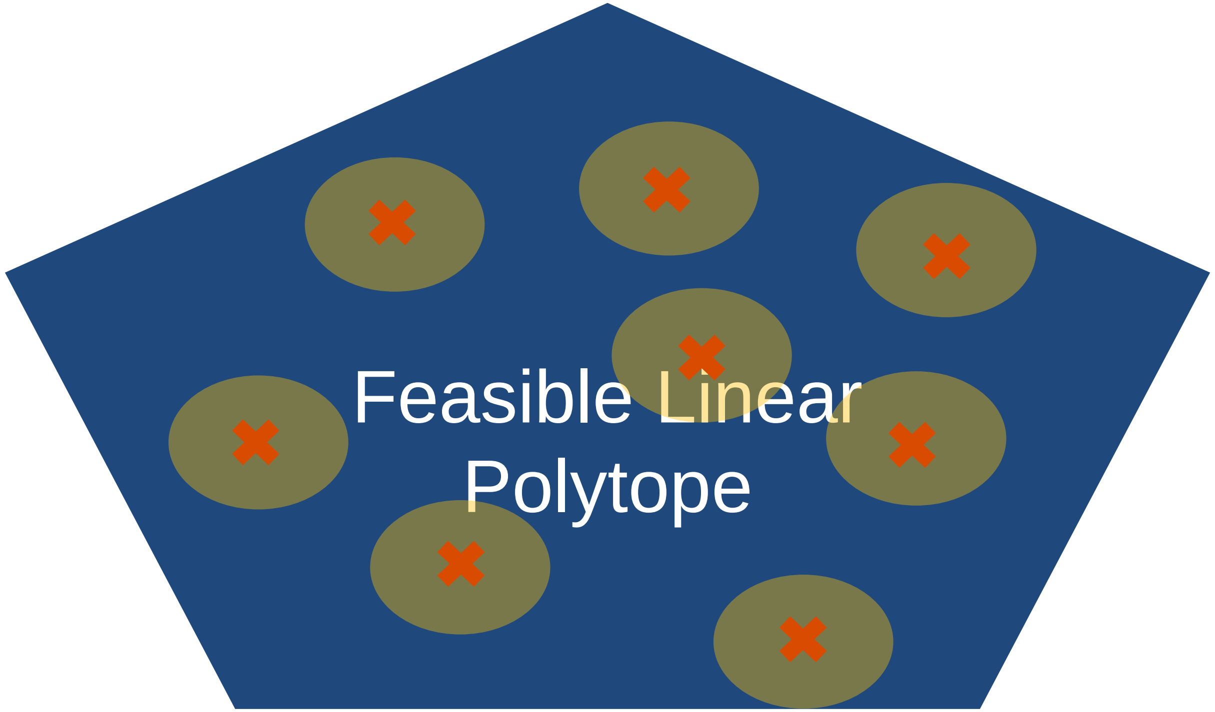


- Distance between defect & absorber edge(r) → $f(Xp_l, Yp_l, \theta p_l, Xf_c\ , Yf_r)$
- $\Delta CD = A\left(He^{-\frac{r^2}{(W/2)^2}} + B\right)$
  - Proposed by Clifford & Neureuther, SPIE 2007 for symmetric Gaussian defects
  - Proportional to defect height at absorber edge
  - 0.5X for absorber-covered defect
- Want $\Delta CD \leq \ CD_{tol}$ for every defect – layoutEdge pair
  – Non-convex constraint → Relax using sigmoid
- $Cost = \sum_{All\ defects} \sum_{All\ shape\ edges} sig(\Delta \mathrm{CD}\ -\ CD_{tol})$
  - Actually needs to be computed only for a small region around a defect



Global Optimization Method for Defect Avoidance

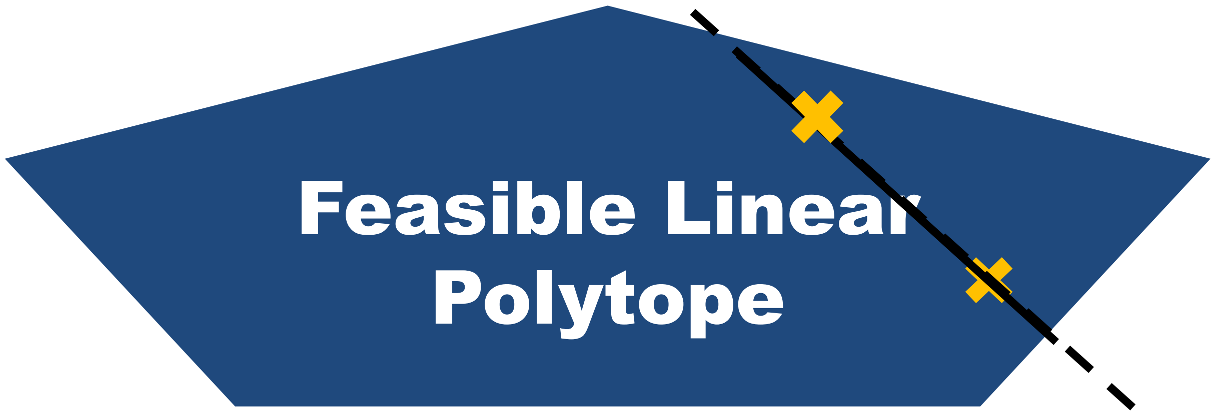




Combines global search (random point generation) with local search (gradient descent) to cover the feasible space for minimizing non-convex objective

Hit-and-Run based Random Walk

- Objective → Generate random starting points such that all spatial linear constraints are satisfied
- Hit-and-run based random walk → Uniformly samples linear polytope
  1. Draw line passing through current solution with random direction
  2. Find part of line inside the linear polytope
  3. Uniformly pick a random point on the line segment
- Given enough iterations entire linear polytope is covered



Computation of Gradient of CD Impact Cost Function

$$\widetilde{X_d} = X_d \cos(\theta p_l) - Y_d \sin(\theta p_l) - Xp_l$$
$$\widetilde{X_d} = X_d\, sin(\theta p_l) + Y_d \cos(\theta p_l) - Yp_l$$
$$Xf_e = Xf_c + X_e$$
$$Yf_e = Yf_r + Y_e$$
$$Z = \frac{\partial\,(Cost)}{\partial\,(r^2)}$$

$$\frac{\partial\,(Cost)}{\partial Xp_l} = -2Z\,(\widetilde{X_d} - Xf_e)$$
$$\frac{\partial\,(Cost)}{\partial Yp_l} = -2Z\,(\widetilde{Y_d} - Yf_e)$$
$$\frac{\partial\,(Cost)}{\partial \theta p_l} = -2Z\,(X_d \sin(\theta p_l) + Y_d \cos(\theta p_l))$$
$$\frac{\partial\,(Cost)}{\partial Xf_c} = -2Z\,(\widetilde{X_d} - Xf_e)$$
$$\frac{\partial\,(Cost)}{\partial Yf_r} = -2Z\,(\widetilde{Y_d} - Yf_e)$$

- Must be aggregated over all relevant defect absorber edge pairs
- Runtime dominated by layout query of shapes around each defect
- Upfront store all shapes close to defect before each round of gradient descent

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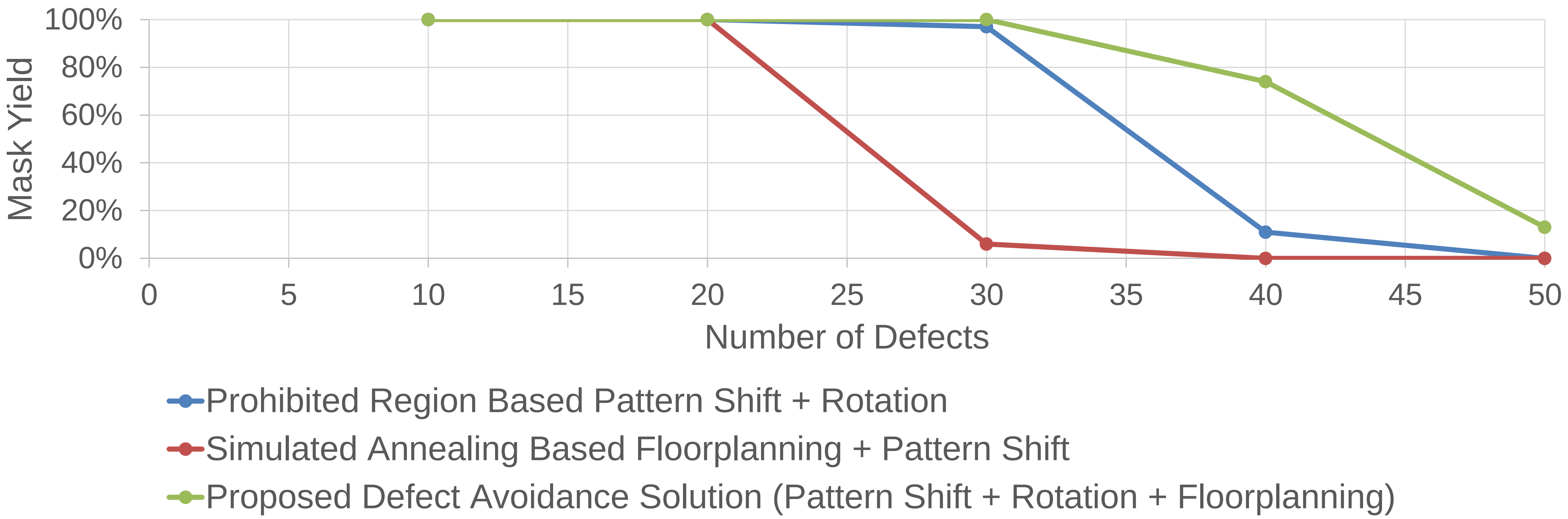
Experimental Setup

- Method implemented in C++ using OpenAccess and Boost Polygon APIs
- Testcase Layout → ARM Cortex M0 synthesized, placed and routed using Synopsys 32nm Library (Scaled to 8nm technology node)
- 100 randomly generated Gaussian defect maps with each defect of height 2nm and full width half maximum 50nm
- Mask Yield → Percentage of defect maps that are completely fixed
- Allowed degrees of freedom: Maximum pattern shift 20µm, maximum scribe area 1%, maximum rotation angle 6^o

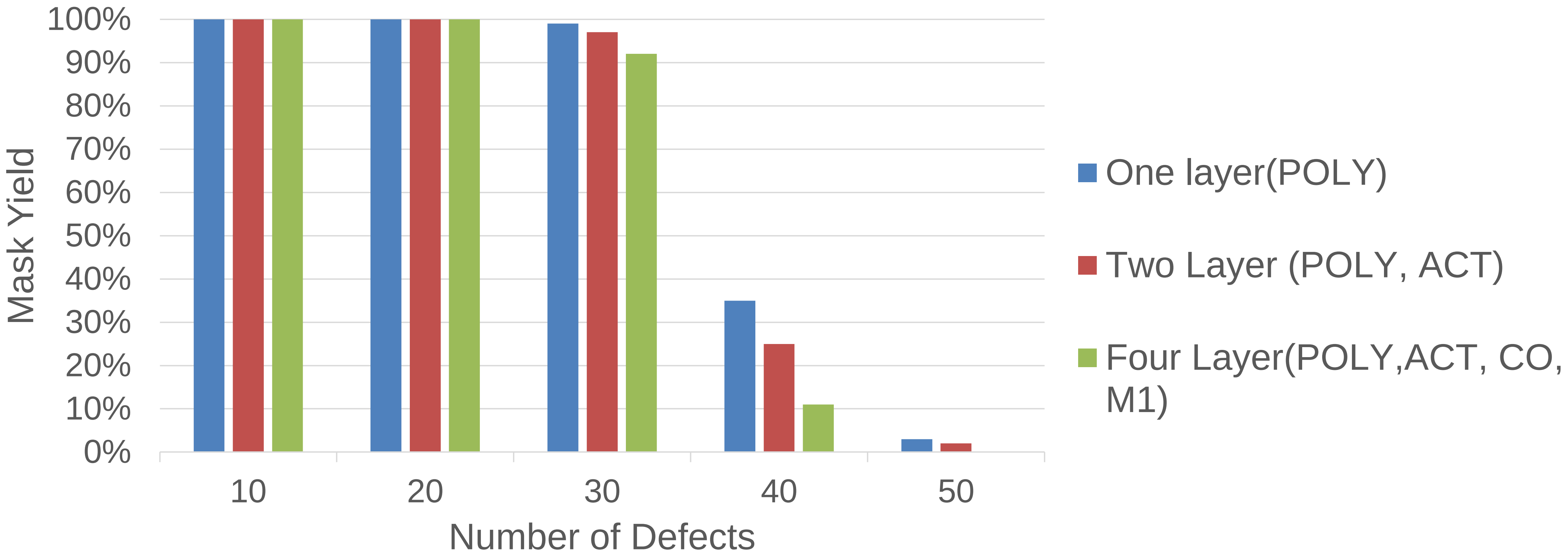
Comparison with Prior Methods for Polysilicon Layer

- Significantly better than simulated annealing due to small angle rotation and continuous move instead of discrete jumps
- More than 2X better mask yield than prohibited region based method due to floorplanning and lack of pessimism of prohibited region construction



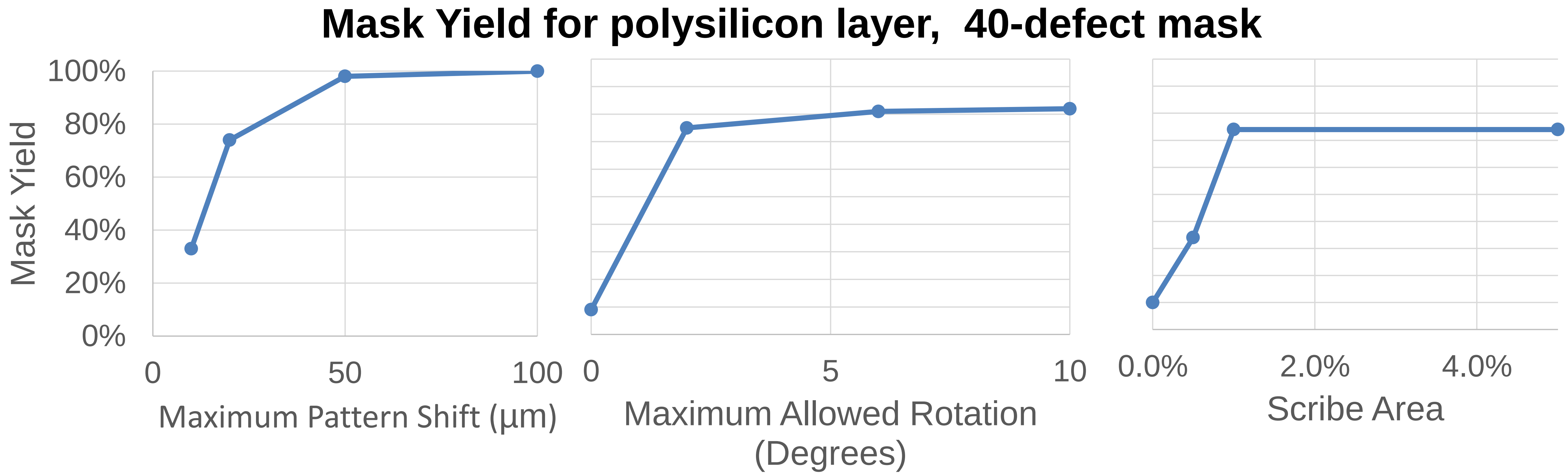
Impact of Multiple Layer

- Mask yield defined as percentage of cases when masks of all the given layers work
- Yield limited mainly by polysilicon layer → Regularity of polysilicon layer makes it mask yield limiting



Comparing Degrees of Freedom for Defect Avoidance

- Maximum pattern shift the most important spatial constraint for improving mask yield
- Benefit from rotation and floorplanning tapers off beyond a certain value



Conclusions

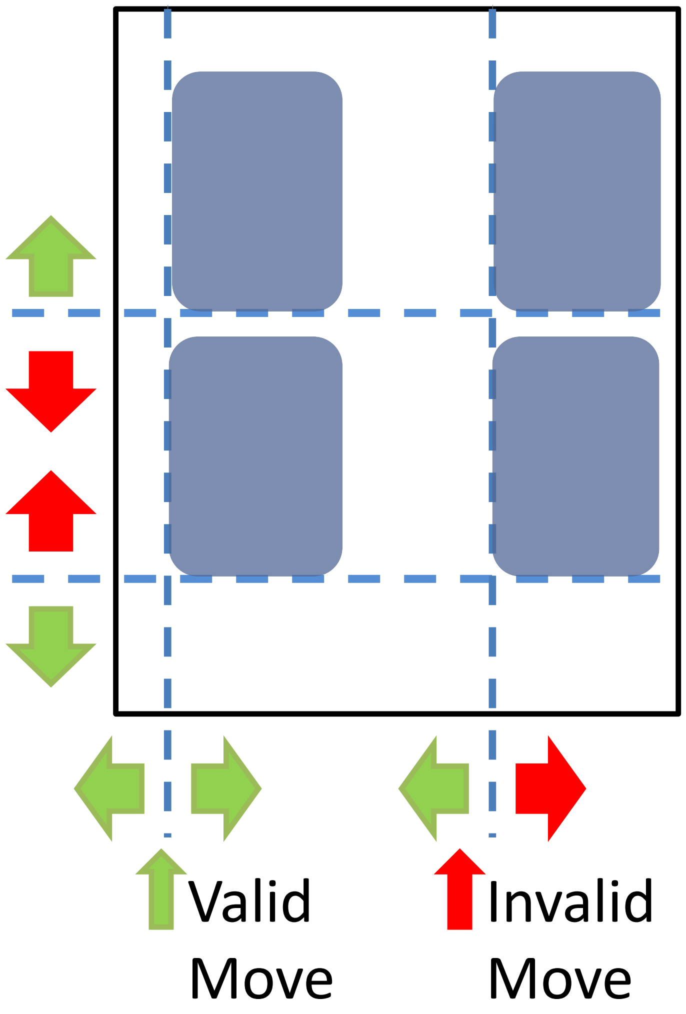
- Novel EUV mask defect avoidance method
  - Can simultaneously handle pattern shift, rotation and floorplanning
  - Method allows continuous shifts and arbitrary angle rotation
- Formulated as a non-convex optimization problem and solved using a combination of random search and gradient descent
  - Hit-and-run based random walk to handle spatial constraints
- More than 60%-point better mask yield compared to prior work for 40-defect mask, polysilicon layer of 8nm ARM Cortex M0 layout

QUESTIONS

Backup Slides

Prior Work → Simulated Annealing Based Mask Floorplanning and Pattern Shift [TSM'13]

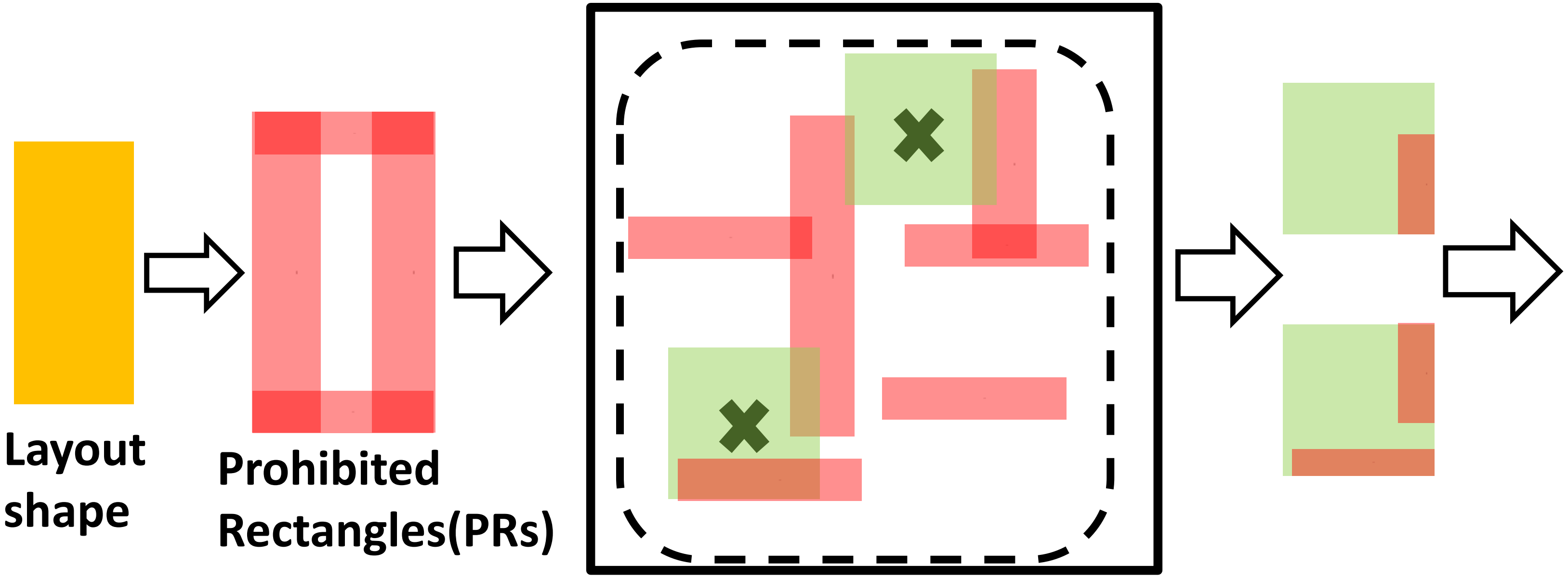
- Define grid-line moves which move the connected dies in small steps
  - Valid moves → Dies don't overlap
  - Invalid moves → Dies overlap
- Compute cost for each potential valid move
- Choose a valid move based on simulated annealing criteria



<u>Limitations</u>

- Cannot handle arbitrary angle rotation
- Exploring continuous space with discrete jumps is computationally expensive

Prior Work → Prohibited Region Based Pattern Shift + Rotation



Prof. Martin Wong (UIUC)
[ASP-DAC’12, ICCAD’12]
Overlap PR clips + find minimum overlap location

IBM (Wagner et. al.)
[JVST’12]
Merge PRs + Boolean OR of clips + Find empty region

- Rotation → For each potential rotation angle, rotate defects and repeat pattern shift [ICCAD’12]
  - Only small angle rotation, discretization of continuous angle values
- Hard to handle mask floorplanning with this approach
- Prohibited region construction is pessimistic at shape corners
  - CD impact of defect depends on Euclidean distance from shape edge

Gradient Descent Speedup

- Runtime for computing gradient dominated by layout query for shapes that are close to defects
- But gradient descent only makes small moves
- At each random start, store all shapes within distance D from defect center for each defect
  - D = 3*defectWidth + numGradientIterations*gradientStepSize