EUV-CDA: Pattern Shift Aware Critical Density Analysis for EUV Mask Layouts

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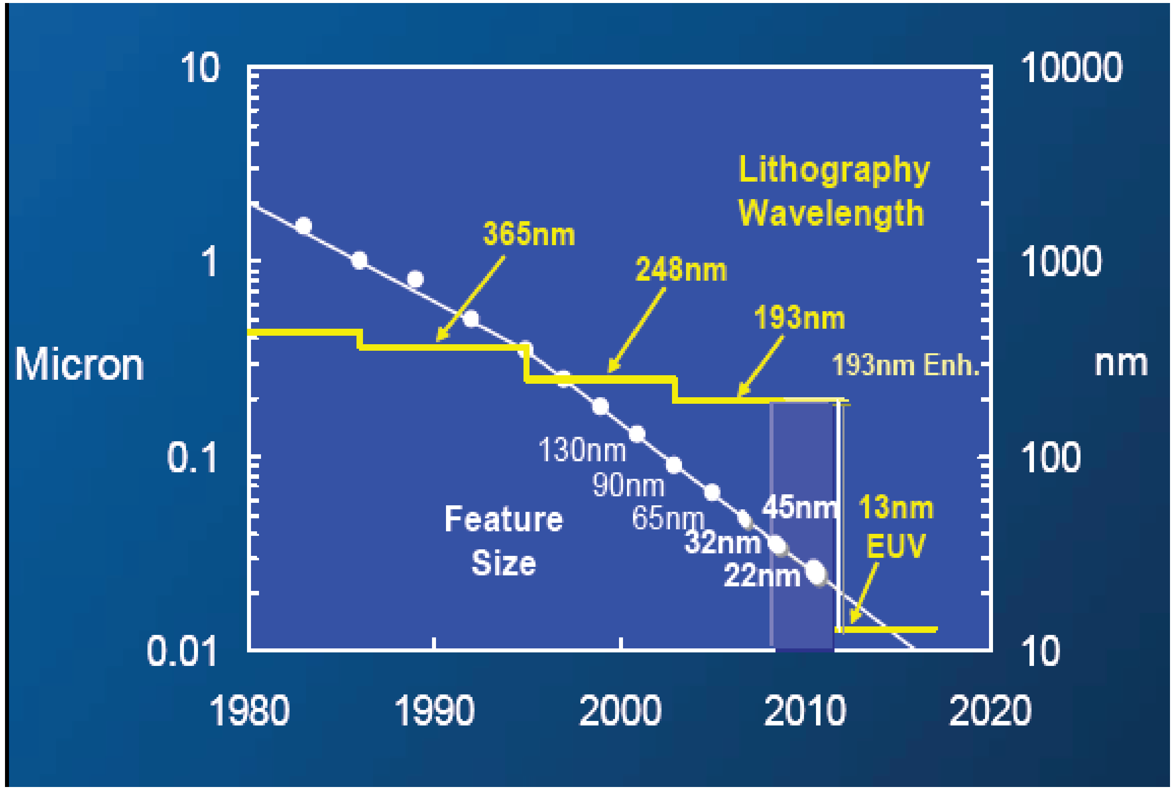
Mentor Graphics

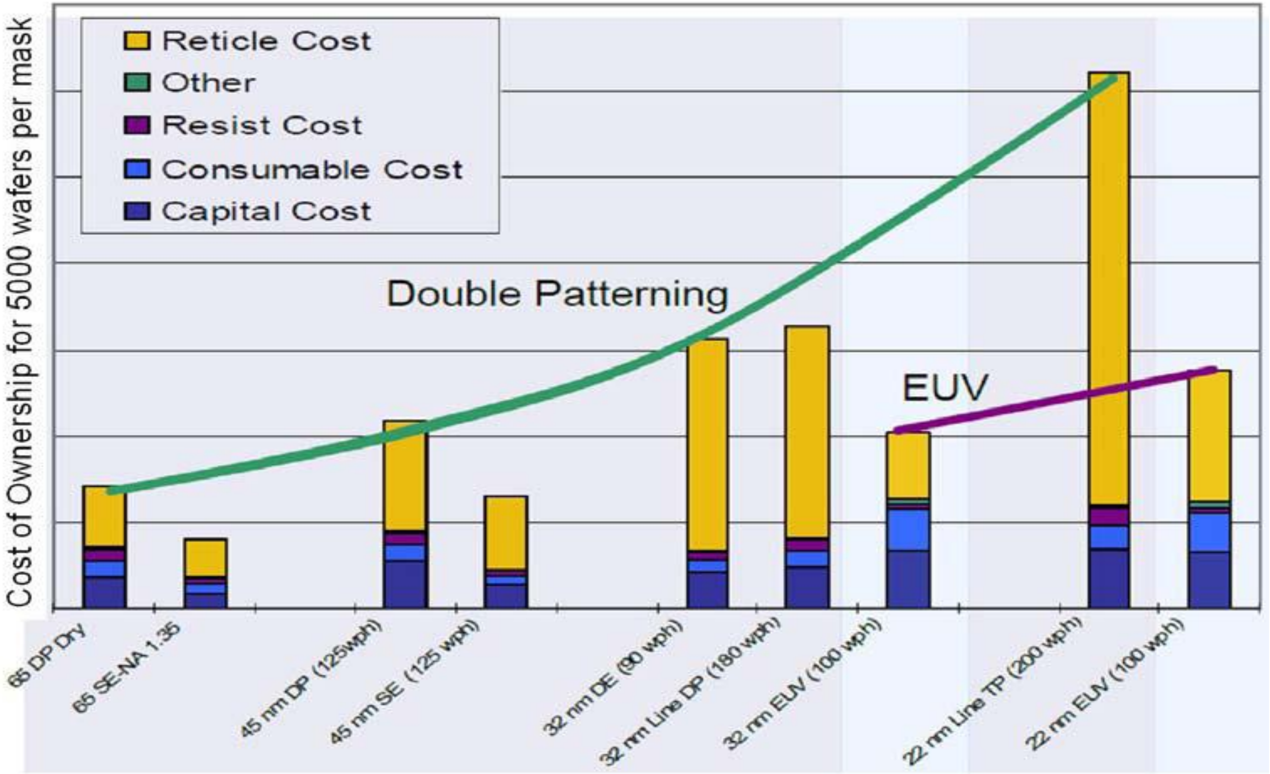
Outline

- **Introduction to EUV Mask Defect and their Mitigation**
- Proposed Mask Yield Estimation Methods
- Experimental Results

Need for EUV Lithography



Source: Intel

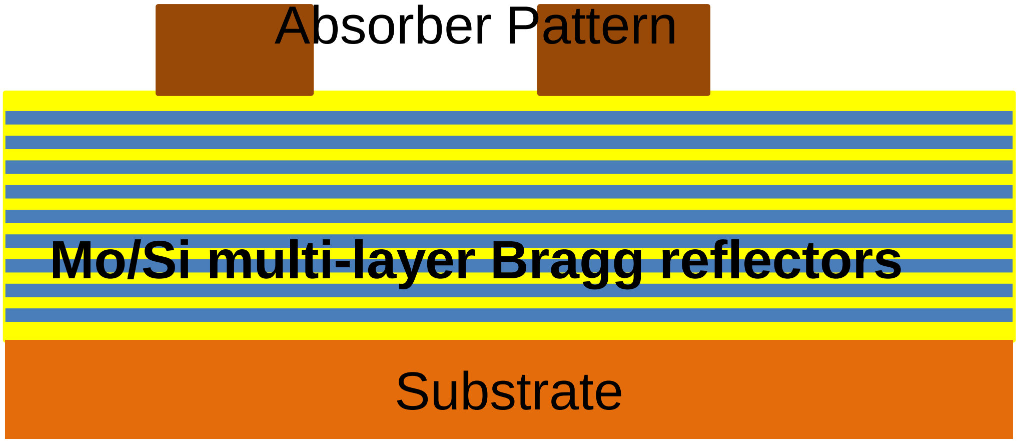


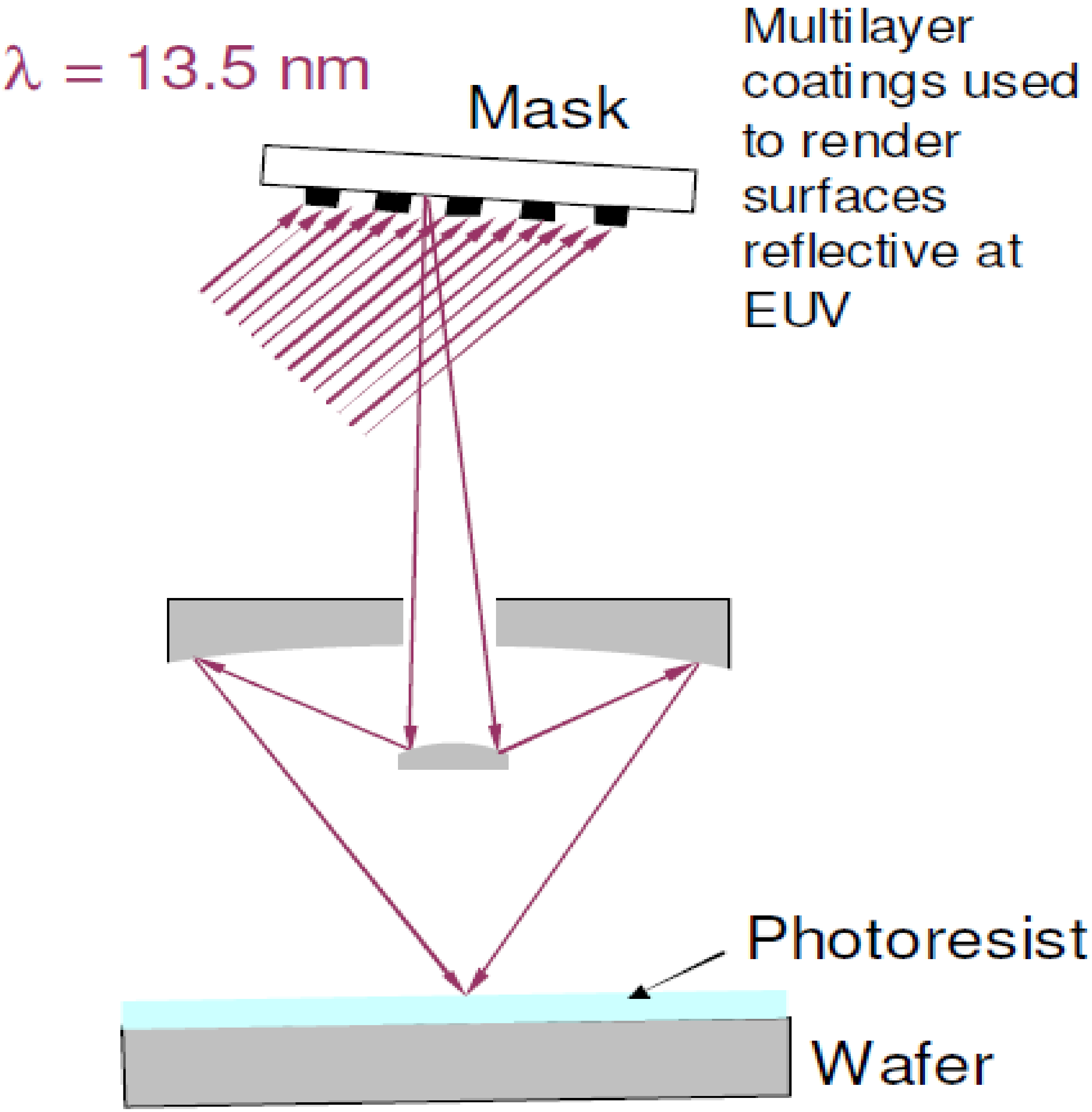
Source: ITRS 2009

- EUV Lithography 193nm → 13.5nm transition
  - Enables several generations of scaling
  - More cost effective compared to multiple patterning

Reflective EUV Masks

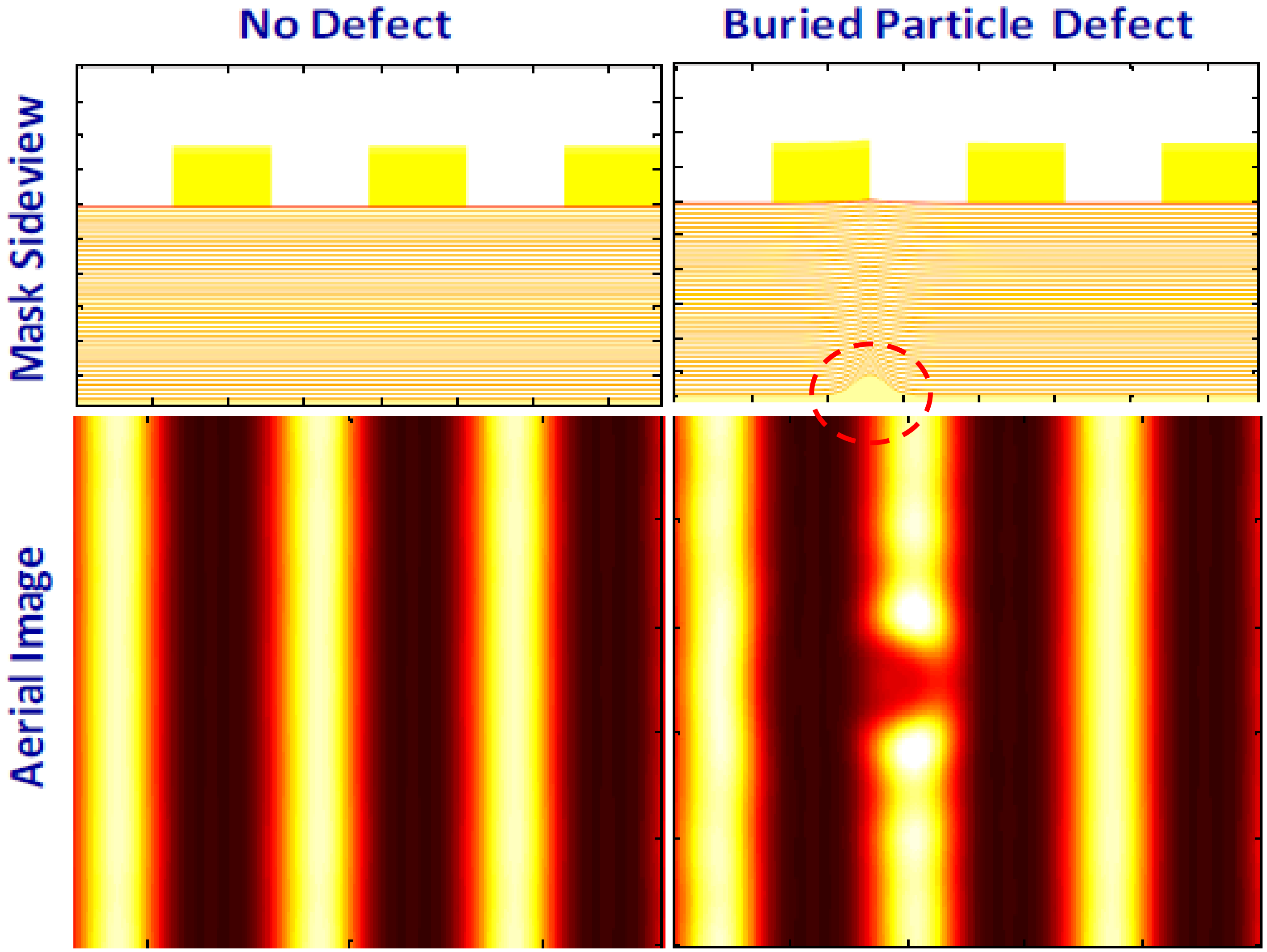
- Reflective optics since all materials absorb 13.5nm light
- Masks blanks are multi-layer Bragg reflectors





Source: Naulleau, SPIE tutorial, 2011

EUV Mask Blank Defects

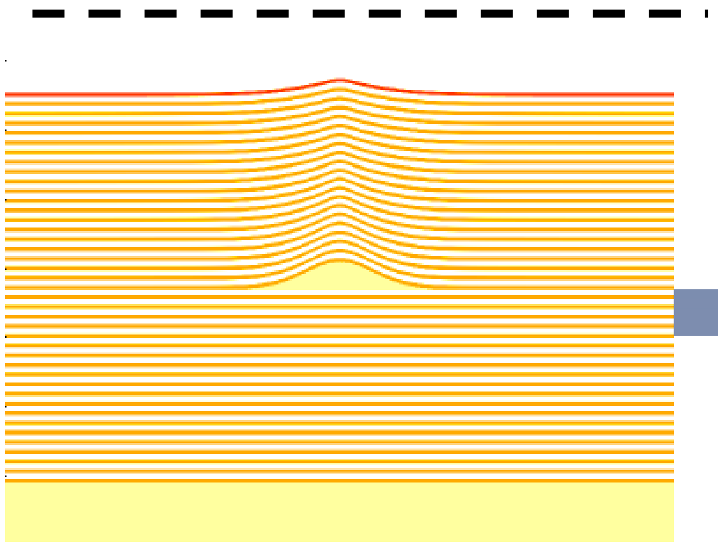


Source: Clifford and Neureutheur, SPIE 2010

- **3.5nm high defect can cause 20nm CD change**
- Caused mainly due to substrate imperfections
- Current defectivity level of 10-50 defects per mask of size > 50nm
- Many defects missed by inspection tool
- Repair expensive

Defect Avoidance Based EUV Mask Defect Mitigation

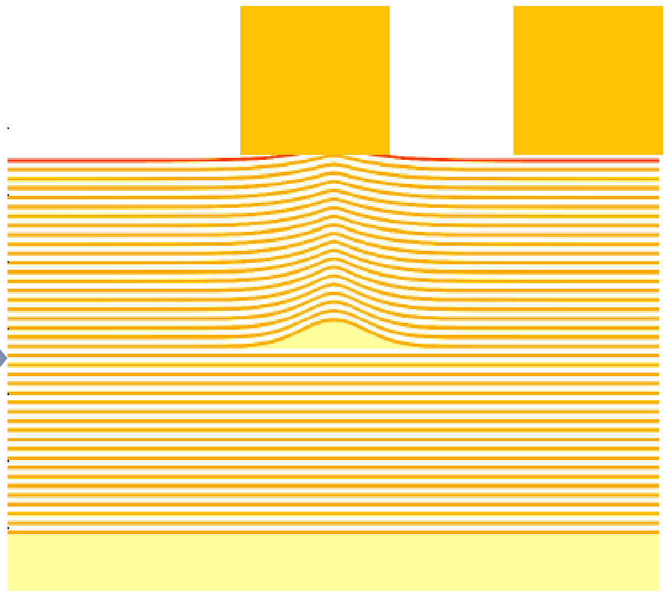
Layout Pattern (Not yet written on mask blank)



Mask Blank with buried defect

Mask Inspection → Defect Avoidance → Mask Write

Defect covered by absorber

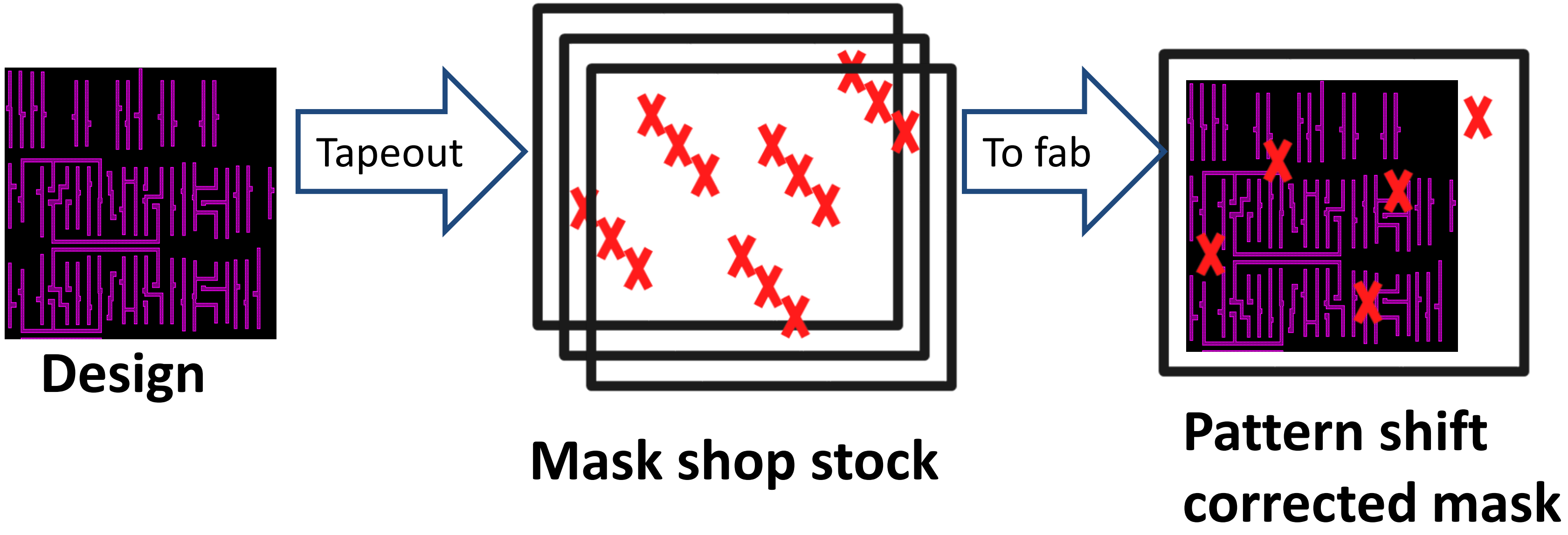


Alternate option is to place it away from any layout feature

EUV Mask Defect Mitigation Strategies

- Defect avoidance based defect mitigation
  - **Pattern shift** → Move entire mask pattern
  - Floorplanning → Each die copy inside field moves separately
  - Rotation → Small angle rotation, 90-180 degree rotation
- Pattern shift most popular approach due to ease of integration into current flows.
- Alternate defect mitigation strategy involves etching mask features after mask write
- **Sub-10nm dense layouts with tight CD tolerance → Defect avoidance techniques insufficient**

Can Circuit Designers help Mitigate Mask Defects ?



- Can designers construct robust EUV layouts ?
- Layout Robustness Metric → Probability of finding defective mask blank that can be safely used (Mask Yield)
  - Mask defect distribution statistics given
  - Resembles critical area analysis for wafer defects

Distinction Between Mask Yield and Wafer Yield

Wafer Yield	Mask Yield
Analyzes the impact of wafer defects	Analyzes the impact of mask defects
Defect location not known during design	Defect location not known during design
Defect location is unknown before wafer patterning	**Defect location known before mask patterning → Can shift layout to avoid defects before mask patterning**

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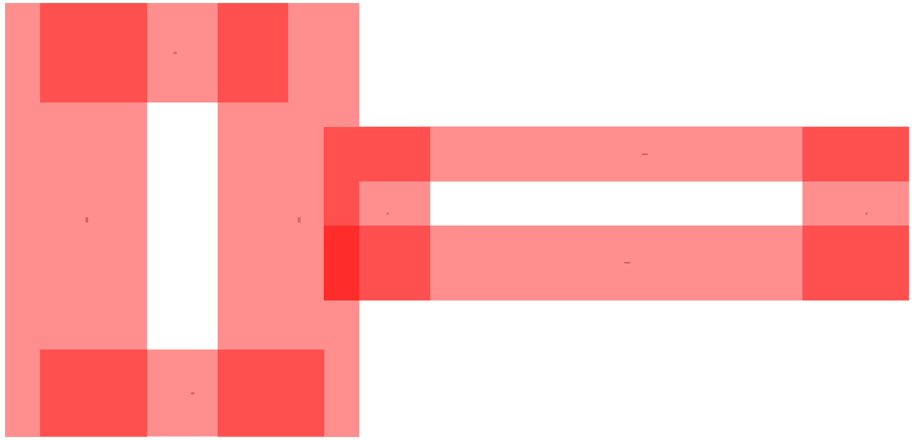
- **Proposed Mask Yield Estimation Methods**
- Experimental Results

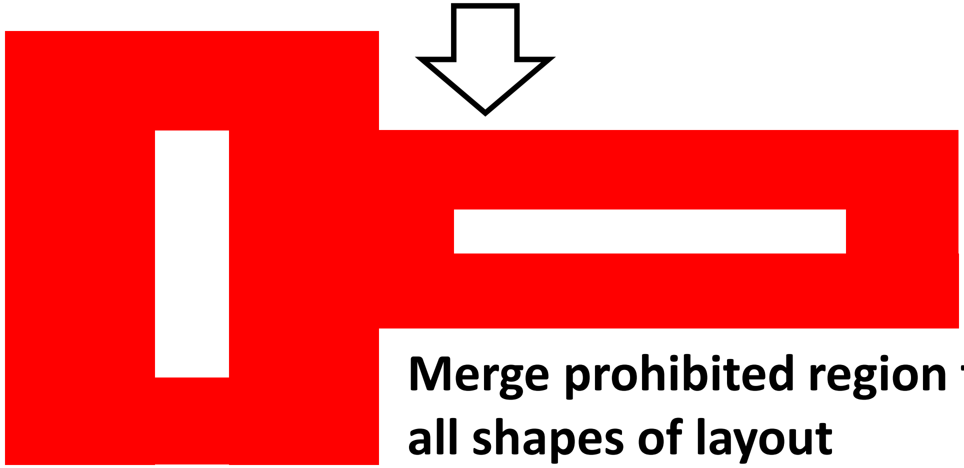
Prohibited Region Construction

Sample layout shapes (absorber patterns)



Draw prohibited region for each absorber shape

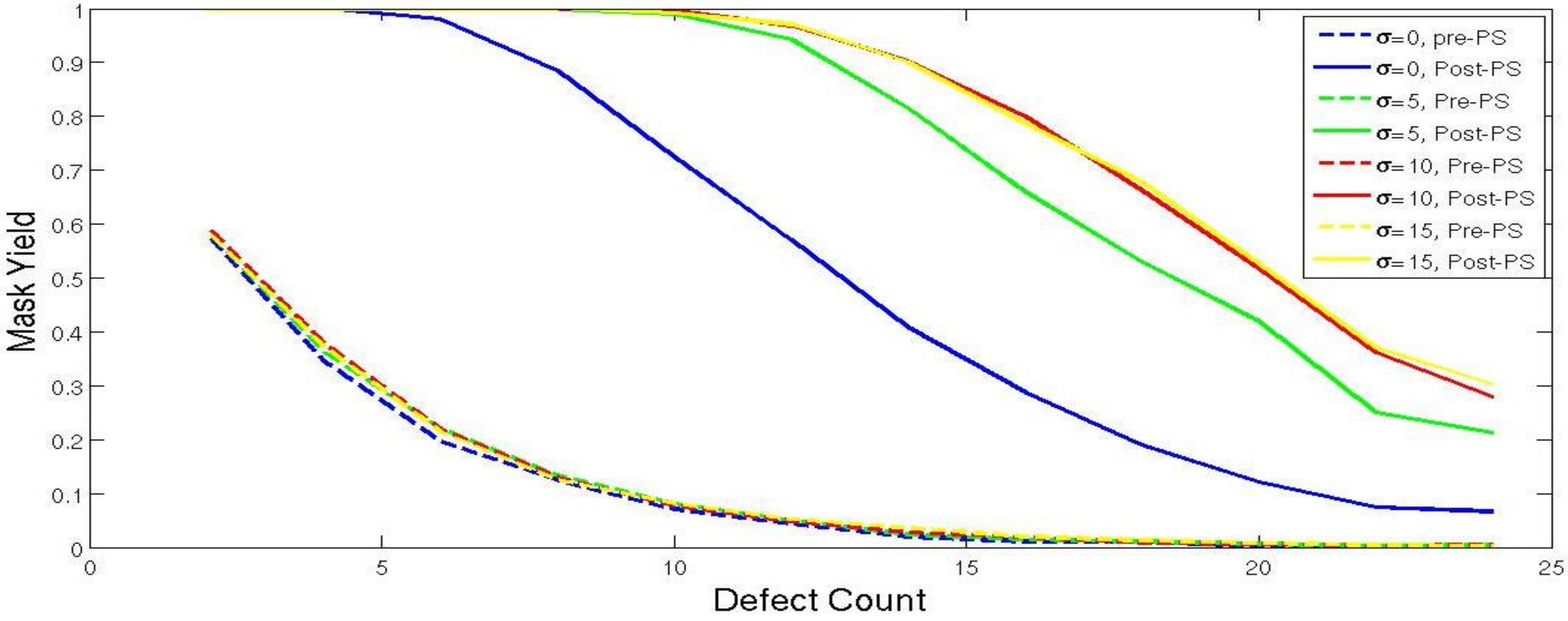
- Abstract 3D Gaussian-shaped defects to point defects
  - Based on linear model [Clifford et. al., 2008]
- Similar to construction of critical area for open/shorts in critical area analysis for wafer yield



Merge prohibited region for all shapes of layout

Are "Critical Area" like Methods Good Enough to Estimate Mask Yield ?

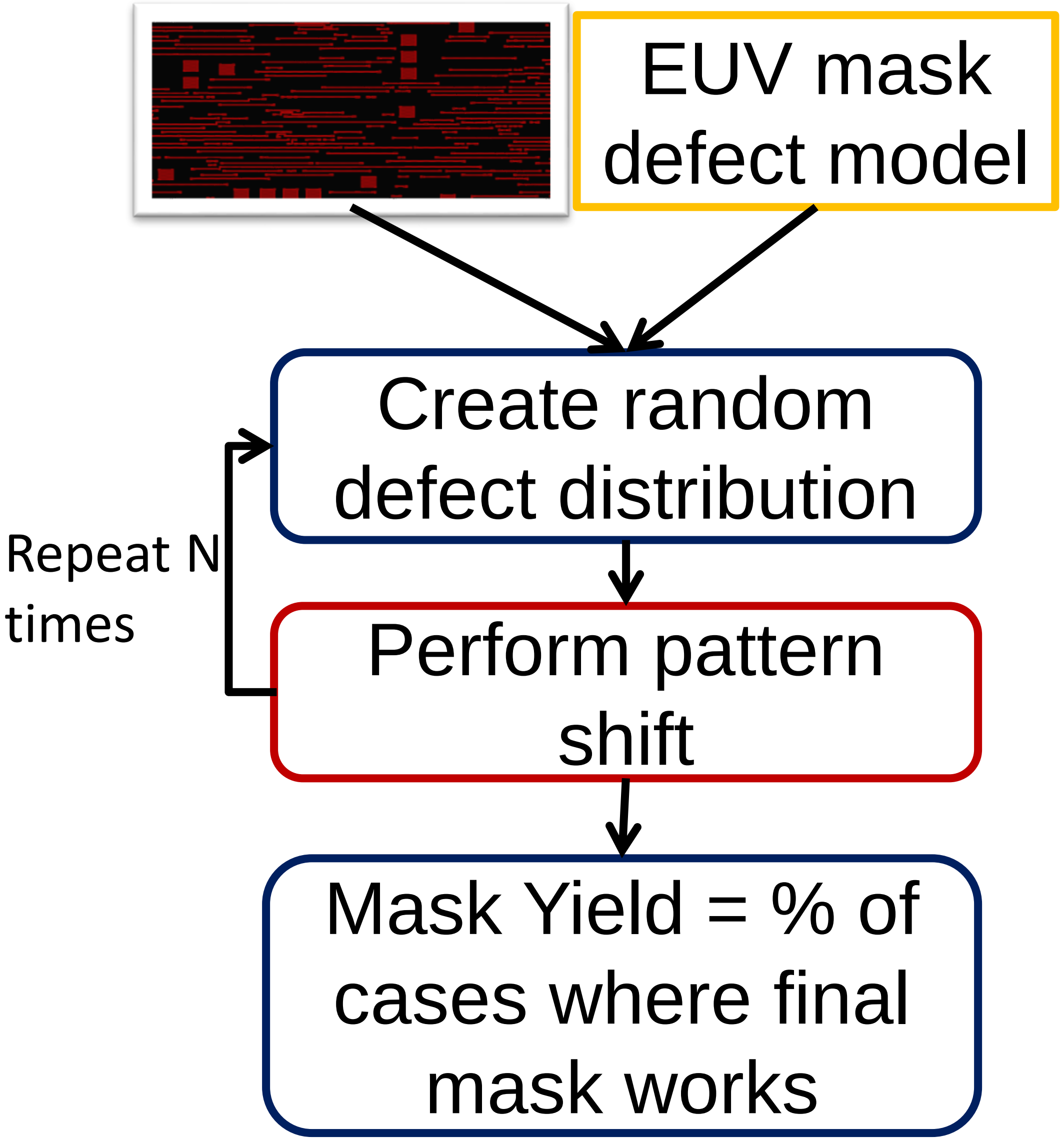
- Parallel line layouts → Same pitch & mean width (→ Same critical area), different width variation



- Post pattern shift mask yield significantly different despite same prohibited region density → Layouts with more variation (higher σ) have better mask yield

Golden Monte Carlo Method

- Naïve, rigorous method to estimate mask yield
- Cannot be used for realistic full chip layout analysis
  - Extremely slow, many iterations to converge
  - No design insight
- Useful as a method for validating accuracy of approximate methods



Hierarchy of Proposed Approximate Methods for Estimating Mask Yield

Inclusion-Exclusion Method

- Key assumption → Pattern shift is discrete
- Works for random layout shapes
- Defect size distribution can be easily handled

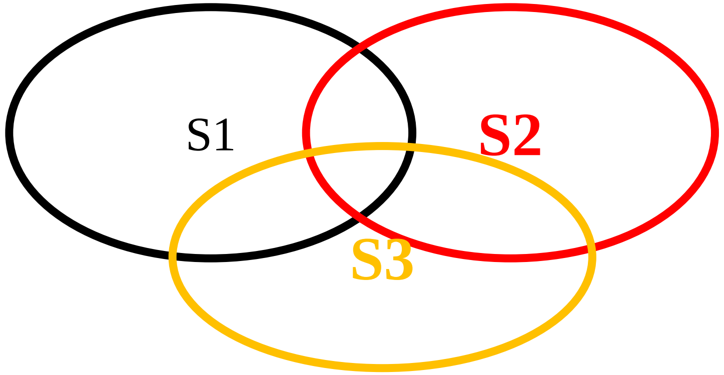
Spacings Method

- Key assumption → Layout is regular and infinite
- Pattern shift is continuous
- Simple analytical expression, easy to compute

Overall EUV-CDA Method

Inclusion Exclusion Method

- Suppose pattern shift selects one solution from several discrete shift options, $S_i\,, i \in \{1, 2, \ldots N\}$



Mask ok if one of these works

$$Mask\ Yield = \sum P(S_i) - \sum P(S_i \cap S_j) + \ldots$$

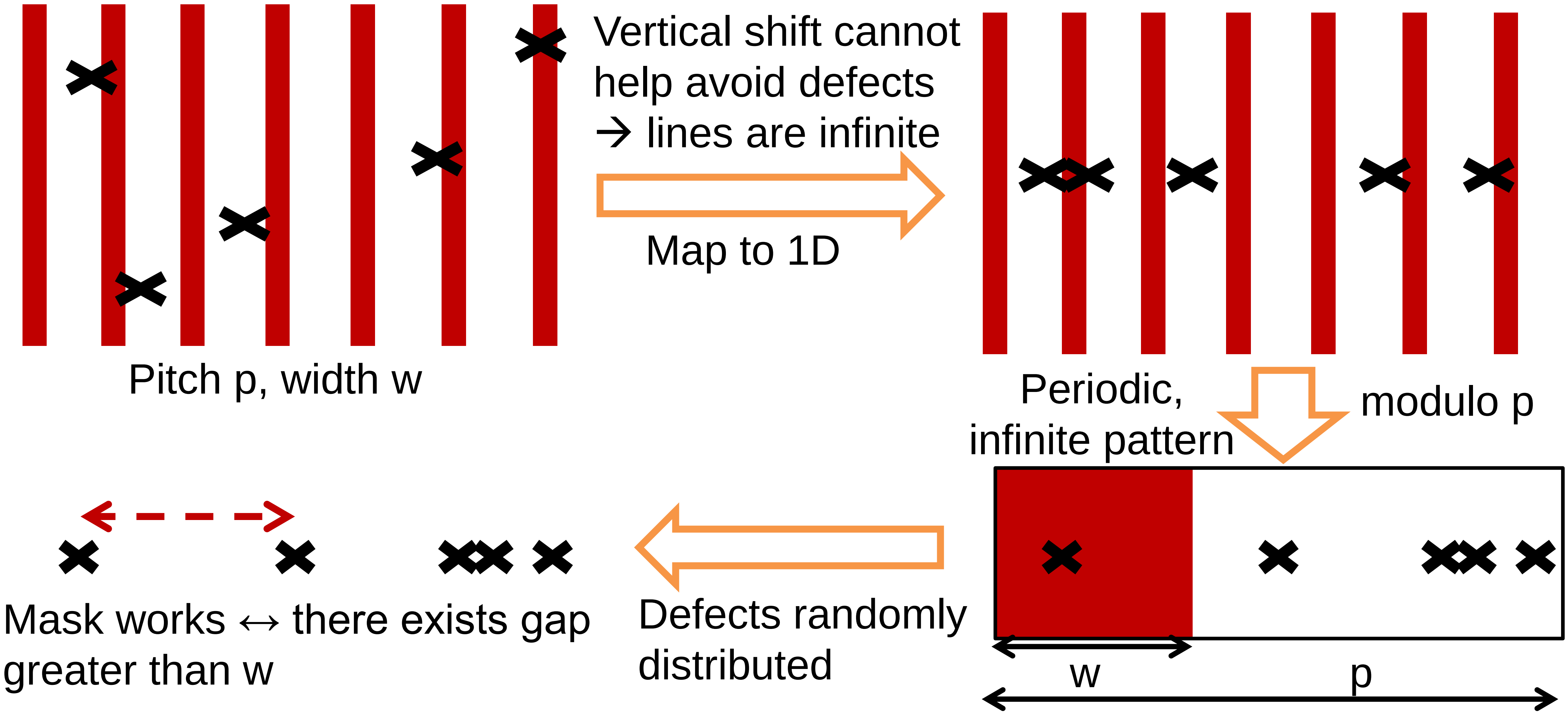
2^N terms

Prohibited Region Density

Density of Boolean AND of shifted layout copies → Autocorrelation

- Method is intractable due to large value of N
- But key insight is that **layout autocorrelation affects mask yield**

Spacings Method: Pattern Shift Aware Mask Yield Estimation for Regular Layout



Spacings Method: Analytical Mask Yield Estimation for Regular Layouts

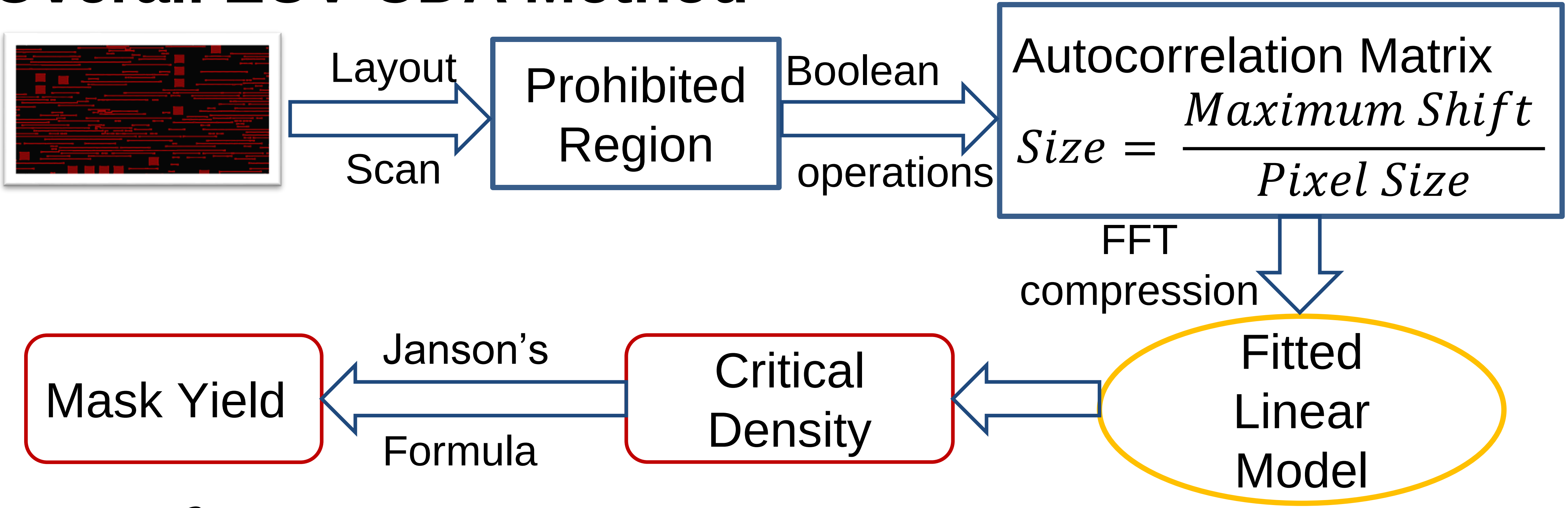
- Pattern shift aware mask yield of contact array layout ↔ Probability that maximum gap between point defects is greater than contact size
- If spatial defect distribution is uniform with N defects and prohibited region density P

$$Y = 1 - e^{-N^2 P e^{-NP}} \quad if\ N \geq \frac{2}{P}$$
$$= 1 \quad otherwise$$

Jansen's Formula

- No analytic expression for non-periodic layouts
  - Critical density → Value of P that allows estimating yield using Jansen's formula
  - Mask yield strongly correlated to layout autocorrelation

Overall EUV-CDA Method



- $O(Size^2 * L\log(L))$ due to the complexity of autocorrelation matrix construction
- Fitted linear model estimates critical density
  - Fitted using 5µm layout clips from polysilicon, active, contact and M1 layers

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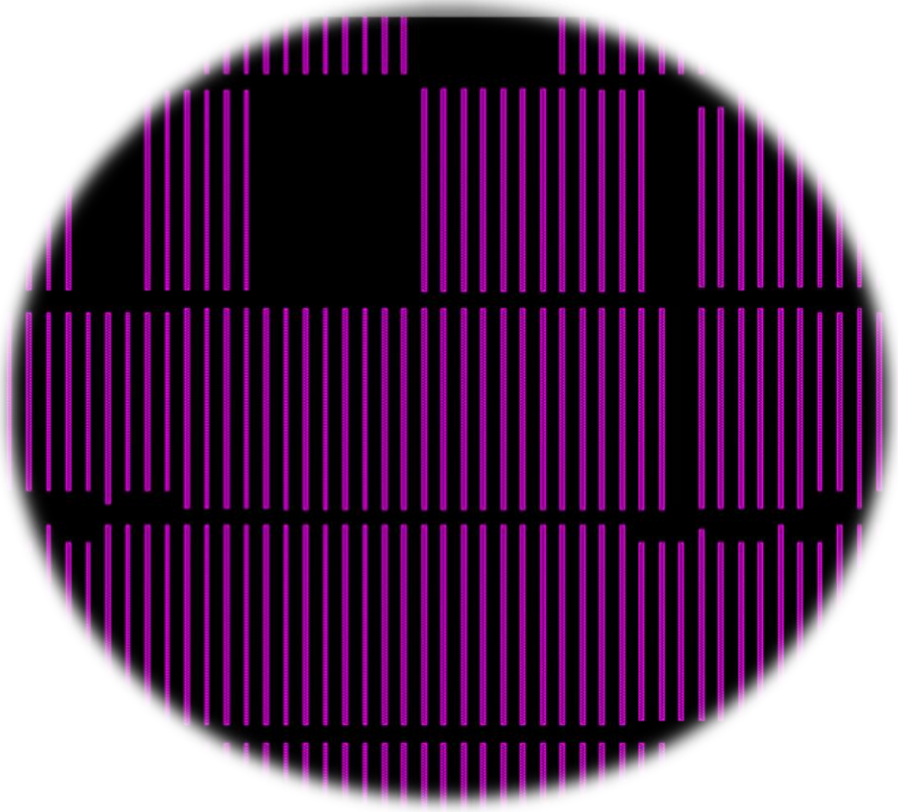
- **Experimental Results**

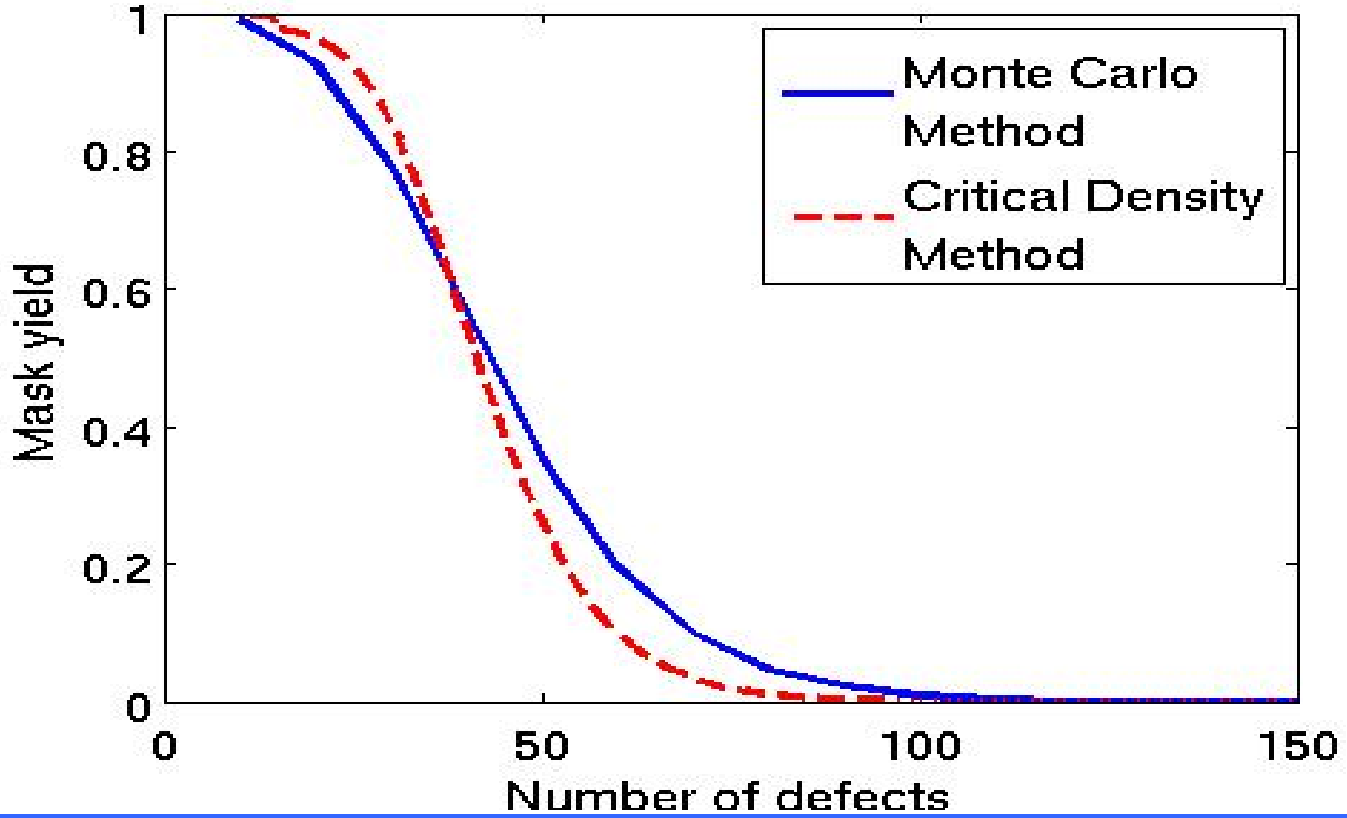
Experimental Setup

- Implemented using C++
  - OpenAccess API for parsing layout, Boost Polygon for Boolean operations and Eigen for matrix operations
- Synopsys 32nm library (scaled to 8nm node) for testcase layouts
- 3D Gaussian defects with probability distribution of size proportional to defect volume
  - Height → {0.5nm, 1nm, 2nm}
  - Full width half maximum → {25nm, 50nm, 75nm}
- Pattern shift limit set to 0.5µm
  - Smaller than typically used due to runtime of Monte Carlo method
- 800 layouts clips used for fitting linear model of critical density

Model Accuracy Results: Regular Polysilicon layer

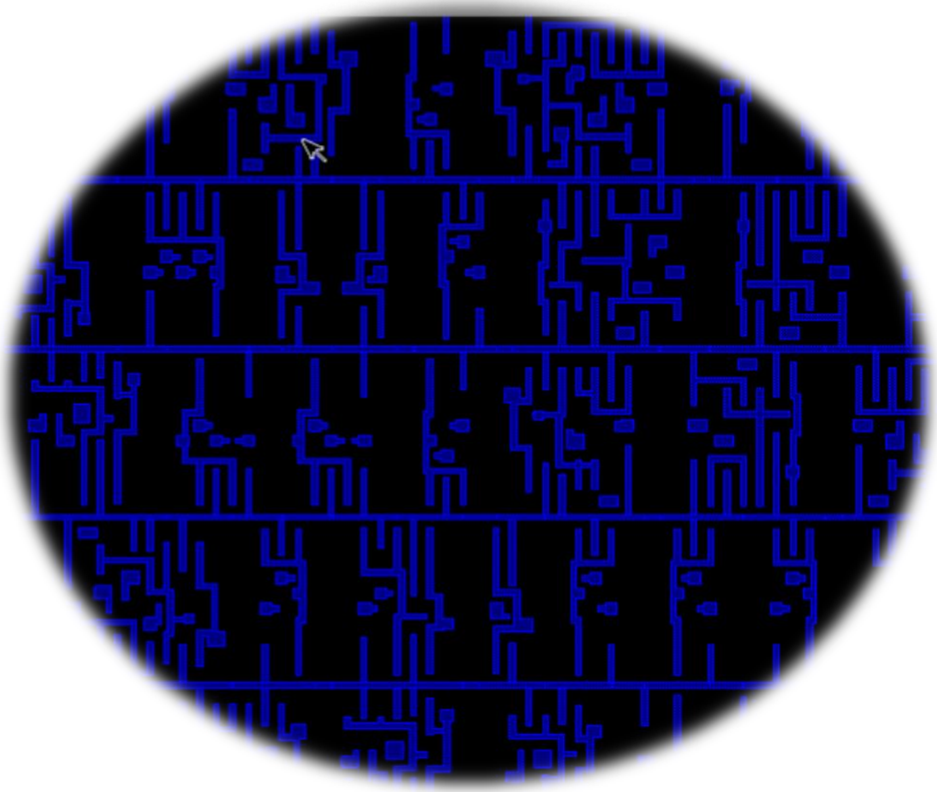
- Average (across defect densities) root mean square error less than 6.5% for four different designs
- More than 565X-775X improvement in runtime over Monte Carlo

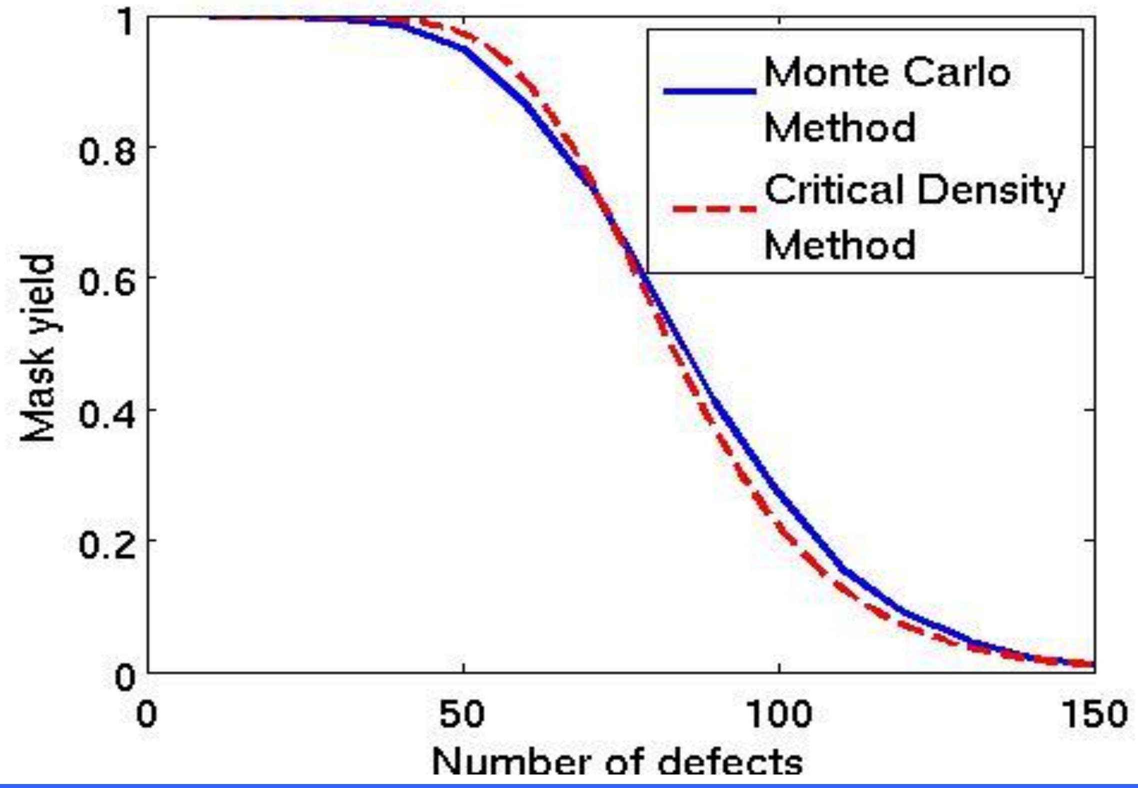




Model Accuracy Results: Random M1 Layer

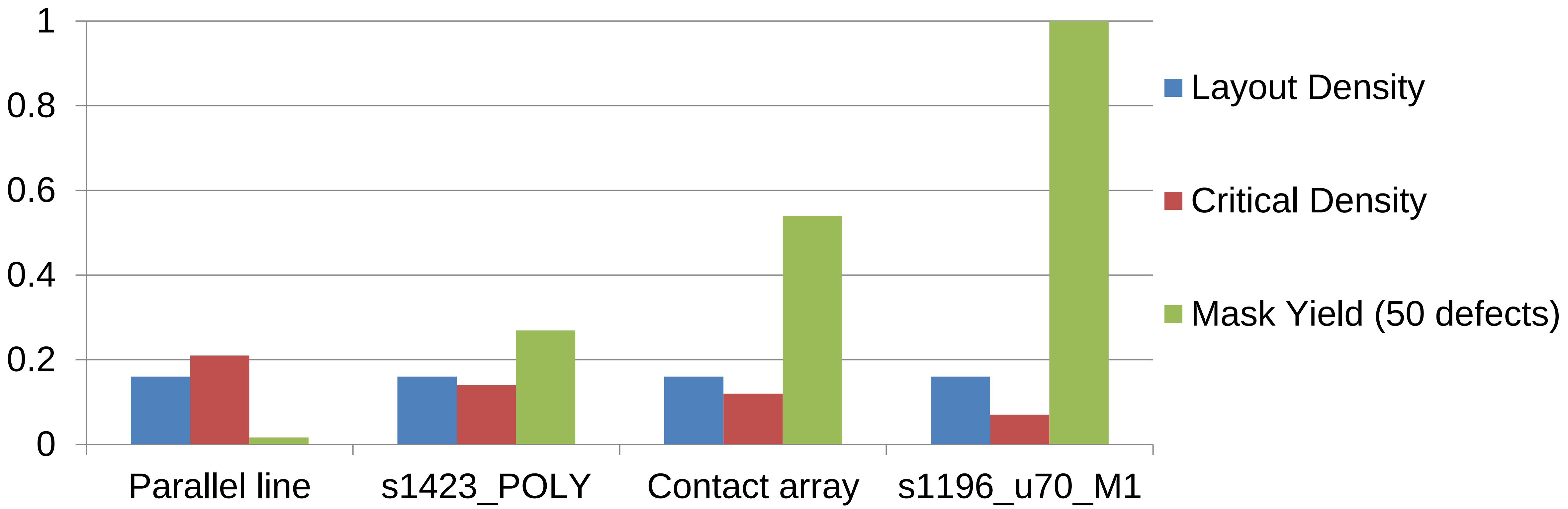
- Average (across defect densities) root mean square error less than 4.2% for four different designs
- 563-919X improvement in runtime over Monte Carlo





Impact of Layout Regularity on Mask Yield of Layouts

- **Four layouts with same layout density have mask yield ranging from 1% to 100% !**
  - 2D layouts better than 1D since they benefit from both X and Y direction shifts
  - Irregular layouts better due to lack of periodicity



Conclusions and Future Work

- Proposed new metric called critical density evaluate robustness of EUV Layouts to mask defects
- Developed critical density based model to estimate mask yield of EUV layouts
  - 300-1300X faster than Monte Carlo, error less than 6.5%
- Irregular, 2D layouts can have more than 50%-point better mask yield than regular 1D layouts
- Ongoing work
  - Develop methods to improve EUV layouts → Requires further speedup in estimation
  - Extend model to account for rotation and floorplanning/ based mitigation techniques

THANK YOU