UCLA

Impact of Range and Precision on Standard Cell Libraries

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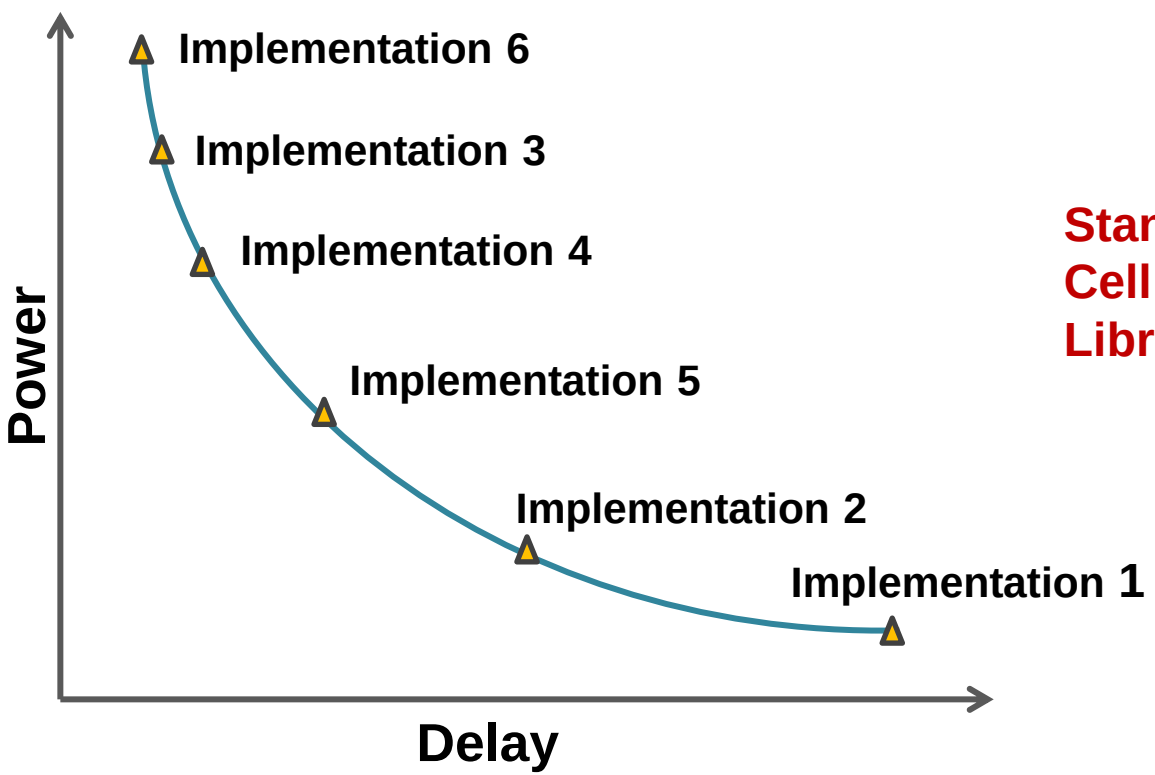
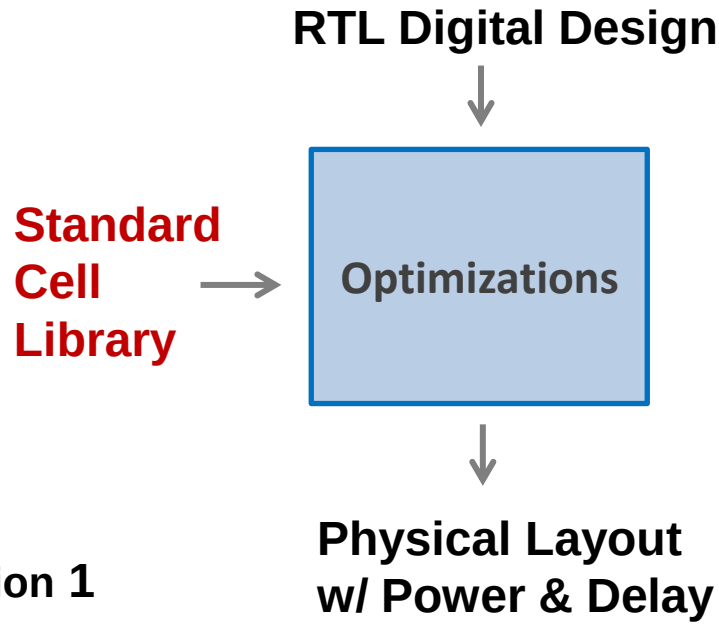
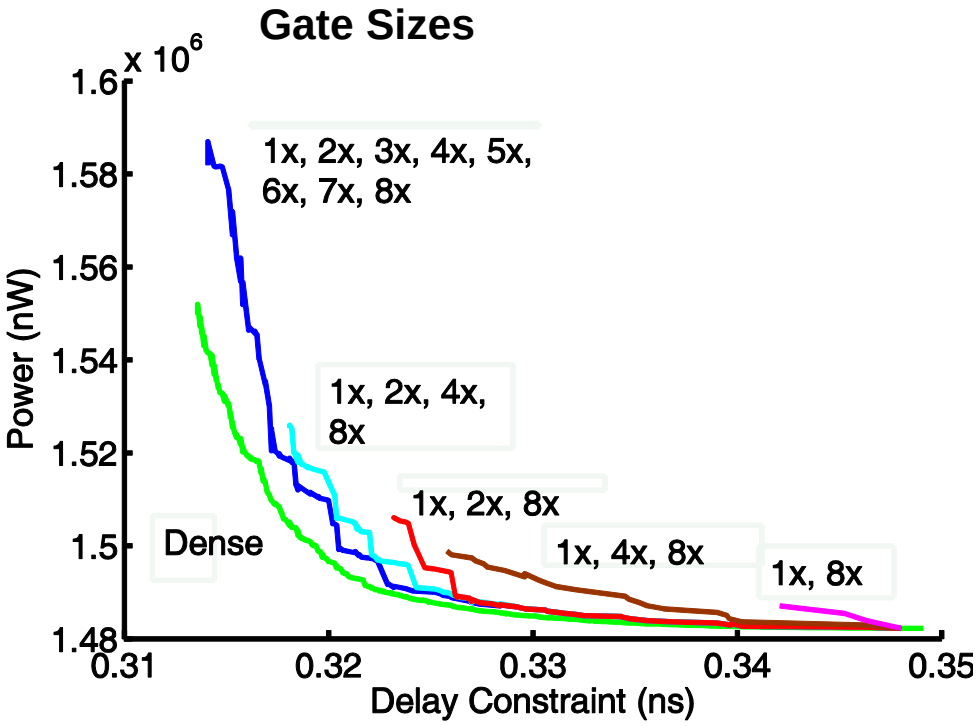
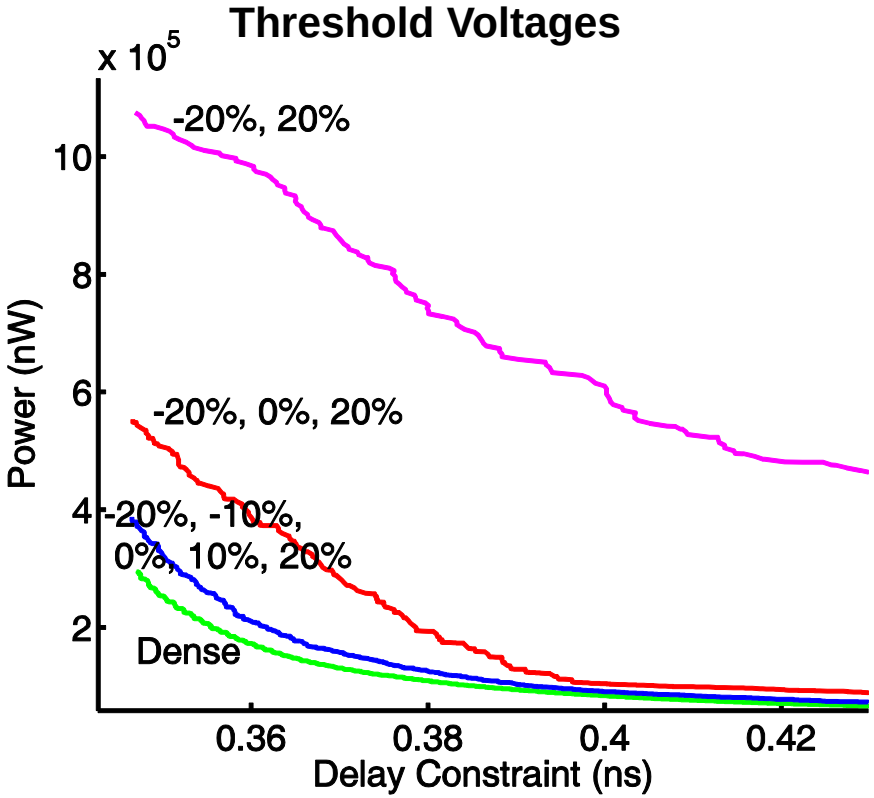
Introduction:
Tradeoff Between Power and Delay





Motivation:
Power and Delay Tradeoffs





S35932 Benchmark (ISCAS ‘89)
32nm Educational Library (Synopsys)

Motivation: FinFET Standard Cell Libraries

- Gate sizes quantized (1x, 2x, 3x, 4x, …)
  - Affects the delay range and feasibility
- Limited availability of Threshold Voltages
  - Created by adjusting gate workfunction or use the back-gate
  - Number of threshold voltages will likely be limited [Warnock 11]
- What does this mean for resulting designs? How can this impact be quantified?

Outline

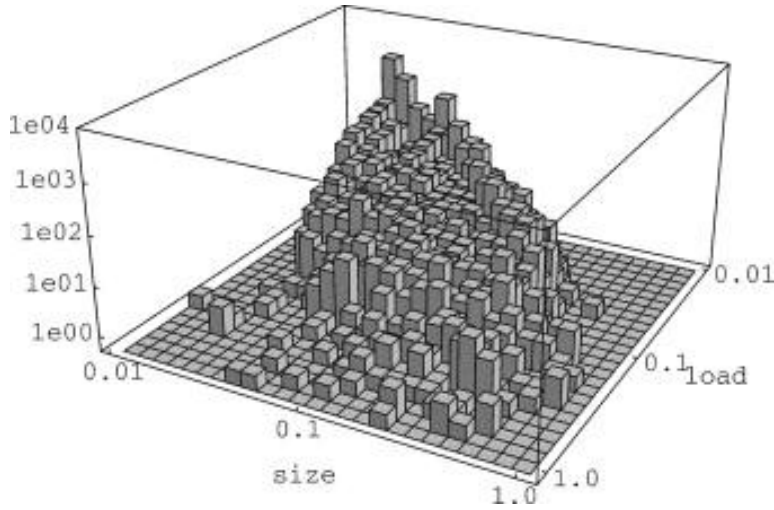
1. Prior Approaches to finding the impact of the standard cell library
2. Expressions to estimate suboptimality
   - Gate Sizes
   - Threshold Voltages
3. Experimental validation
   - Gate sizes
   - Threshold voltages
4. Discussion on Range and Precision

Prior Approaches

- Experiments and heuristics for selecting library sizes
  - Using **Quantization** Error + Experimental Results
    [Beeftink et al 98, 00]

$$\mathrm{so}_{Q(\mathrm{size})} = \min_{s_i} |s_i - s|$$

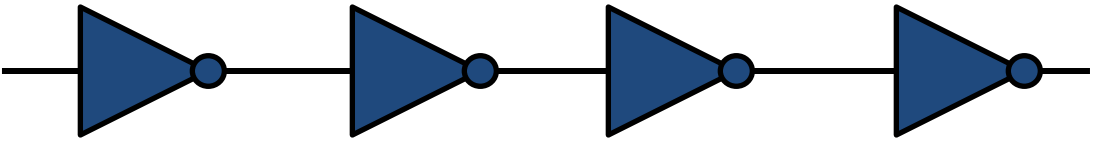
  - Experimental Results to determine best library sizes
    - Use the geometric progression 1.3x, $(1.3)^2$x, $(1.3)^3$x, $(1.3)^4$x, etc.
      - [Singhal and Girishankar 06]
    - Use .5x, 1x, 2x, 3x, 4x, 5x
      - [Afonso et al 09]
- Prior art could not predict suboptimality of size selection
  - More difficult and stronger question



[Beeftink et al 00]

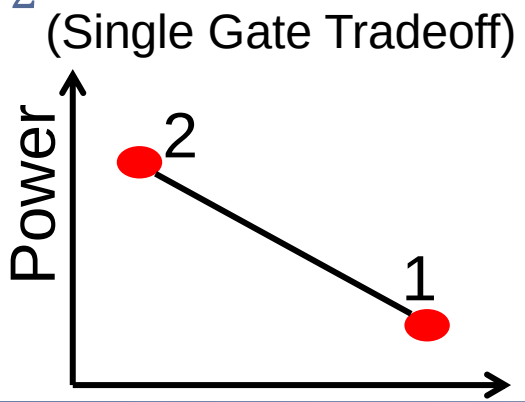
Thought Experiment #1

- N Inverter Chain,
  - Delay Constraint T



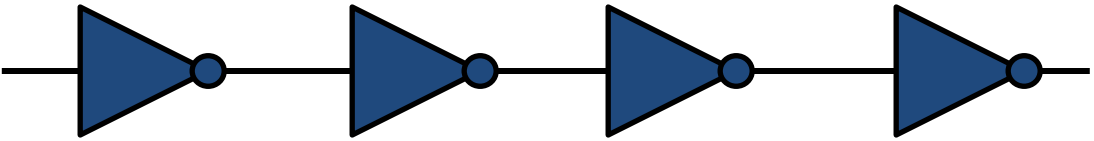
Vth	Delay	Power
x	x	3-x
1	1	2
2	2	1

- Continuous Optimum for $\mathrm{v_{th}} = \frac{T}{N}$
- With $v_{th} \in \{1, 2\}$
  - Discrete Optimum: have $\lfloor T - N \rceil$ gates at $\mathrm{v_{th}} = 2$
  - Suboptimality is at most 1
    - Proportional to 1/N & decreases as $N \to \infty$



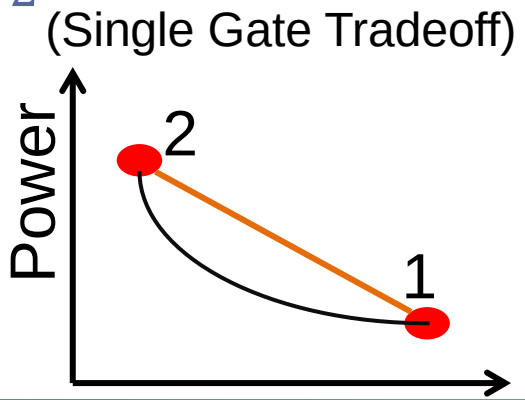
Thought Experiment #2

- N Inverter Chain,
  - Delay Constraint T



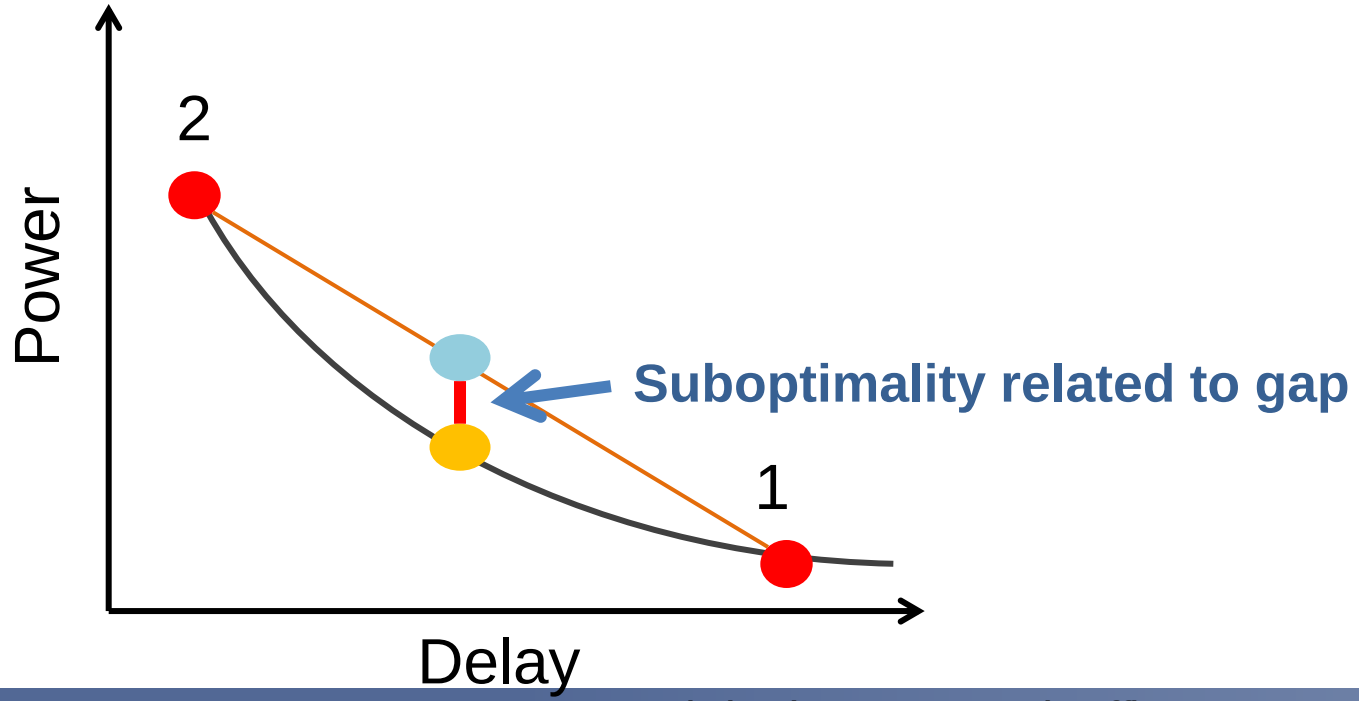
Vth	Delay	Power
x	x	$2^{-v_{th}+2}$
1	1	2
2	2	1

- Same Continuous Optimum: $\mathrm{v_{th}} = \frac{T}{N}$
- With $v_{th} \in \{1, 2\}$
  - Discrete Optimum: have $\lfloor T - N \rfloor$ gates at $\mathrm{v_{th}} = 2$
  - Suboptimality does not decrease as $N \to \infty$



Suboptimality and Convexity

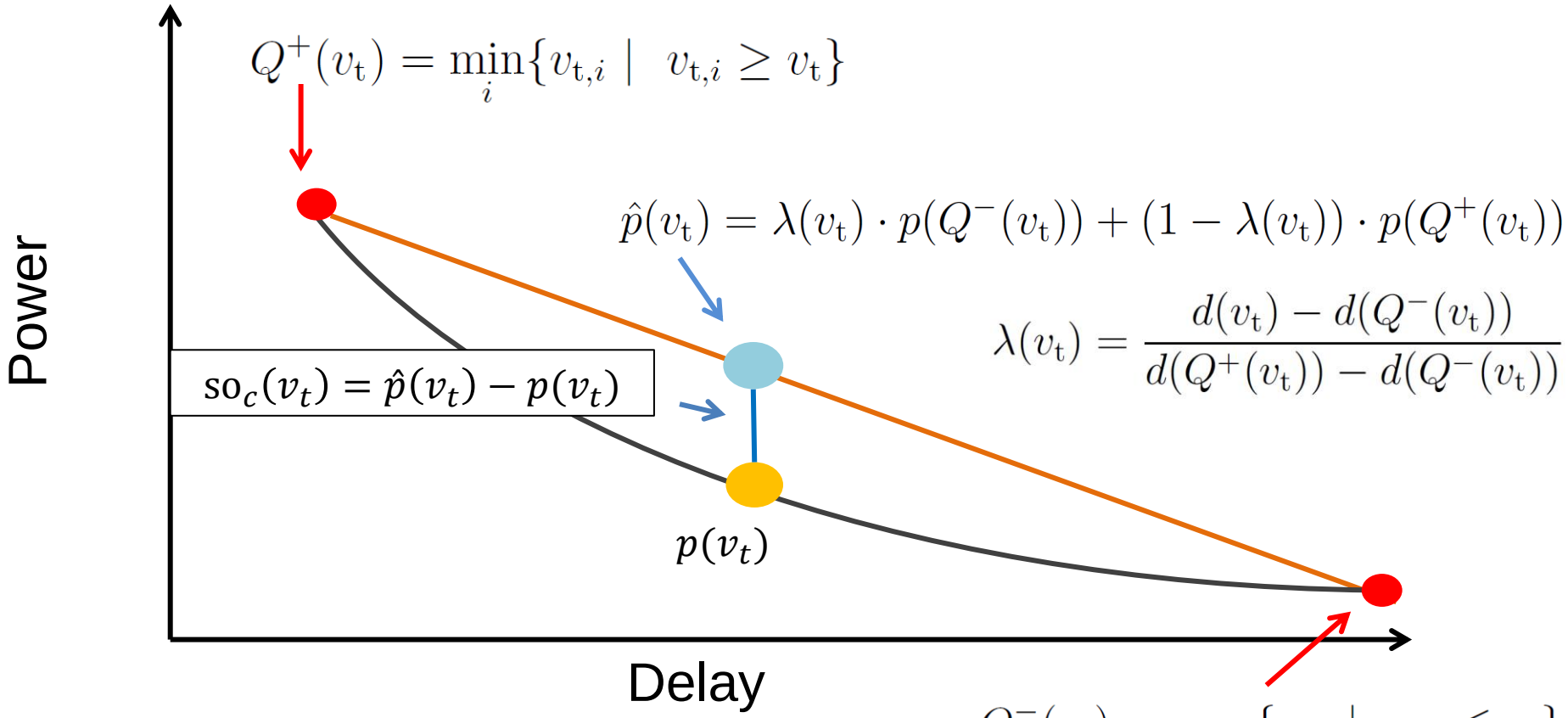
- Power vs. Delay Tradeoff curves are convex non-increasing functions
- Convex curves have the property that any secant line lies at or above the curve



(Single Gate Tradeoff)

Suboptimality expressions: v_t

- Suboptimality is the difference between the upper line and the lower tradeoff curve



(Single Gate Tradeoff)

Suboptimality of Full Design

- Sum of individual gate suboptimalities

$$\mathrm{so}_c(\mathrm{Design}) = \sum_{\{\forall g \in \mathrm{Design}\}} \mathrm{so}_c(v_t)$$

with

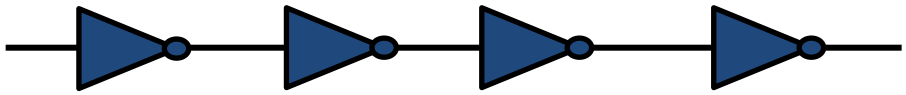
$\mathrm{so}_c(v_t) = \hat{p}(v_t) - p(v_t)$: Per gate suboptimality

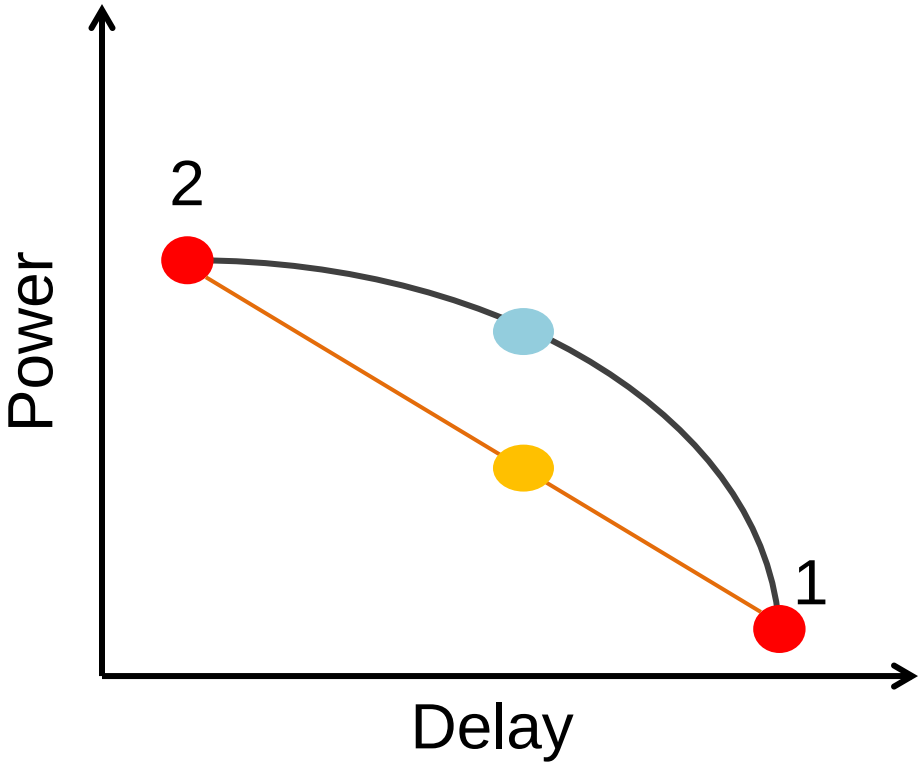
$\hat{p}(v_t)$: Achievable power tradeoff with given sizes

$p(v_t)$: Continuous optimal size (v_t) and power $p(v_t)$

Non-convex Power Delay Curves

Non-convex curves



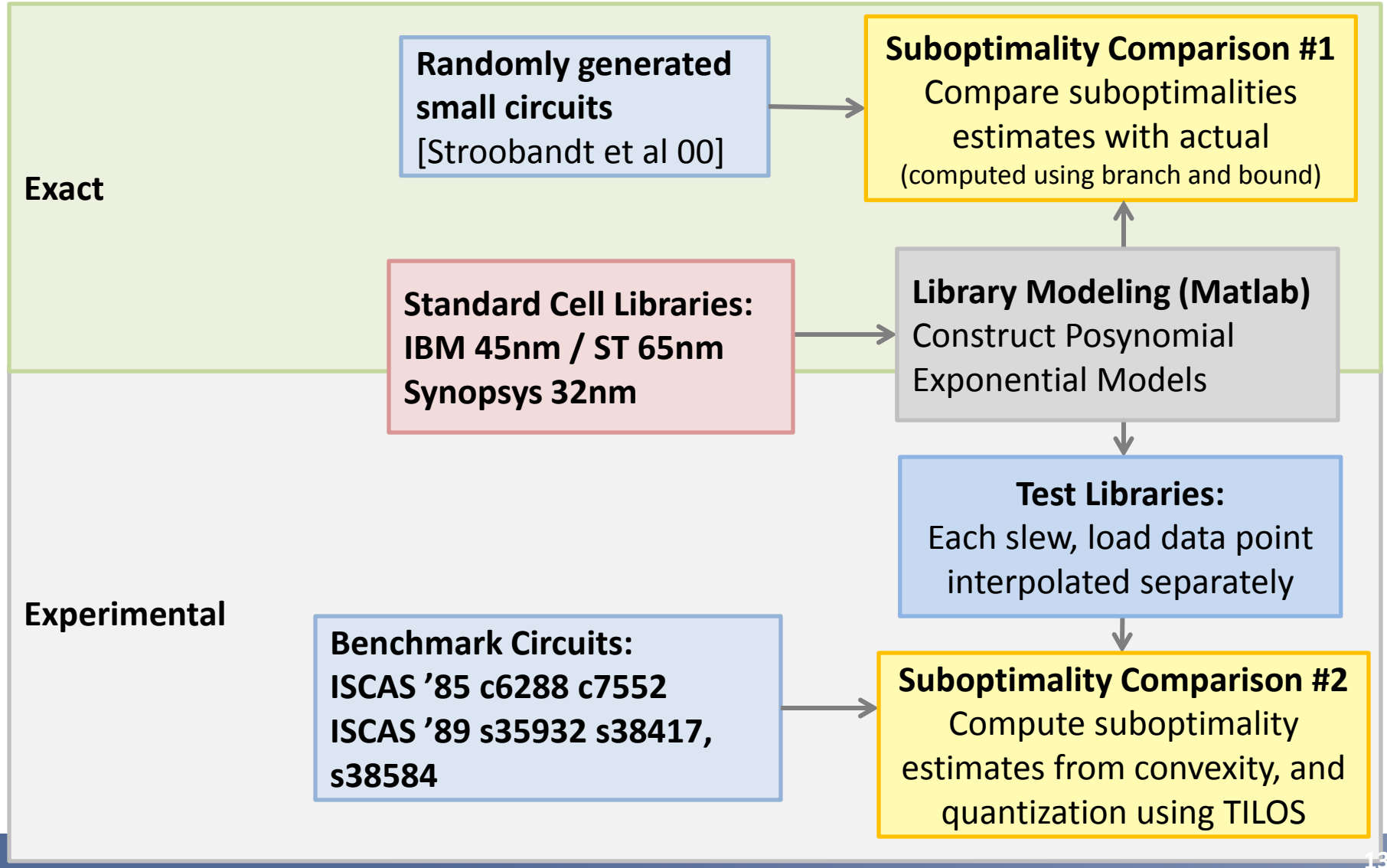


Concave Curves

- Optimal Solution Utilizes a mixture of (1) and (2)

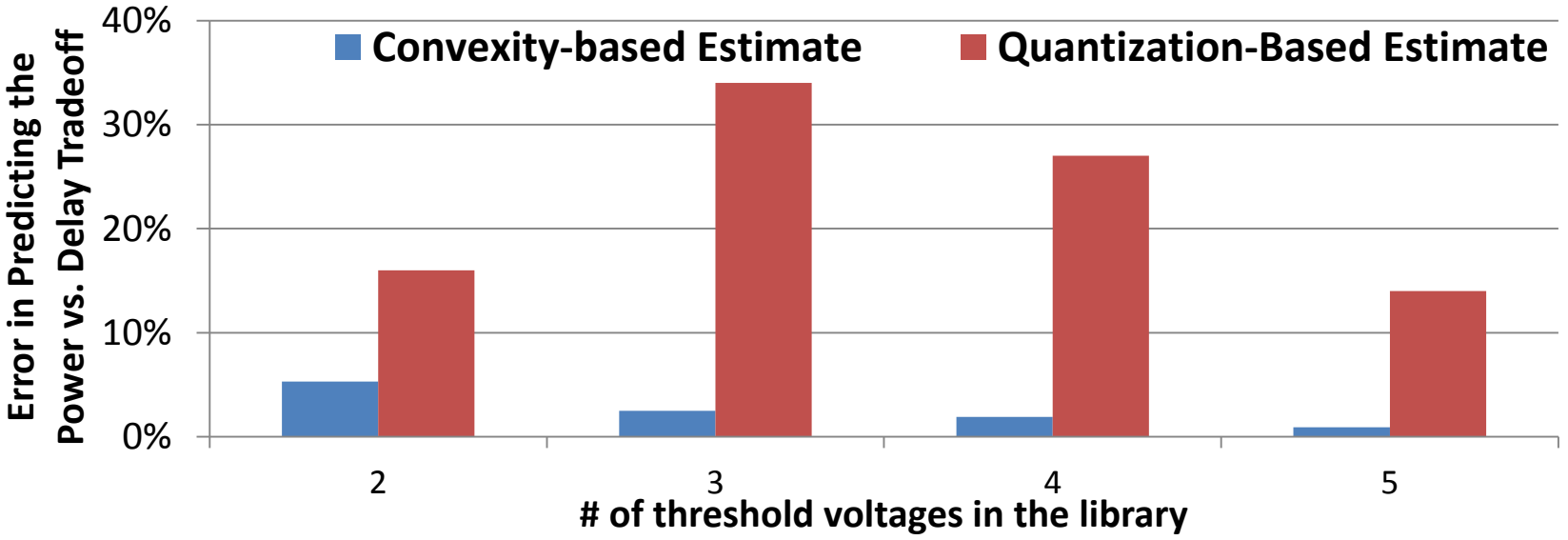
(Single Gate Tradeoff)

Experimental Setup: v_t assignment



Experiment (Exact Methods): Estimating the tradeoff of v_t assignment

- 30 randomly generated circuits, each with size 30 using [Stroobandt 00]
- Used to predict power delay tradeoff for different v_t libraries

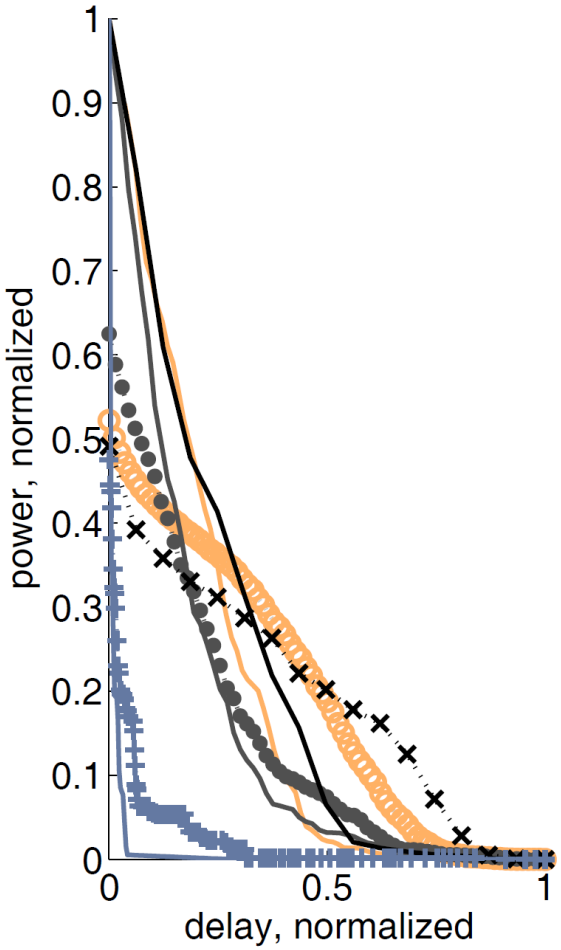


Estimation error is relative to total power

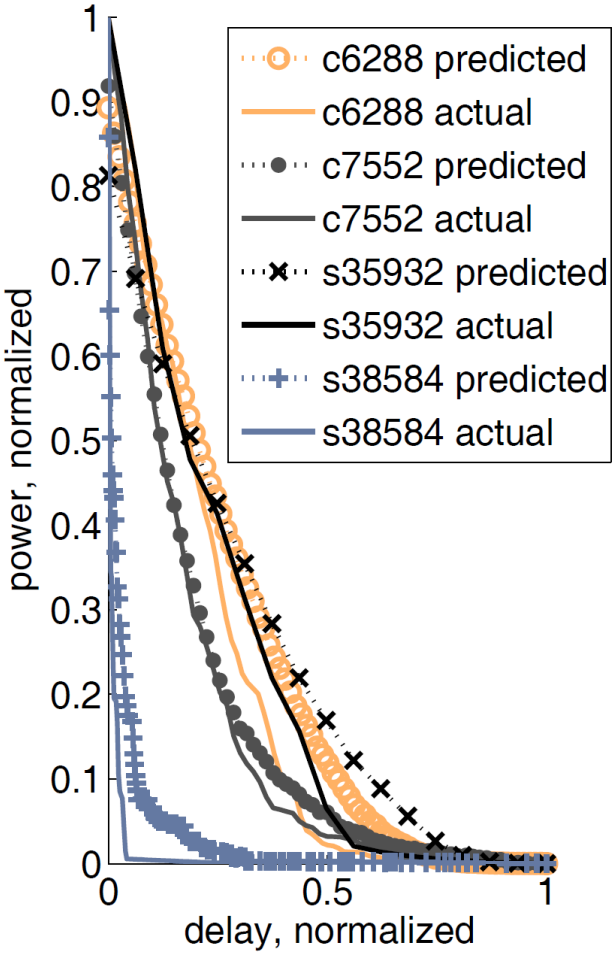
Experiment (TILOS): Estimating the tradeoff of v_t assignment

2 v_t tradeoff prediction

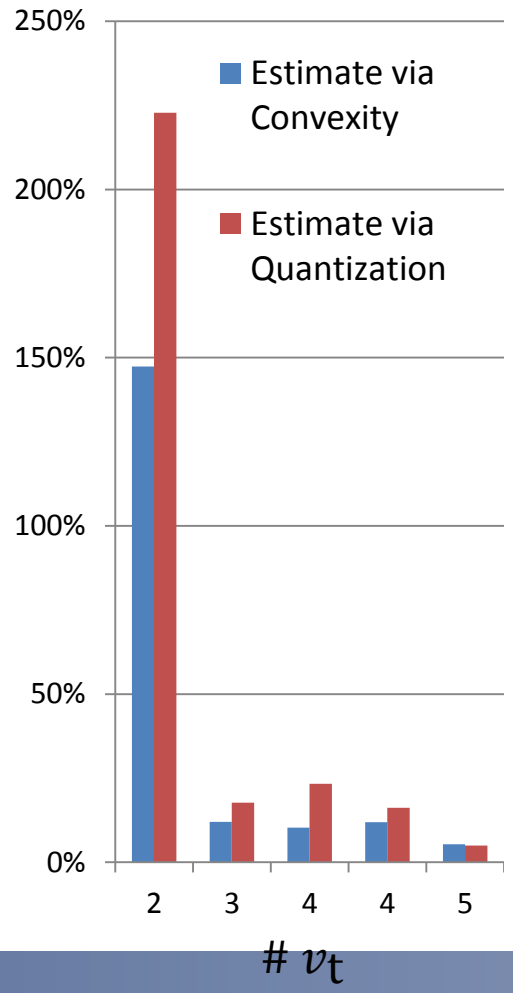
Quantization-based Estimate



Convexity-based Estimate



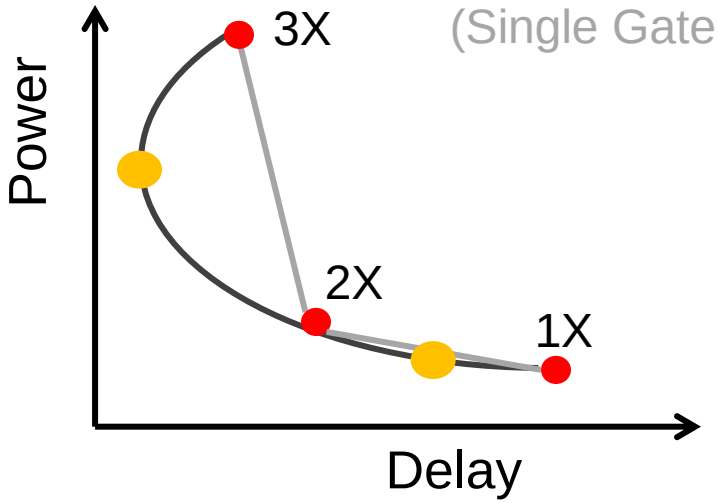
Estimation Errors
(as a percentage of total power)



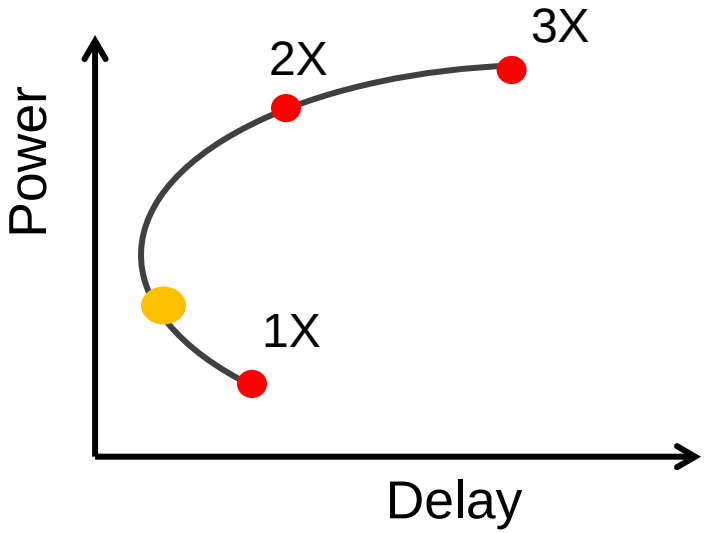
(Design Tradeoff)

Extension to Gate Sizing

- Power delay curves different for gate sizing
  - Account for both delay at the input and output of the gate

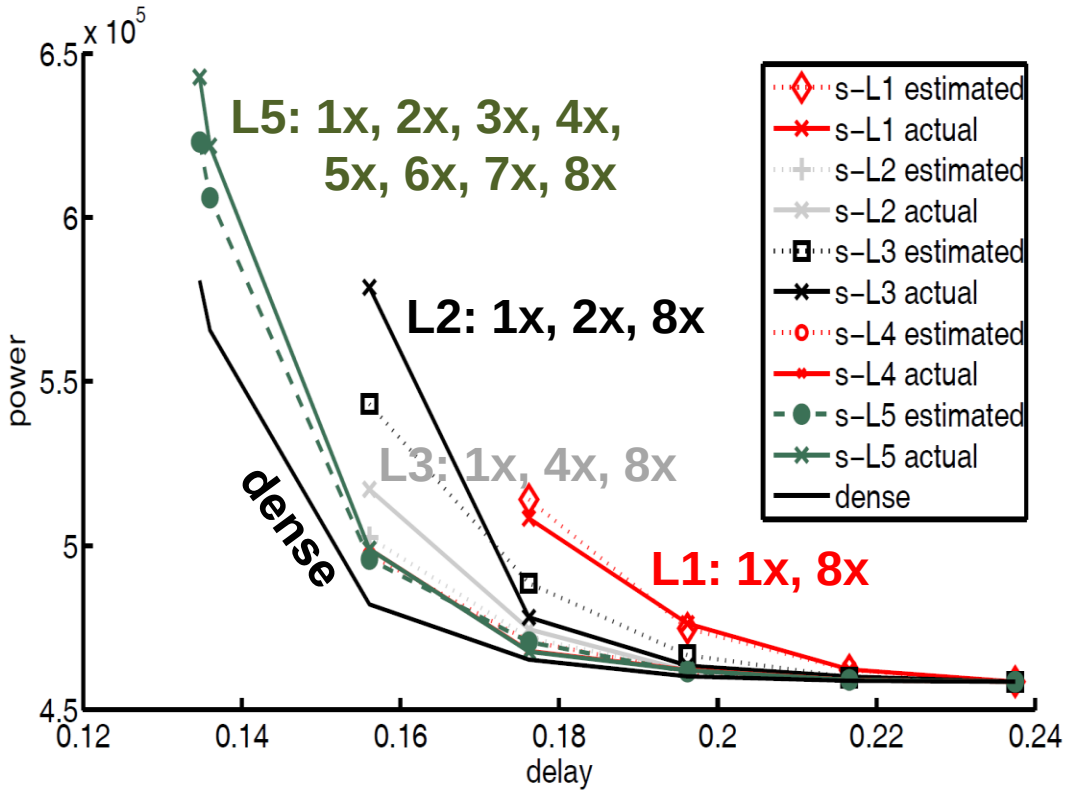


(Single Gate Tradeoffs)



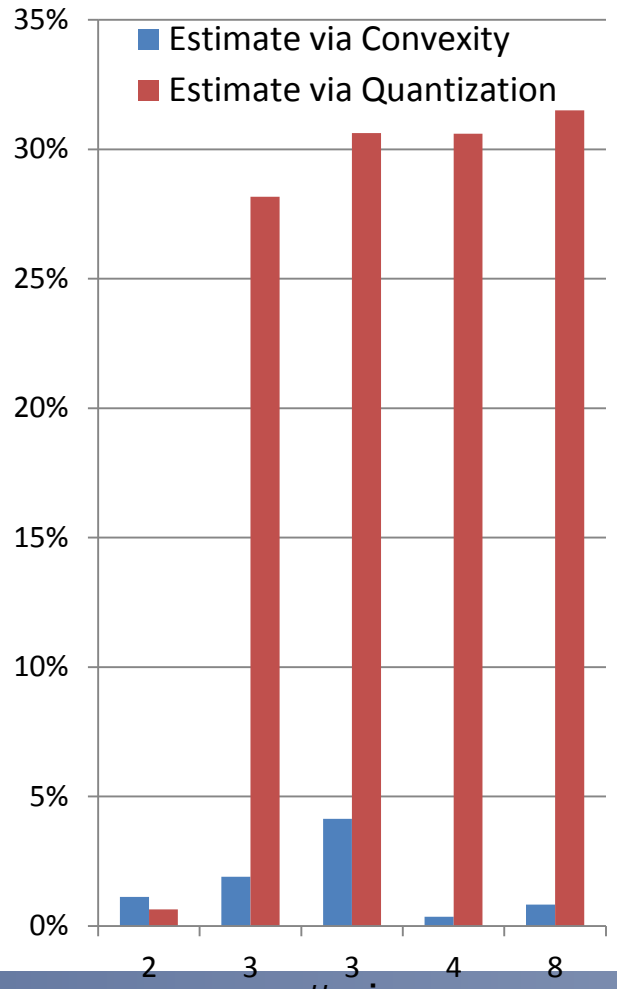
- Two cases:
  - Required delay is **possible** (use the same method as before)
  - Required delay is **impossible** (estimate with **round-up** penalty)
    - Fitting term needed (benchmark dependent)

Experiment: estimating the tradeoff of gate sizing



C7552 design power vs. delay tradeoff

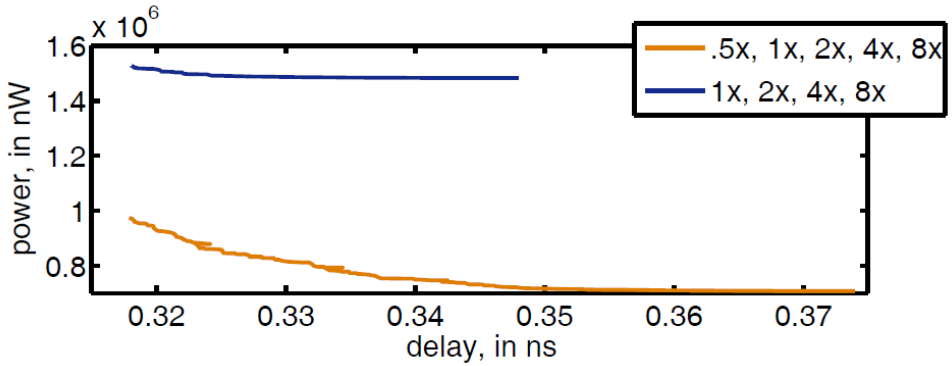
Estimation Errors
(as a percentage of total power)



Discussion: Dynamic Range Considerations

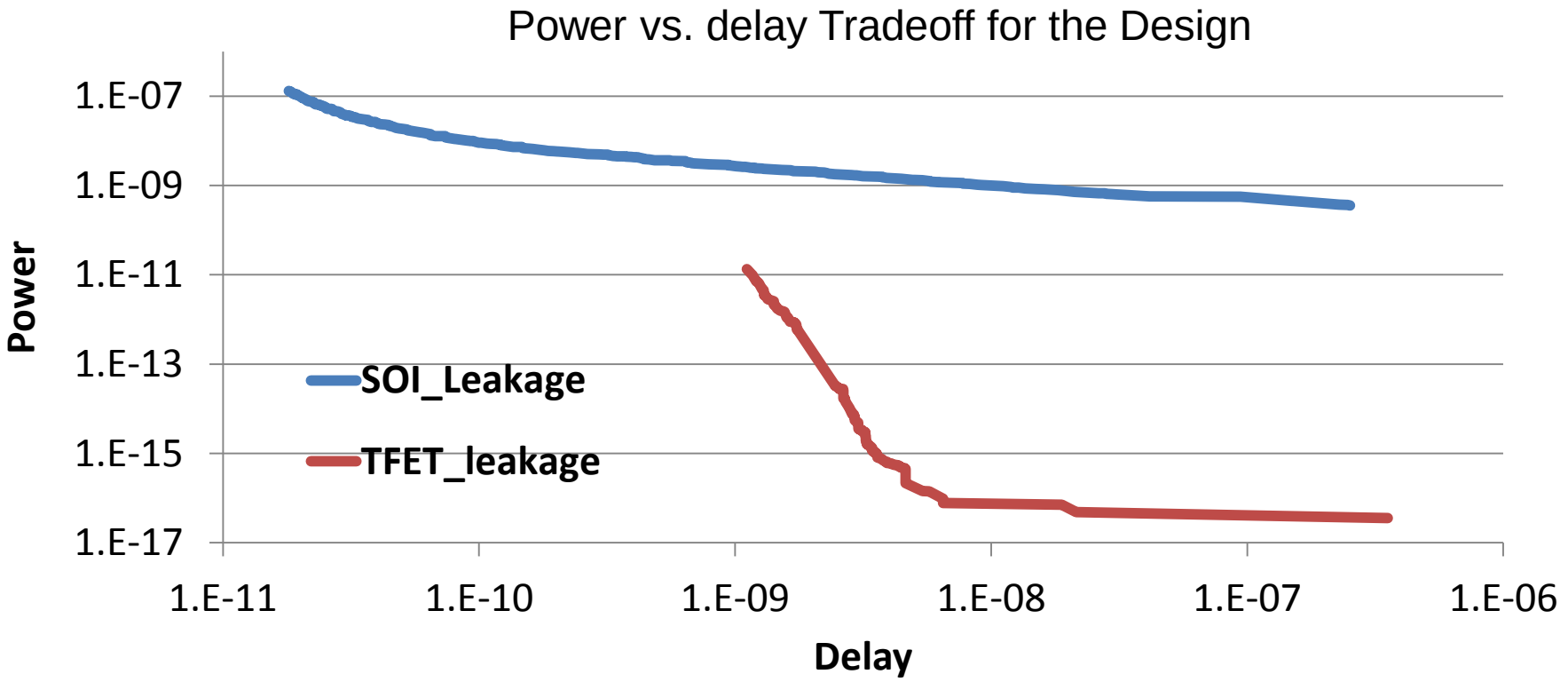
- Always need a low power option
  - Dictated by the technology and allowable slew rates

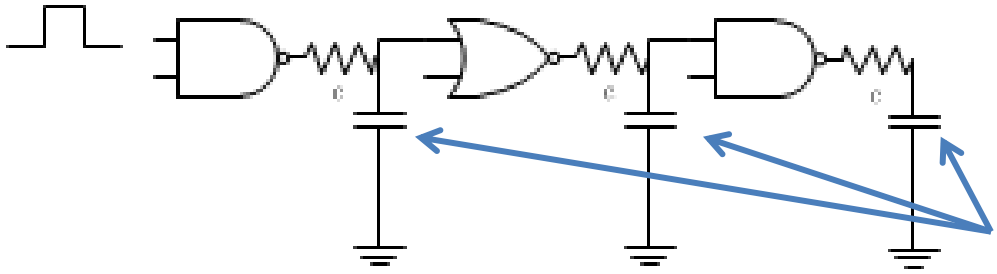
S35932 design tradeoff



  - Estimate as fraction of minimum-sized devices with pos. slack
- Largest Size
  - Related to the capacitive loads in a design
  - Convex p/d curve – tradeoff between power vs. delay is worse
- Lowest Vt
  - Related to delay range needs

Discussion:
SOI and TFET Technology Example

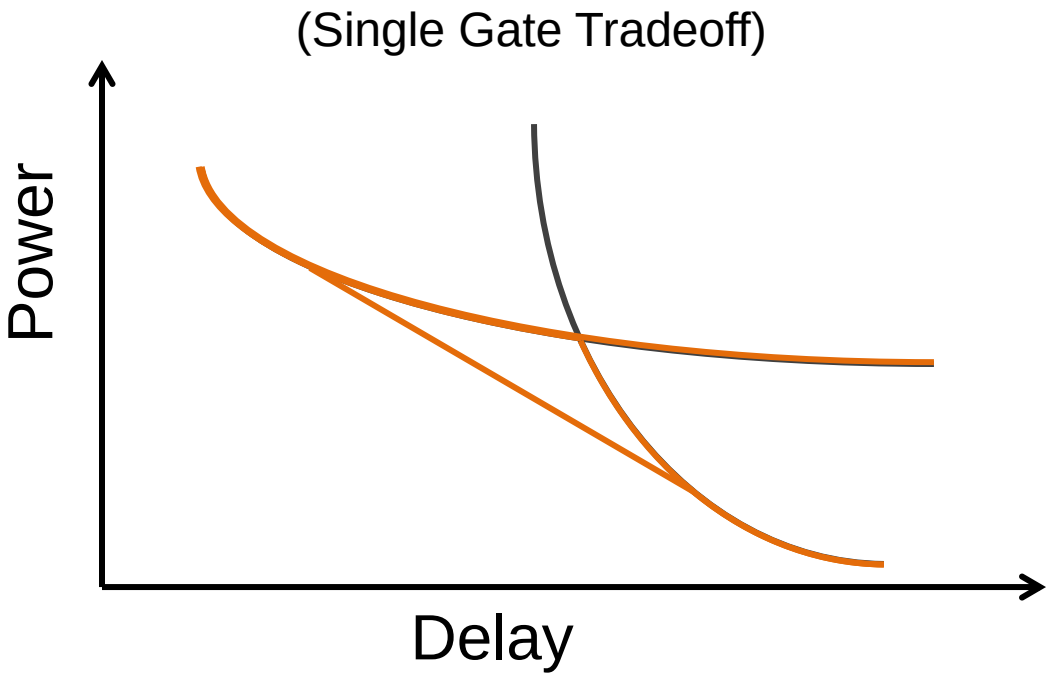




(Data and plot courtesy of Shaodi Wang)

Discussion: Mixing Technologies

- Allows for several tradeoffs:
  - Use one technology
  - Use both technologies but optimize independently
  - Use both technologies and optimize jointly



Summary

- Method to estimate the suboptimality related to a selection of sizes or v_t
  - Related to the convexity of the power delay tradeoff
- Experimental results show strong explanatory power compared to prior work
  - 2x better (gate sizing) and 10x better (threshold voltage)
  - Use in determining which standard library cells to provide
- Can be used to understand impact of future technologies
  - FinFet Libraries with limited size and vth availability
  - Designs with mixtures of different technologies

References

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