# A Framework for Double Patterning-Enabled Design

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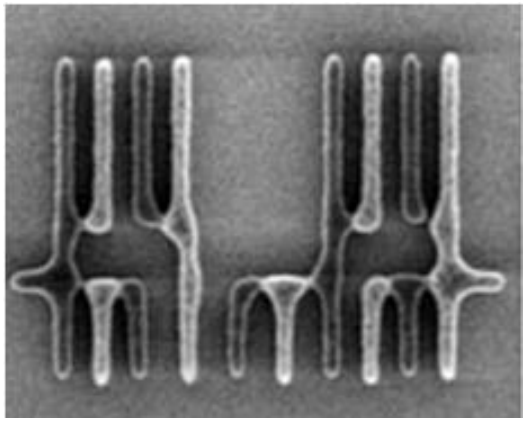
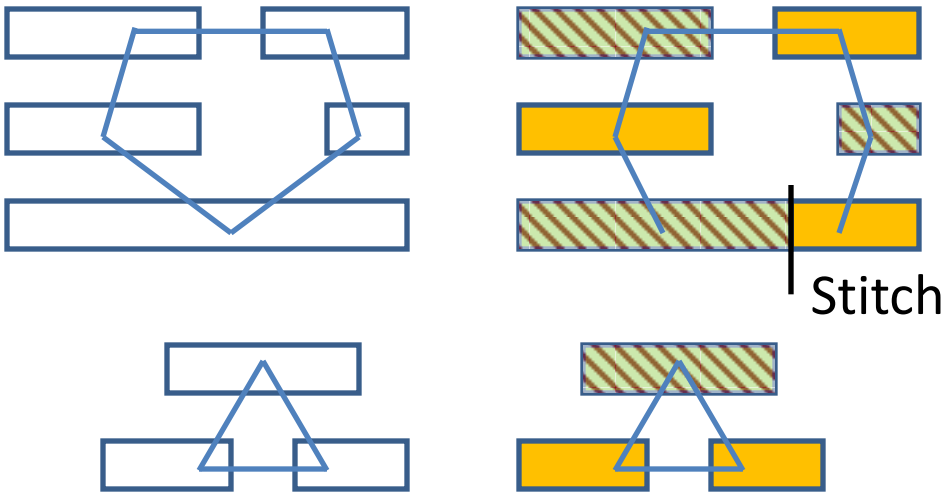
# Double-Patterning Lithography

- DP in LELE process is an attractive technique to scale tech to 20nm an below
- Delays in EUV → DP is inevitable
- DP's biggest challenge is coloring conflicts
  - Stitching cannot resolve all conflicts
  - Odd cycle in post-stitching conflict graph → native conflict

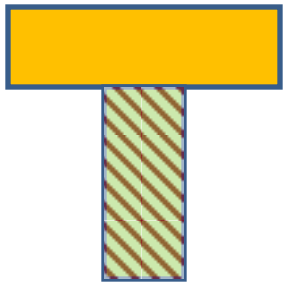


*C. Mack, IEEE Spectrum 08*

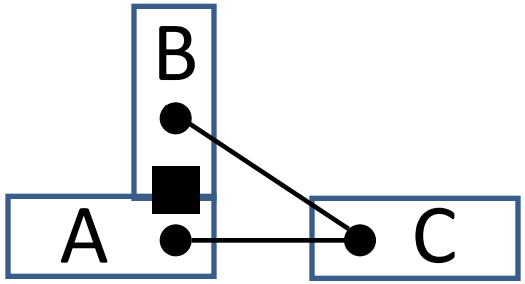


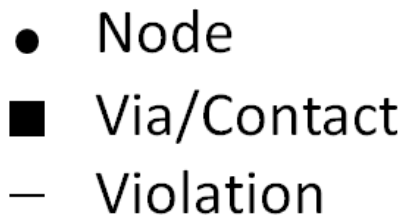
# Prior Art in Coloring

*Rule based stitching*



*Segmentation*



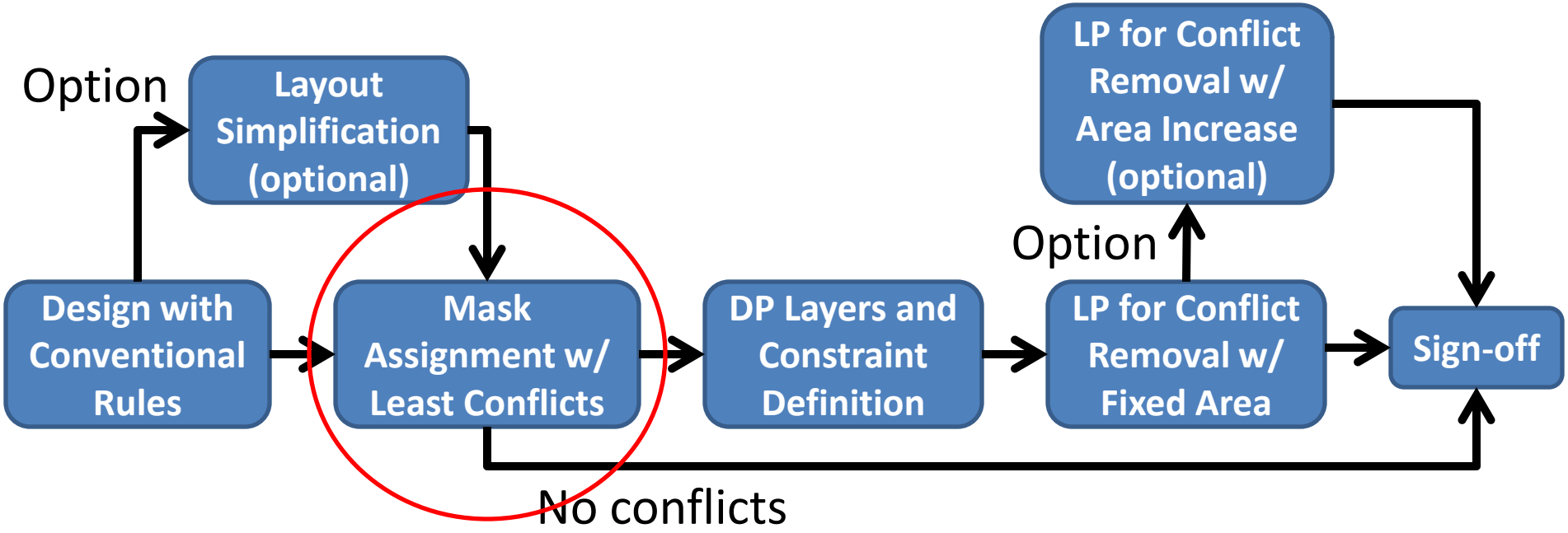




- Rule based stitching (Chiou *et al.* & Tritchkov *et al.* SPIE'08)
  - Stitch at specific shape locations
  - Many stitch locations cannot be found
- Segmentation-based coloring and stitch minimization
  - Segment polygons into rectangles (e.g. Kahng TCAD'10, Yuan ISPD'09)
  - Unnecessarily grows the problem size
  - Difficult to handle different tip-to-tip, tip-to-side, and side-to-side spacing rules

# Prior Art in Conflict Removal

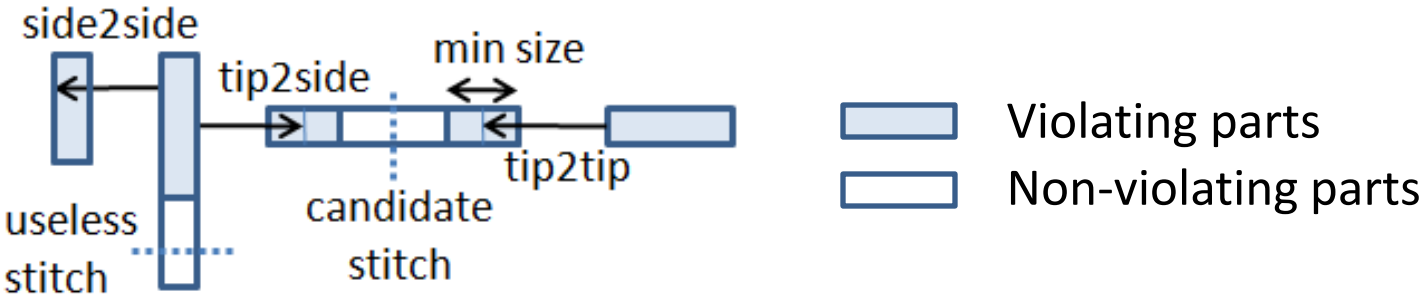
- ILP-based layout perturbation (Hsu *et al.* & Yuan *et al.* ICCAD'09)
  - Slow solving time
  - DP constraints in ILP → even slower
- Iterative layout compaction (Chen et al. ICCAD'09)
  - DP-compliance check at every iteration → slow
  - DP constraints only at odd cycles → Resolution of one conflict may introduce another and may not converge
- Use segmentation
  - Earlier drawbacks
  - Also, needs to maintain connectivity at joints

# Overview of the Framework




- Fast linear time coloring
- LP-based conflict removal
  - Simultaneously fixes all conflicts without creating new conflicts

# Mask Assignment

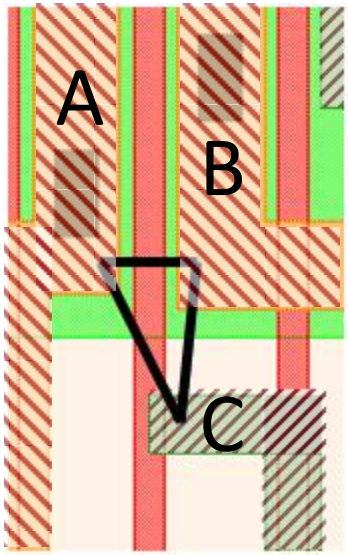



- Design rule-dependent projection
  - Project from each lineside and lineend based on rule value
    - Violating parts → min same-color space
    - Non-violating parts → can be any color
  - Grow violating parts to meet minimum feature size on mask
  - Stitch locations are non-violating parts b/w 2 or more violating parts of size > min overlap length

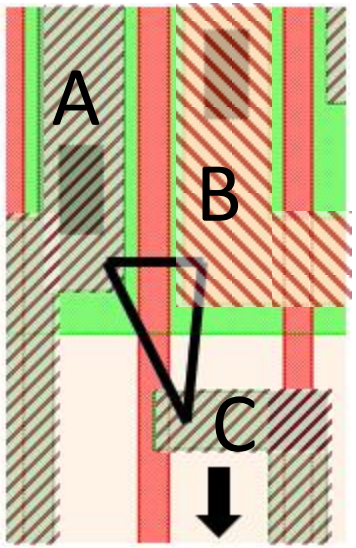
# Mask Assignment and Benefits

- Assign violating parts to the first and second mask
  - Constraint: min achievable # of conflicts with DP DRs obeyed
  - Objective: minimize # of stitches
- Guarantee to find a coloring solution if one exists
- No segmentation
  - Handles tip-to-tip, tip-to-side, side-to-side, and min size rules naturally
  - Dealing with polygons rather than rectangles → smaller problem size

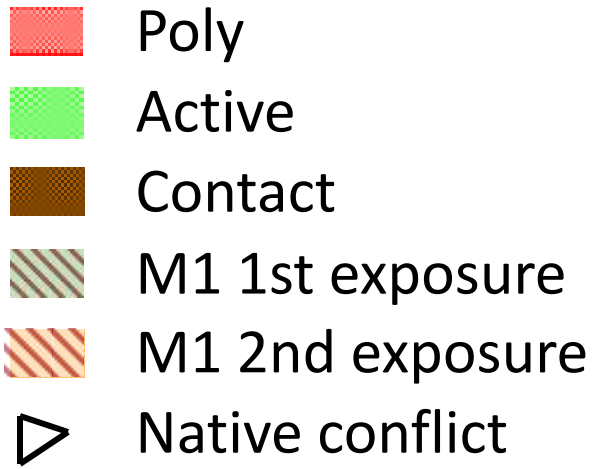
# Mask Assignment – Preferred Coloring




*Bad coloring*

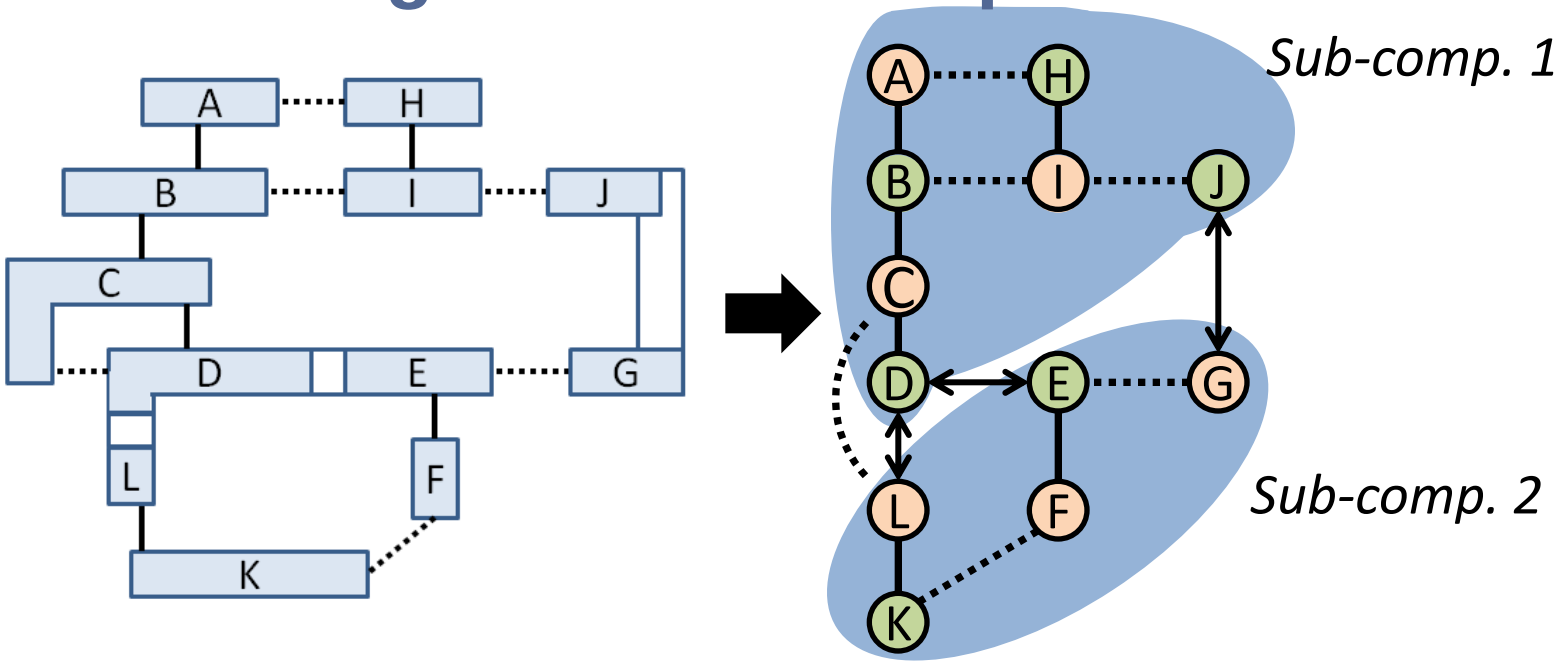



*Good coloring*




- Coloring of native conflicts affects efficiency of conflict removal
- Give preference for opposite coloring for certain violations over others → label violations critical vs. less-critical
  - E.g., horizontal spacing violation more critical than vertical or diagonal in case of vertical poly orientation

# O(n) Mask Assignment – Example




1. Conflict graph with critical viol, less-critical viol, and stitches
2. Identify connected components (colored independently)
3. Identify sub-components (sub-graph with no stitches)
4. Alternating coloring with critical nodes colored before
   - less-critical nodes and until a stitch must be used
5. Flip sub-component coloring to reduce used stitches

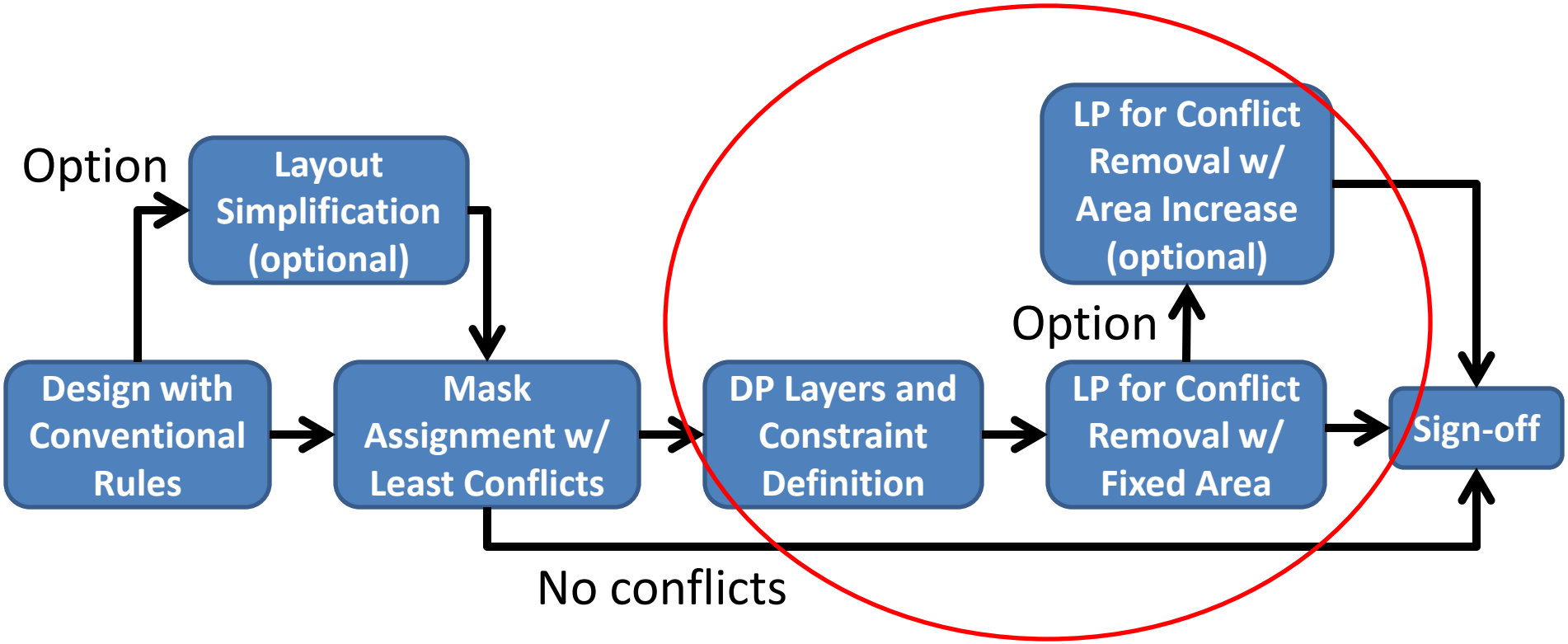
# Coloring Results

*Cuts = used stitches*
*Min = min overlap length in [nm]*

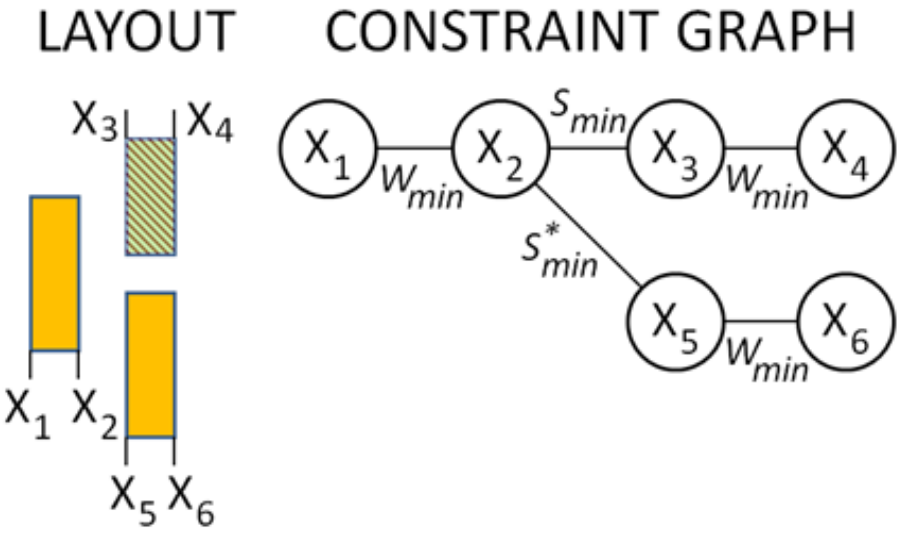
| | | ILP | | CCD | | Our approach | |
|---|---|---|---|---|---|---|---|
| **Design** | **Min** | **Cuts** | **Secs** | **Cuts** | **Secs** | **Cuts** | **Secs** |
| ART-A 45(70%) | 8 | 24290 | 564.6 | 25521 | 378.6 | 25480 | 6.1 |
| ART-B 45(70%) | 10 | 72828 | 2887.4 | 76550 | 2316.8 | 76634 | 20.5 |
| ART-C 45(70%) | 8 | 121916 | 8291.2 | 127935 | 7895.8 | 126715 | 35.5 |
| ART-A 45(90%) | 13 | 25432 | 612 | 26629 | 391 | 27691 | 6.3 |
| ART-B 45(90%) | 10 | 76292 | 2892.2 | 79836 | 2355.2 | 82089 | 20.5 |
| ART-C 45(90%) | 8 | 126238 | 8129 | 132303 | 8205 | 135558 | 37.5 |

- Test cases (Kahng *et al.* TCAD'10)
  - 100-500K cells, 45nm Poly, same rules
- Coloring 230X faster than ILP-based coloring
- # of stitches larger by a modest 4% to 8.8%

# Layout Legalization for Conflict Removal



# DP Layers and Constraint Definition




- DP layer → two stand-alone layers
- 2D prob. → successive 1D (in x and y directions)
- Construct constraint graph
  - Nodes → layout edges, Arcs → constraints (rules)
- Same mask DRs → arcs b/w features of same mask (e.g., $S^*_{min}$)
- DRs b/w the two mask layouts (e.g., min overlap length) → arcs b/w nodes of the two stand-alone layers
- DRs b/w whole DP layer & other layers → arcs with union layer

# LP Formulation to Remove Conflicts

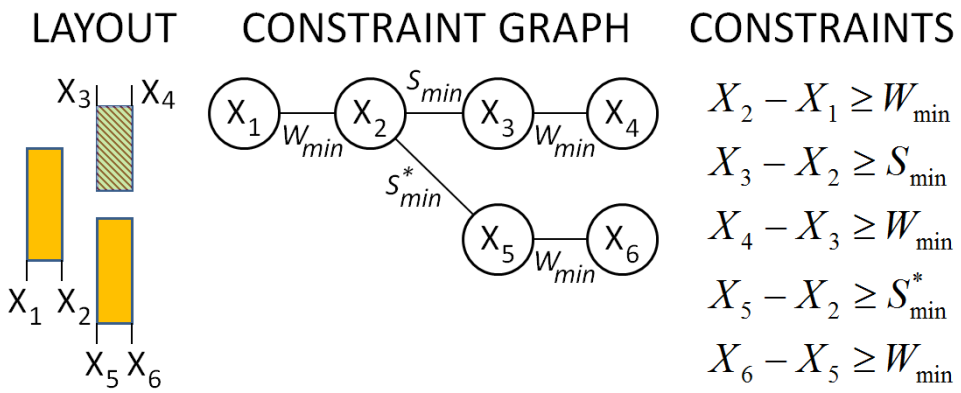
Problem formulation

$$Min \sum_i W_i |X_i - X_i^{init}|$$

$$St: X_j - X_i \geq d_{ij}, \forall A_{ij}$$

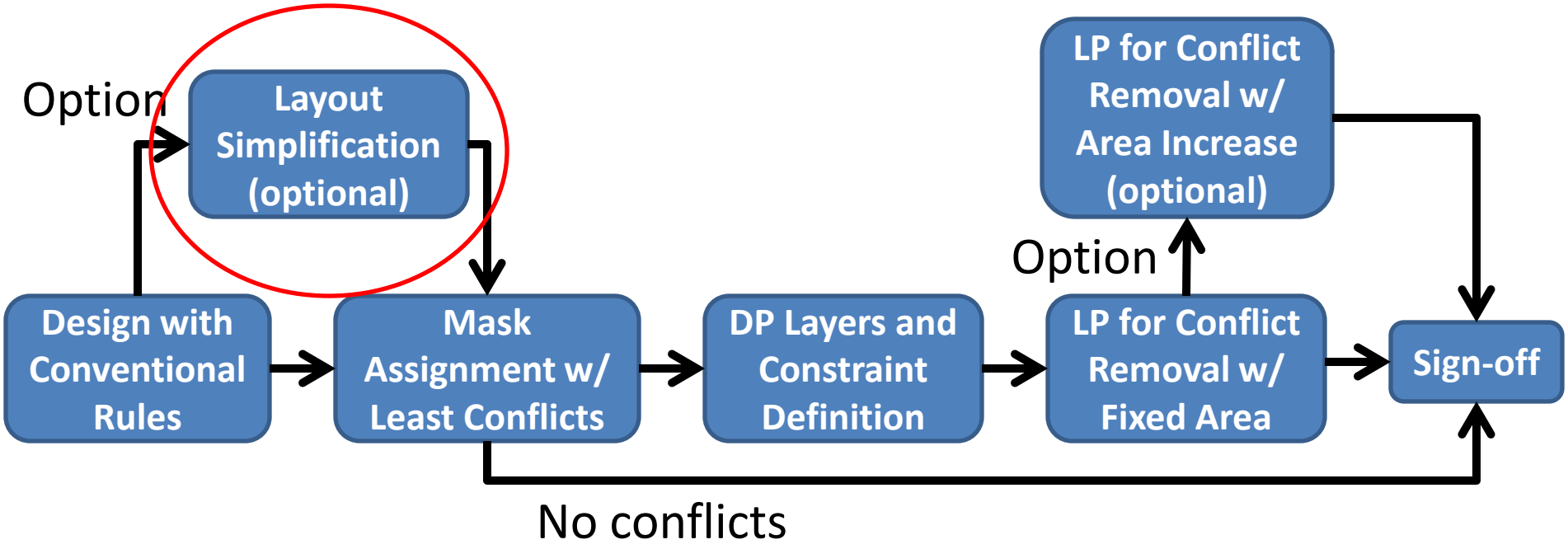
DP rules

$X_i$ = current location,
$X_{init}$ = initial location of edge $i$
$W_i$ = weight, $A_{ij}$ = arc b/w edges $i$ and $j$
$d_{ij}$ = DR value



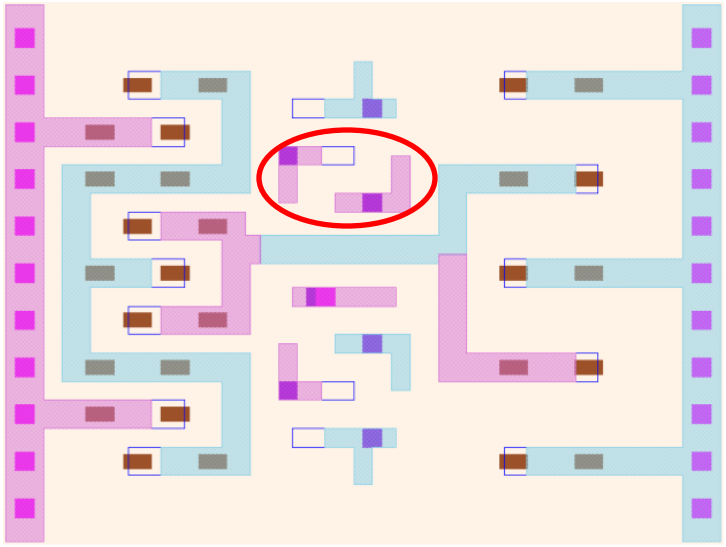

- LP formulation allows fast polynomial time solution
- Advantages of fixing coloring before legalization
  - Solving conflict on one layer cannot create another elsewhere
  - No need for iterative loop of coloring + legalization
  - Handling of spacing rules is clean

# Layout Simplification for More Efficient Conflict Removal

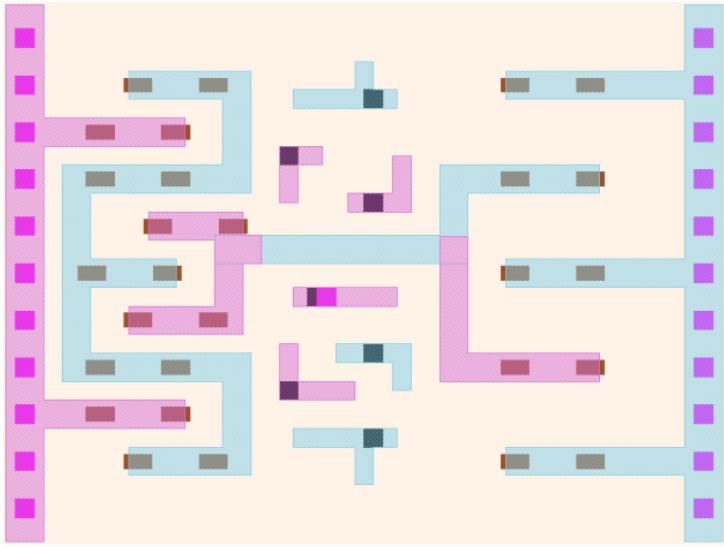


# Layout Simplification for More Efficient Conflict Removal

*Before legalization*



*After legalization*

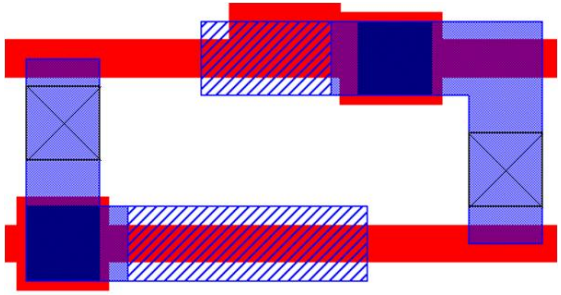


- Many conflicts on M1 are caused by segments for redundant contacts/vias or pin-access
  - These improve yield/routability but are not absolutely required

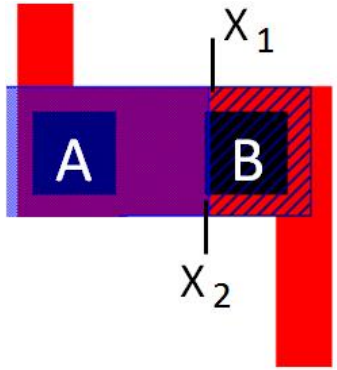
→ possible sacrifice of redundancy and extra pin segments for more efficient conflict removal

# Sacrificing Unnecessary Layout Features

Pin Segments



Redundant Contacts




Poly

New M1

Removed M1

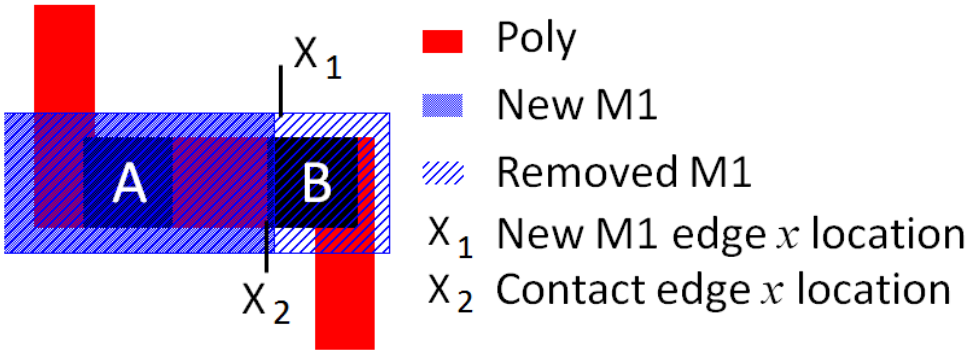
Via 1

$X_1$ New M1 edge $x$ location

$X_2$ Contact edge $x$ location

- Identify redundant CA and extra pin segments and remove them *before* coloring
- Add recommended constraints to add the features back after legalization

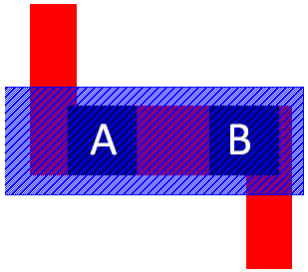
# Handling of Recommended Constraints



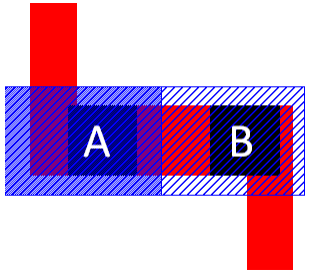

$$Min \quad \sum_i W_i |X_i - X_i^{init}| + \sum_{ij} W_{ij} r_{ij}$$
$$ST: \quad X_j - X_i \geq d_{ij}, \forall A_{ij}; r_{ij} \geq 0$$

$X_1 - X_2 + r_{12}$ = *contact width + M1 overlap past contact*

$r_{12} = 0$

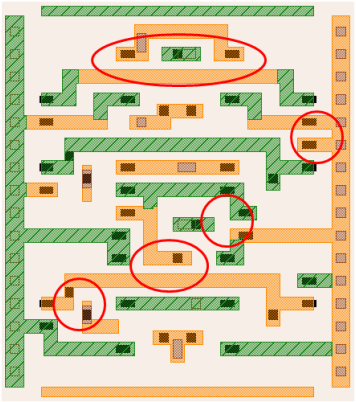



$r_{12} > 0$

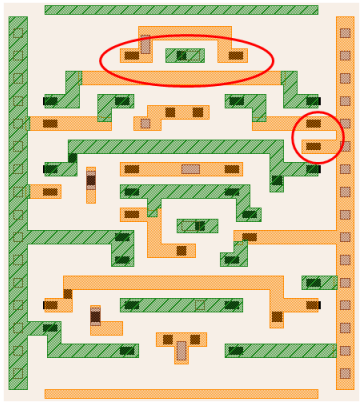



- Introduce $r_{ij}$ variable to relax the constraint
- Minimize $r_{ij}$ in objective function
- $r_{ij}$ minimization given less priority than non-recommended rules by assigning smaller weight $W_{ij}$

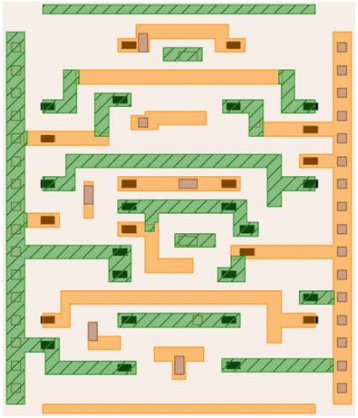
# Experimental Setup – Conflict Removal



Original
5 conflicts



Same area,
2 conflicts



No conflicts, 6.2% area increase

- Conflict removal results
  - Tested on commercial 22nm standard cells and macros
  - On dense M1, assumed to be double patterned
  - Min spacing = min width = 40nm
  - SS, TS, TT spacing rules = 80nm (i.e. 2X pitch relax.)
  - Results with fixed area and non-fixed area

# Conflict Removal Results

| | Original | | No Area Increase | | W/ Area Increase | | |
|---|---|---|---|---|---|---|---|
| Layout | N. Area | Conf. | Conf. | Sac. Red. CA | Conf. | Sac Red. CA | Area Increase |
| LCB + latch 1 | 1 | **1** | **0** | 0 | - | - | - |
| latch1 | 1.6 | **3** | **2** | 0 | 0 | 0 | 9.1% |
| oai | 1.6 | **2** | **0** | 1 | - | - | - |
| scan latch | 2.3 | **5** | **3** | 0 | **0** | 0 | 6.2% |
| xor | 2.4 | **2** | **0** | 0 | - | - | - |
| latch2 | 4.3 | **19** | **8** | 0 | **0** | 0 | 3.3% |
| nand4 | 4.7 | **4** | **0** | 0 | - | - | - |
| latch3 | 5.3 | **4** | **3** | 0 | **0** | 0 | 5.4% |
| nand3 | 6.7 | **7** | **0** | 0 | - | - | - |
| LCB control. 1 | 13.7 | **13** | **7** | 4 | **0** | 4 | 8.3% |
| LCB control. 2 | 50.3 | **53** | **31** | 1 | **0** | 2 | 9.1% |

- Conflict removal framework achieve DP-compatible cells
  - No area overhead for simple cells
  - Modest area overhead (at most 9%) for complex cells and macros
  - Few sacrificed redundant contacts (CA)
- Less than 1 min in real time for largest macro (460 trans.)

# Summary

- A novel framework to enable DP in the design
  - Conflict-free cells & designs w/ modest area overhead
  - Enables designing with conventional DRs
  - Shields designer from DP complexity
- Coloring method
  - Fast O(n)
  - Using all candidate stitches → guarantees conflict-free solution when it exists
- Automated DP conflict removal and layout legalization
  - Fast polynomial time solution using LP
  - Simultaneously across all layout layers
  - Minimizing layout perturbation
- Ongoing work: better stitch minimization heuristics

# Thank you for your attention!

Questions?