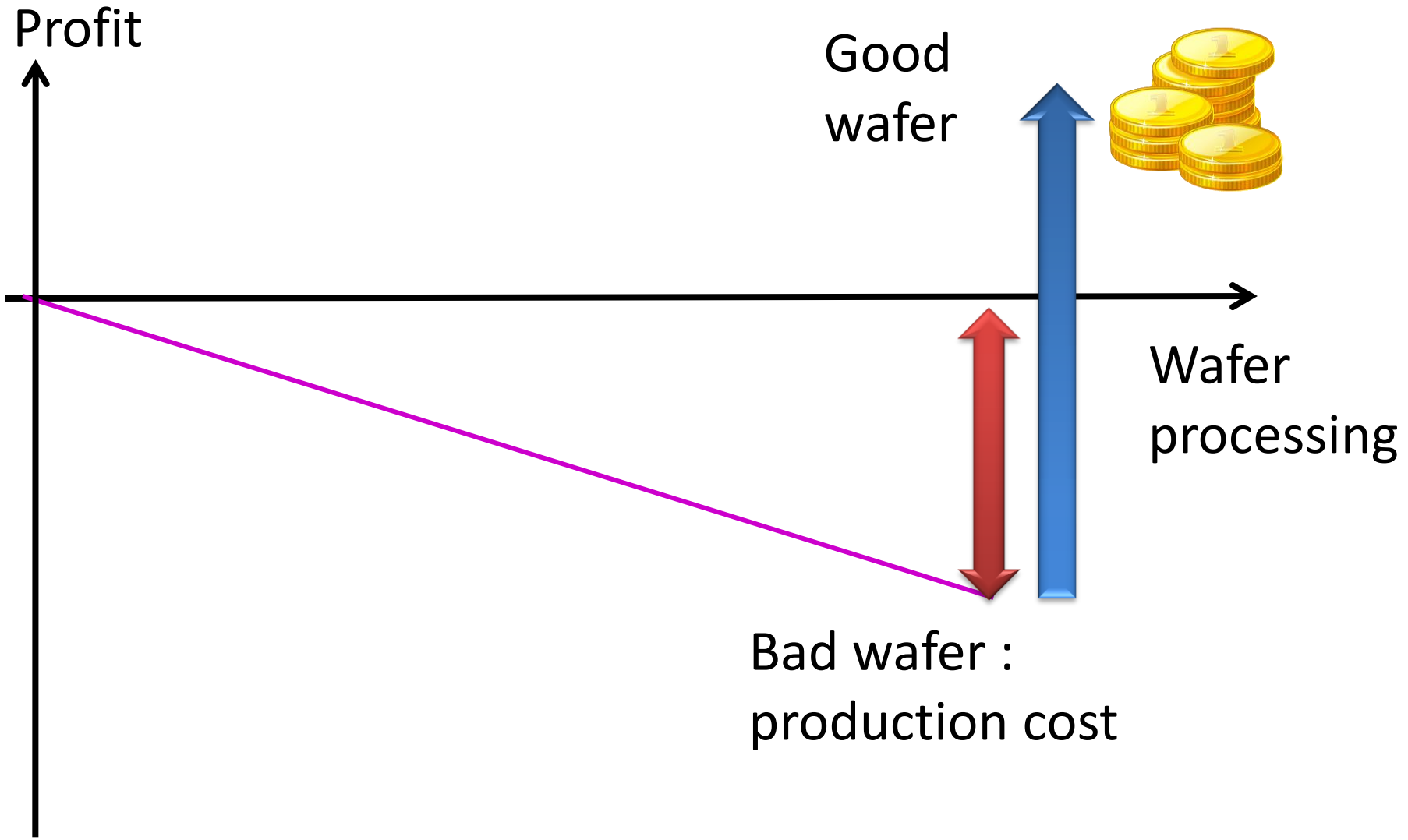
Design Dependent Process Monitoring for Back-end Manufacturing Cost Reduction

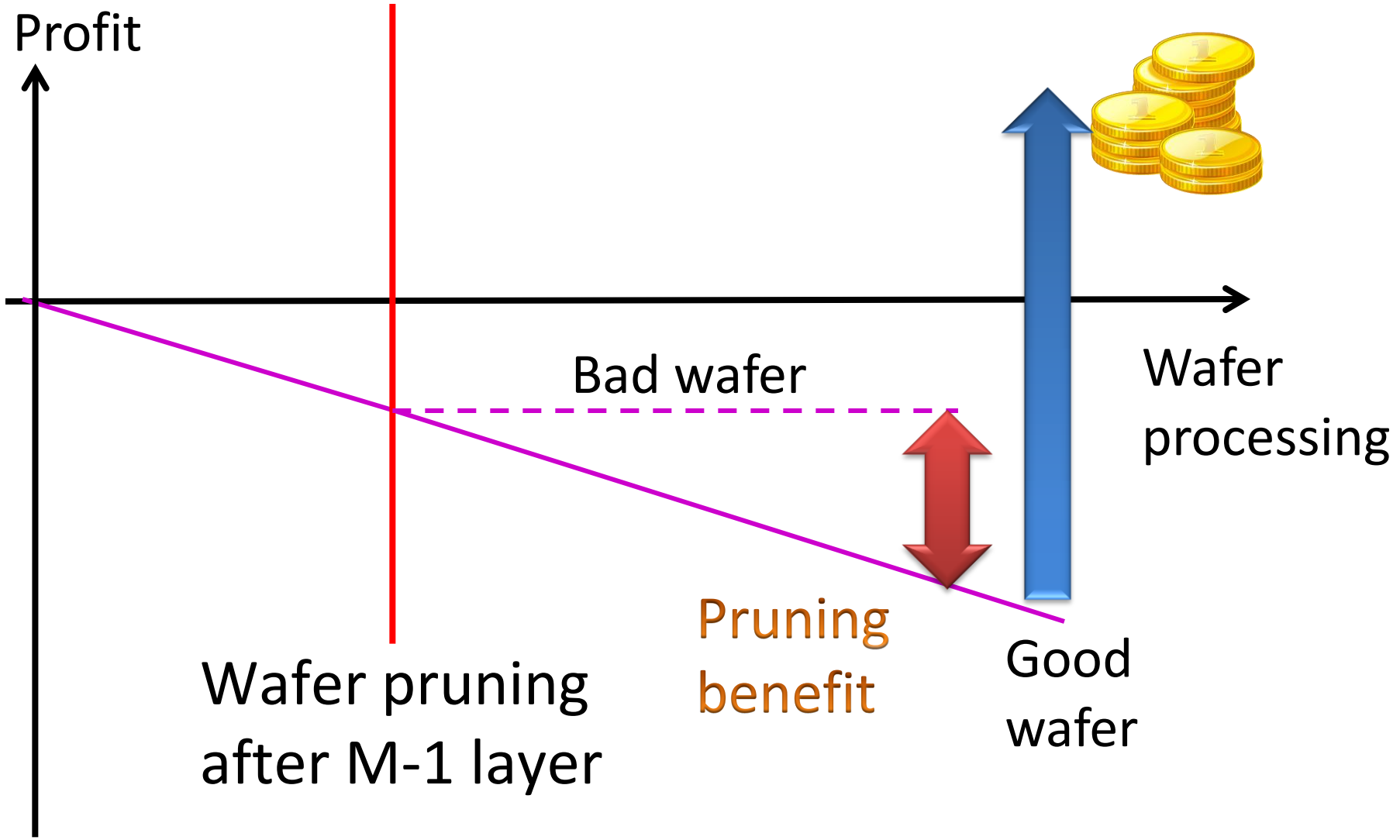
Authors:
[1]T.-B. Chan, [3]A. Pant, [2]L. Cheng & [1]P. Gupta
[1]University of California Los Angeles, [2]SanDisk,[3]Mentor Graphics
tuckie@ucla.edu

Acknowledgements :
SRC, IMPACT UC Discovery and NSF

Motivation of Early Wafer Pruning



Motivation of Early Wafer Pruning



The Challenge

- Estimate circuit performance early during manufacturing

Previous methods:

- Simple RO measurements
- Scribe-line device measurements

} design-independent

  - E.g., Ioff, Cg, Idsat, Ieff, etc

Proposed method :

- Use simple scribe-line measurements coupled with design-dependent parameters
  - ➢ No area overhead, test structures are always available on wafers for process control
  - ➢ Measurement after M-1
  - ➢ Capture design specific variation

Design Dependent Process Monitoring

Design dependent parameters

Process variation

$$circuit\ delay = delay_{\text{nominal}} + k_{nmos} \times \frac{\Delta I_{eff}^{nmos}}{I_{eff\ \text{nominal}}^{nmos}} + k_{pmos} \times \frac{\Delta I_{eff}^{pmos}}{I_{eff\ \text{nominal}}^{pmos}}$$

Delay and leakage power model

Design

Compressed design dependent parameters

wafer

Measured I-V , C-V values after M-1

Early Performance estimation

Wafer pruning

Scribe-line test structures

Delay Model

- Characterize nominal cell delay and its sensitivity to I_{eff}
- Estimate delay based on measurements from scribe-line test structures

Measured from test structures

Pre-characterized

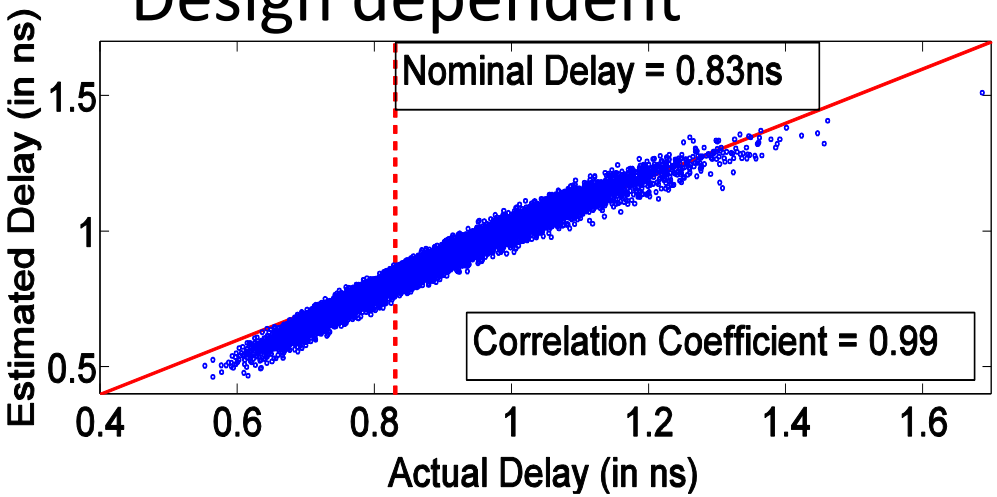
$$\text{Cell delay} = \text{Cell delay}_{\text{nom}} + \sum_{t} \left(\text{Sensitivity}^{t} \times \frac{\Delta I_{eff}^{t}}{I_{eff\ \text{nominal}}^{t}} \right)$$

Device types

$$\text{Path delay} = \left[\sum \text{Cell delay} - \text{Interconnect delay} + \text{Interconnect delay} \right] \times \frac{C_{\text{gate}}}{C_{\text{nominal}}}$$

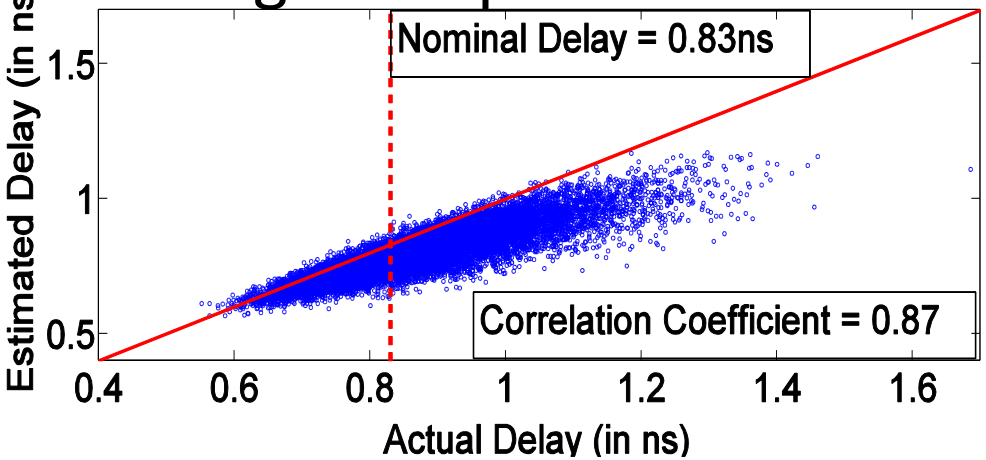
Design Dependent vs. Independent (timing)

Design dependent



$$\Delta\text{Cell delay} = \sum_t k^t \times \frac{\Delta I_{eff}^t}{I_{eff\ \text{nominal}}^t}$$

Design independent



$$\Delta\text{Cell delay} = \sum_t k \frac{\Delta I_{eff}^t}{I_{eff\ \text{nominal}}^t}$$

Leakage Power Model

- Model leakage power as a linear function of I_{off}
- Chip leakage power = ∑ cell leakage

Total number of instances of a cell type

Measured from test structures

$$\text{Leakage power} = \sum_{t} \sum_{c} N_c \alpha_c(t) I_{off}(i,t)$$

Device types

Cell types

Pre-characterized coefficient

Modeling Within Die variation

Timing (delay)

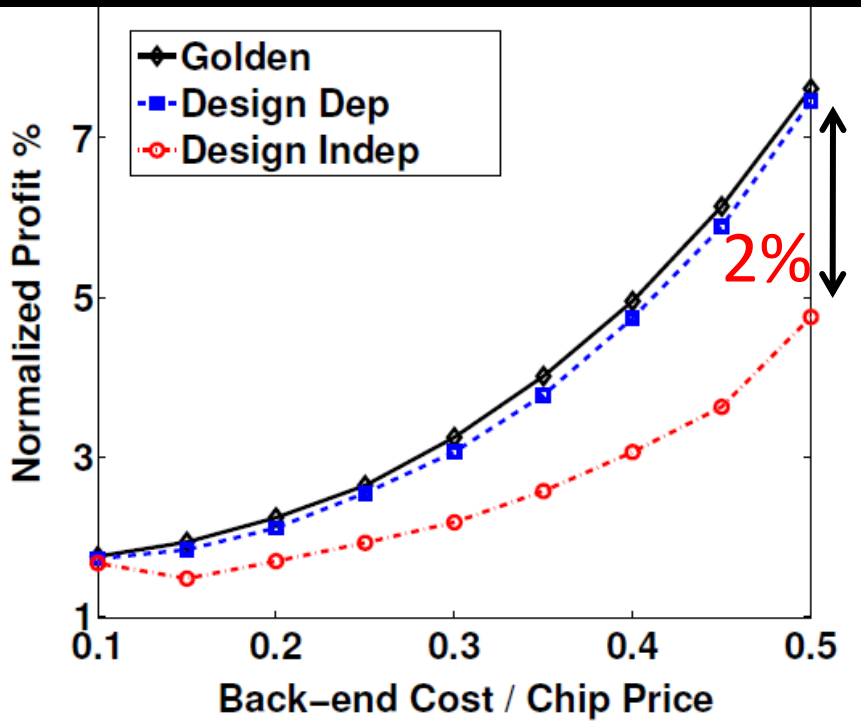
- Model I_{eff} of each device instance as normal random variable
- Estimate Δ delay distribution due to within die variation

Leakage power

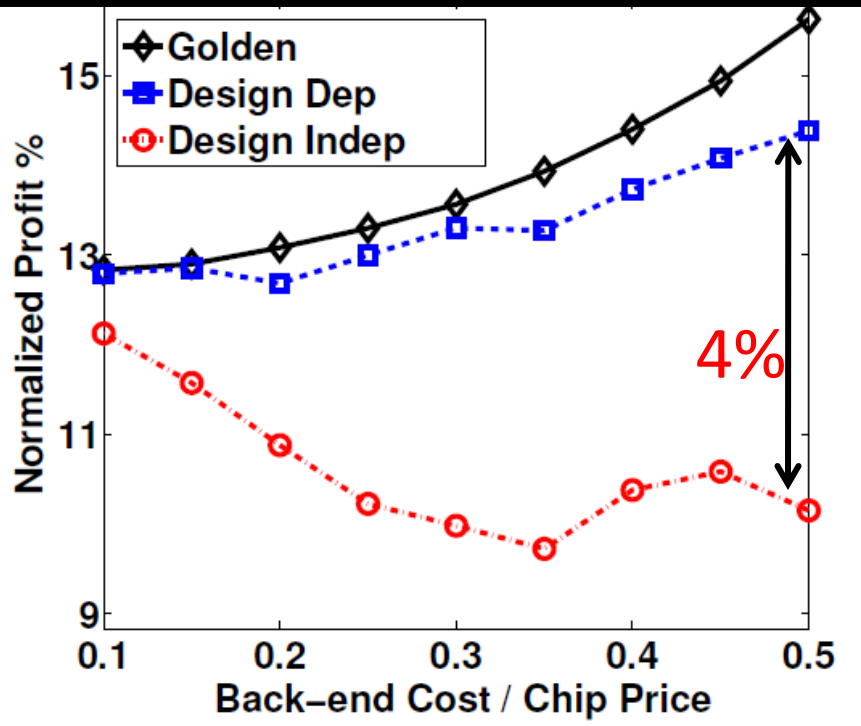
- Model I_{off} as an exponential function of variation sources
- Leakage power α exp (within–die variations)

Wafer Pruning Benefit

C432



MIPS



Normalized profit : $\frac{\text{Wafer Pruning Benefit}}{\text{Max possible number of good chips}}$

Reduce Measurement Noise

- **Connect multiples devices in parallel for measurement**
- **Increase number of measurements**
- **2-3% improvement with 5 repeated measurements and 10 devices under test**

# Measurements	# Devices on Test Structure	Wafer Pruning Threshold		
		25%	40%	50%
1	1	0.94	0.93	0.95
5	10	0.94	0.95	0.98
100	100	0.94	0.95	0.98

normalized to maximum achievable benefit from ideal wafer pruning

Conclusions and Ongoing Work

- Design dependent process monitoring improves early wafer pruning result by 2% to 4% of maximum achievable revenue

- Ongoing work
  - Die pruning to reduce testing cost
  - Lot pruning : discard a lot of wafers if good chips are below threshold

Thank you

Back up slides

Within Die Variation

Path delays with variation = $\begin{pmatrix} \text{Path delay \#1} \\ \text{Path delay \#2} \\ \vdots \\ \vdots \\ \text{Path delay \#n} \end{pmatrix} + \mathbf{W} \cdot \mathbf{I}_{\mathbf{eff\_wd}}$

Independent random variables

Correlation matrix

- **Use only a set of largest principle components of W**
  => reduces the size of W