UCLA

Incremental Gate Sizing for Late Process Changes

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Outline

1. Process change
2. ECO Costs
3. ECO Aware Design via LPECO
4. Experiments
5. Summary

Manufacturing process

- The foundry provides designers with a model of the **manufacturing process**
  - Information about the way transistors and interconnect
  - BSIM / PTM models, Liberty (.lib) model
- Model contains information about:
  - **Electrical parameters**: threshold voltage, saturation current, leakage current, I-V characteristics, interconnect resistance, capacitance, dielectric information
  - **Geometrical parameters**: gate length, gate width, source / gate / drain capacitance

Manufacuring Process Changes

- Aggressive schedules = uncertainty
  - From ITRS 2008:

Table DESN9 Design for Manufacturability Technology Requirements

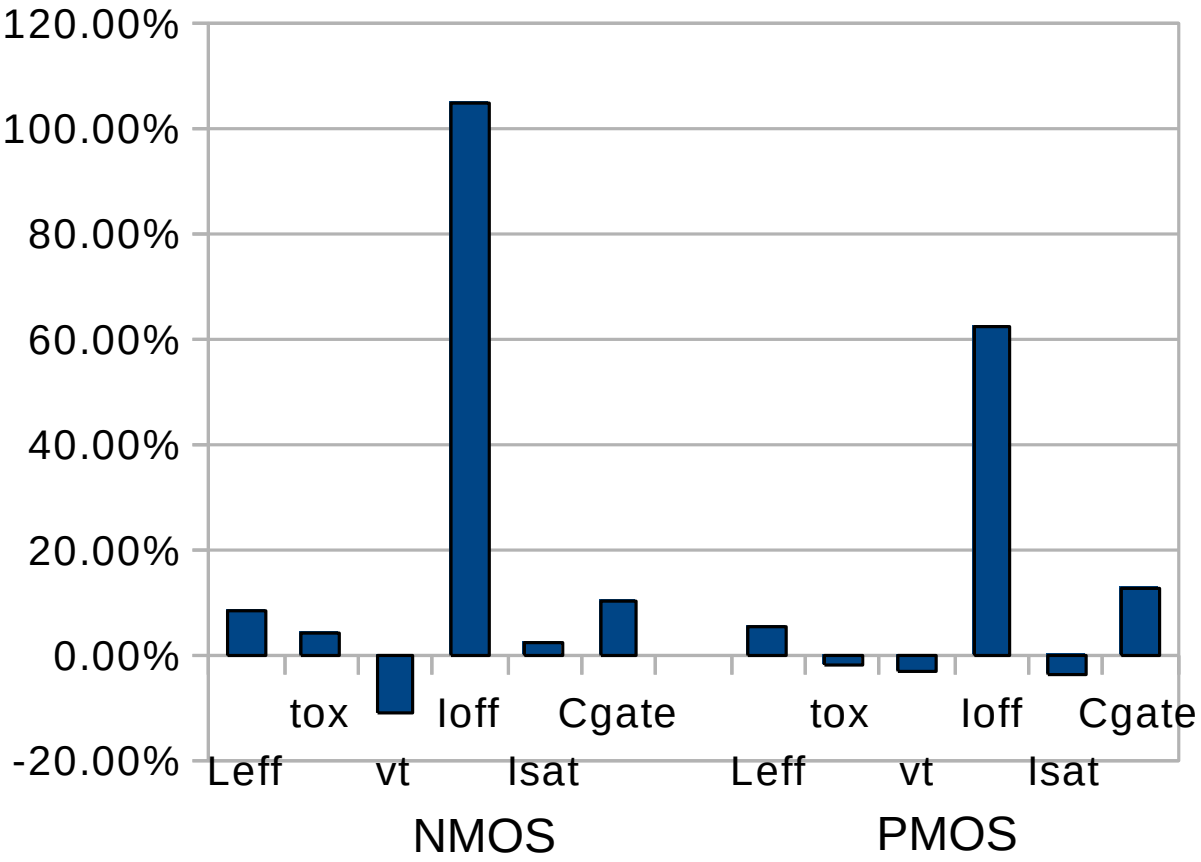
Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*
Normalized mask cost from public and IDM data	1	1.3	1.7	2.3	3	3.9
% V_{dd} variability: % variability seen in on-chip circuits	10%	10%	10%	10%	10%	10%
% V_{th} variability: doping variability impact on V_{th}, (minimum size devices, memory)	31%	35%	40%	40%	40%	58%
% V_{th} variability: includes all sources	33%	37%	42%	42%	42%	58%
% V_{th} variability: typical size logic devices, all sources	16%	18%	20%	20%	20%	26%
% CD variability	12%	12%	12%	12%	12%	12%
% circuit performance variability circuit comprising gates and wires	46%	48%	49%	51%	60%	63%
% circuit total power variability circuit comprising gates and wires	56%	57%	63%	68%	72%	76%
% circuit leakage power variability circuit comprising gates and wires	124%	143%	186%	229%	255%	281%

Solutions known, under development

Solutions not known

45nm Manufacturing Process change Example

- From April 2008 to March 2010
  - Real data from a commercial 45nm process



Engineering Change Order (ECO)

- Design changes that are made late in the design process are referred to as an **Engineering Change Order (ECO)**

Example:

HotFab Foundry provides Design Tech Inc. with an updated set of manufacturing parameters that decrease I_{sat} (the saturation current), causing their current designs to violate timing.

They fix their design using an ECO which includes changing the gate sizes (e.g. INV X1 -> INV X8), and routing changes

ECO = design / tool time + delays! (€€€ / $$$!)

ECOs should minimize implementation costs!

What does an ECO cost?

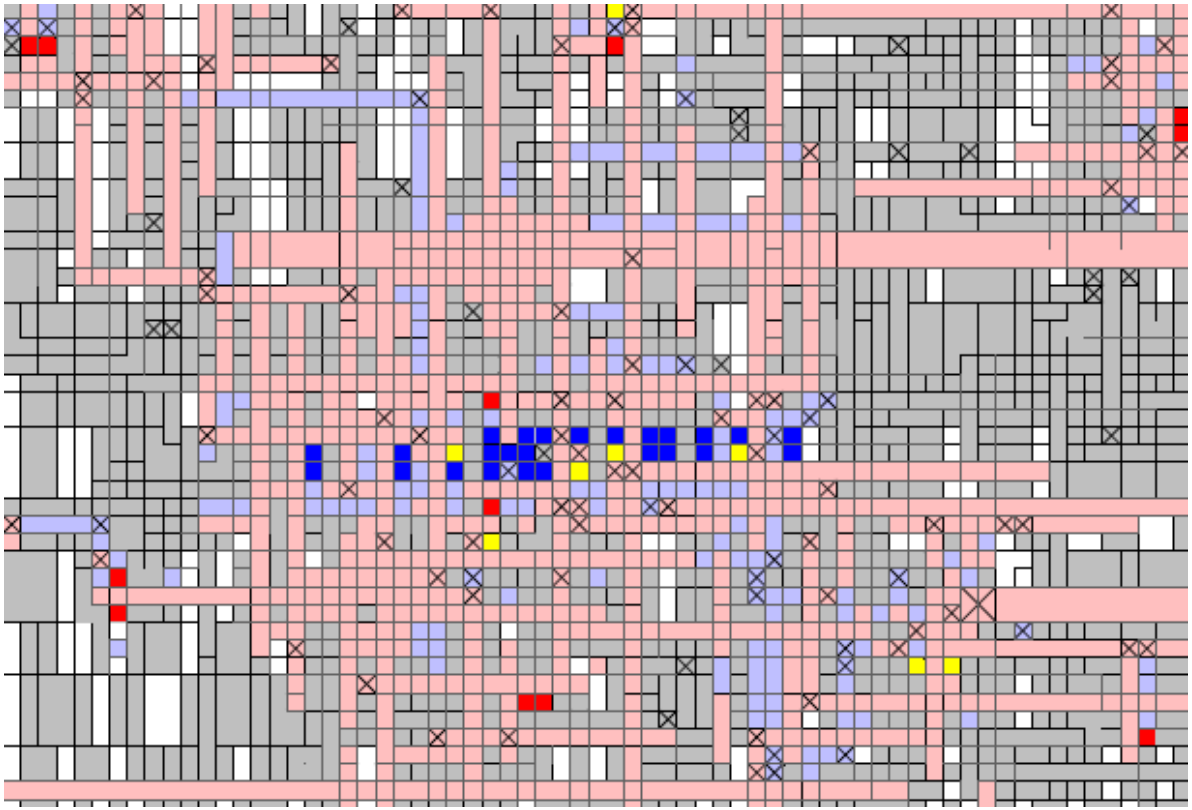
Legend

Added nets

Deleted nets

Moved cells

Resized cells



Quantify ECO cost → Guide Optimization

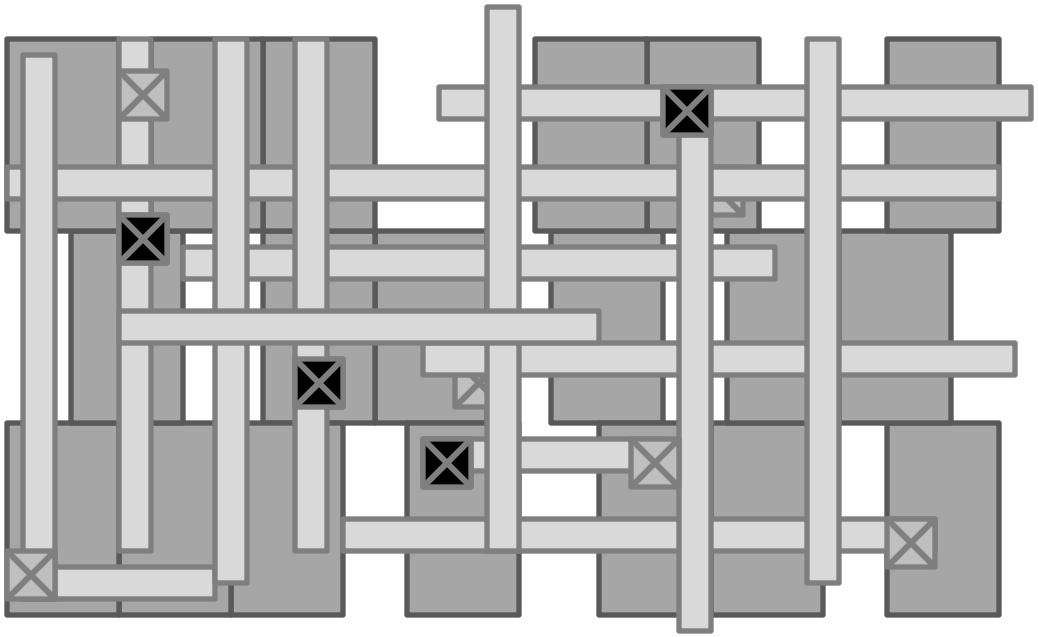
Proposed Measures for ECO Cost

- ECO Area Cost: Changed area
  - Amount of area that must be reanalyzed for
    - Parasitic Extraction & LVS / DRC
  - Potential layout errors to be corrected

- ECO Timing Cost: Changed timing
  - The effect of the ECO on the timing signal (circuit topology):
    - # of pins with unnecessary timing changes
      - The pin was not violating timing before the ECO
  - Changes cause slew, crosstalk violations, in paths that run through the ECO
  - Potential timing errors to be corrected

ECO Area Cost

- Measured as the amount of area, in μm^2 that has changed
  - Includes gate area, metal wires and vias



Estimating ECO Area Cost

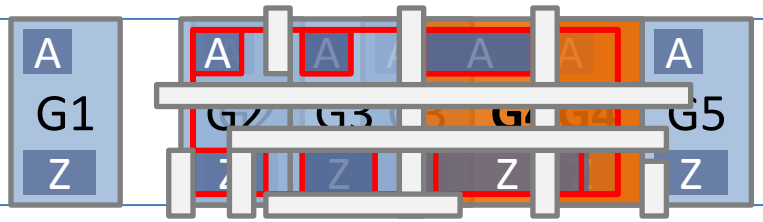
- Performing trial ECOs are too costly:
  - Impractical to try all possible ECO moves
  - Estimates of routing cost are needed to guide optimization
- Area Cost Estimated as a linear function of:
  - Number of changed pins
  - Number dislocated pins
    - Old and new locations do not overlap
  - Area of the pin bounding box
  - Congestion over the pin bounding box

Estimating ECO Area Cost

- Area Cost Estimate:
  - m_1: Number of affected pins
  - m_2: Number of dislocated pins *(old locations and new* locations do not overlap)
  - m_3: Pin bounding box area
  - m_4: Utilized area over pin bounding box *(routing over all layers*)

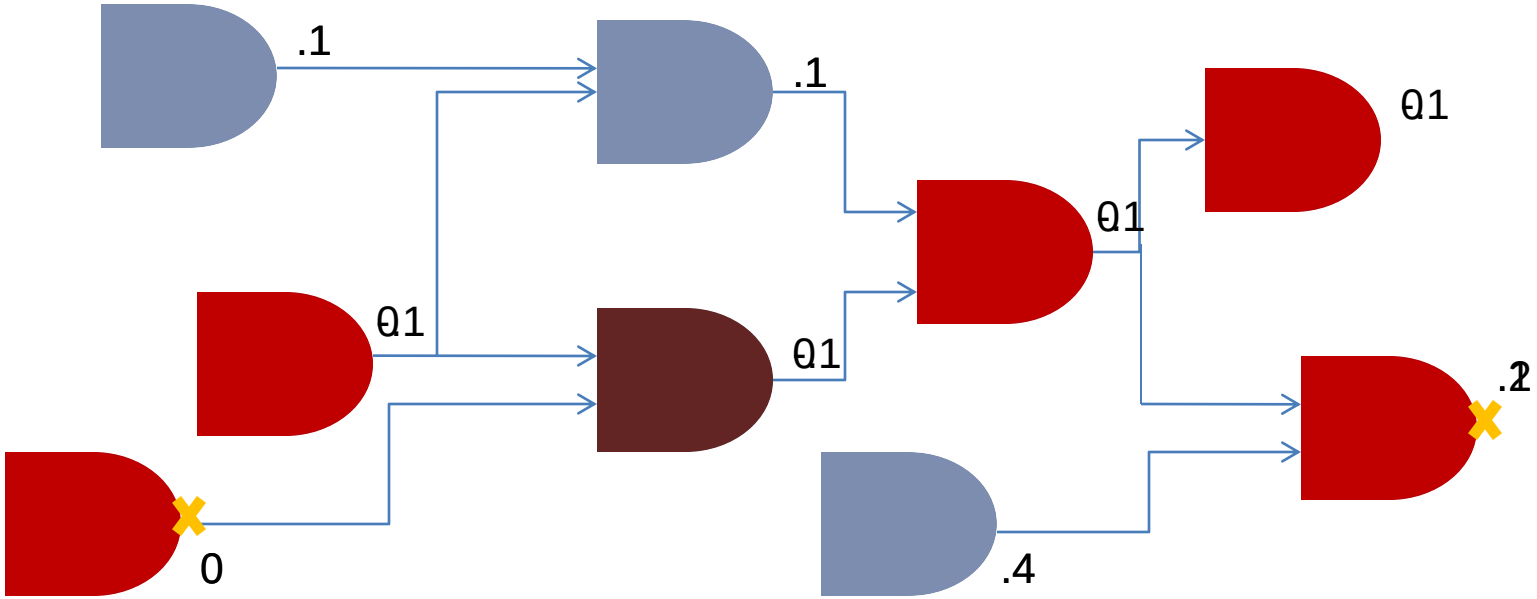
$$\hat{c}_{\text{area}} = \sum_{i=1}^{4} a_i m_i + b$$

$a_1 = 0.0367\ \mu m^2/\text{pin}$
$a_2 = 0.186\ \mu m^2/\text{pin}$
$a_3 = 5.35$
$a_4 = 9.65$
$b = .264\ \mu m2$



ECO Timing Cost

- Timing is affected downstream and upstream
- ECO Timing cost is defined as:
  - # of non-critical pins that are upstream and downstream from an ECO



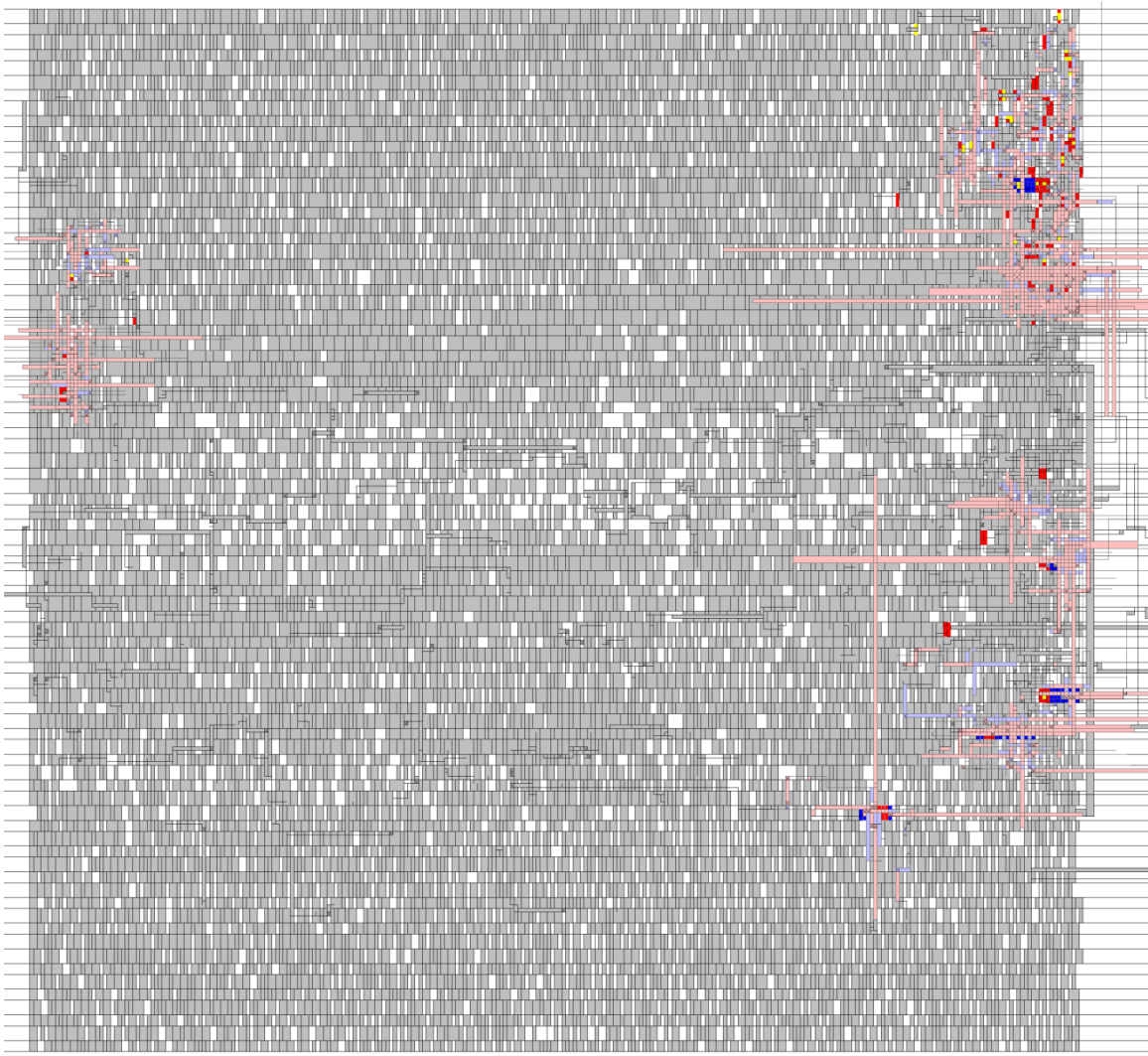
ECO Cost Example:

Timing cost:

118.9 μm^2

Pin Cost:

2838 pins



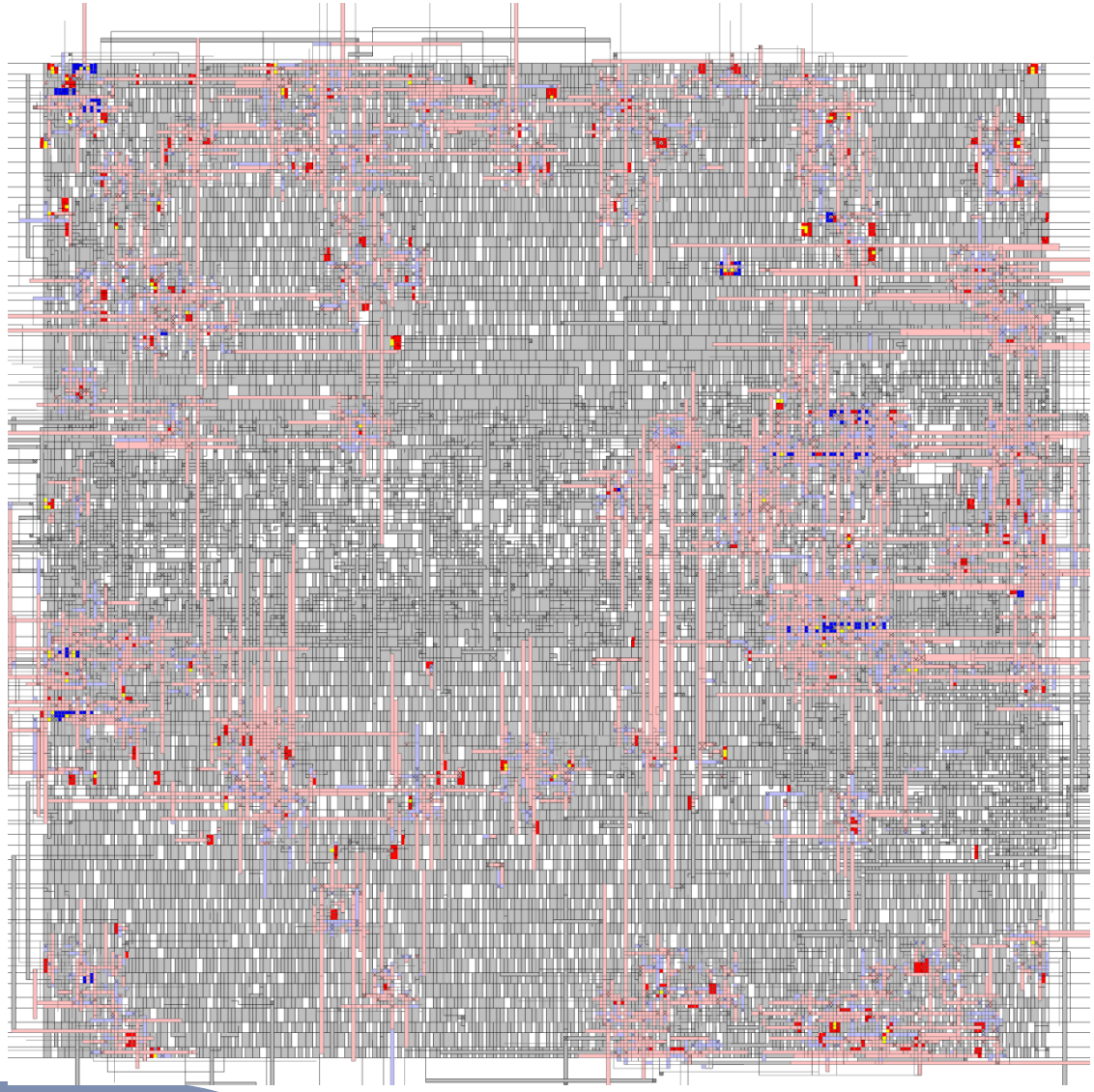
ECO Cost Example:

Timing cost:

586.6 μm^2

Pin Cost:

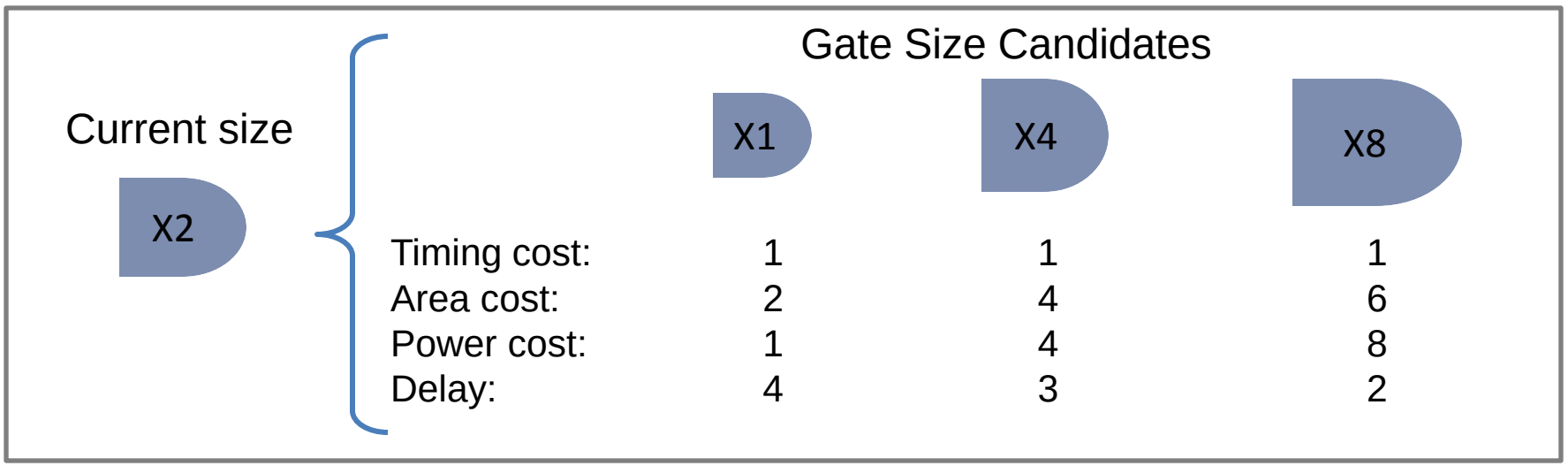
10198 pins



ECO-cost aware design via LPECO

- Linear programming based ECO gate sizing
  - Objective: ECO cost + Power cost
  - Constraints: Delay (timing closure)
  - Timing, power and ECO are modeled as a function of the candidate gate size

Example: Gate 1



ECO-cost aware design via LPECO

$$\text{minimize} \quad \sum_{i,k} p_{ik} y_{ik} + \gamma_t \hat{c}_{\text{timing}}(\text{y; x}) + \gamma_a \hat{c}_{\text{area}}(\text{y; x})$$

$$\text{subject to} \quad t_i + d_{i0} + \sum_k \delta_{ik} y_{ik} \le t_j, \quad \forall i \in \text{fo}(j)$$

$$t_i \le T_{\max}$$

$$\sum_k y_{ik} \le 1, \quad \forall i$$

$$0 \le y_{ik} \le 1$$

t : arrival time for gate i

d_{i0} : current delay for gate i

δ_{ik} : change in delay of gate i under size k

y_{ik} : assignment variable of gate i to size k

p_{ik} : change in leakage power of gate i to size k

(δ_{ik}, d_{i0} are from the commercial tool)

Example: Gate 1

Current size: X2

Gate Size Candidates

	X1 ($y_{11}=1$)	X4 ($y_{14}=1$)	X8 ($y_{18}=1$)
Timing cost:	1	1	1
Area cost:	2	4	6
Power cost:	-1 (p_{11})	3 (p_{11})	7 (p_{11})
Delay change:	4 (δ_{11})	3 (δ_{14})	2 (δ_{18})

Experimental Setup

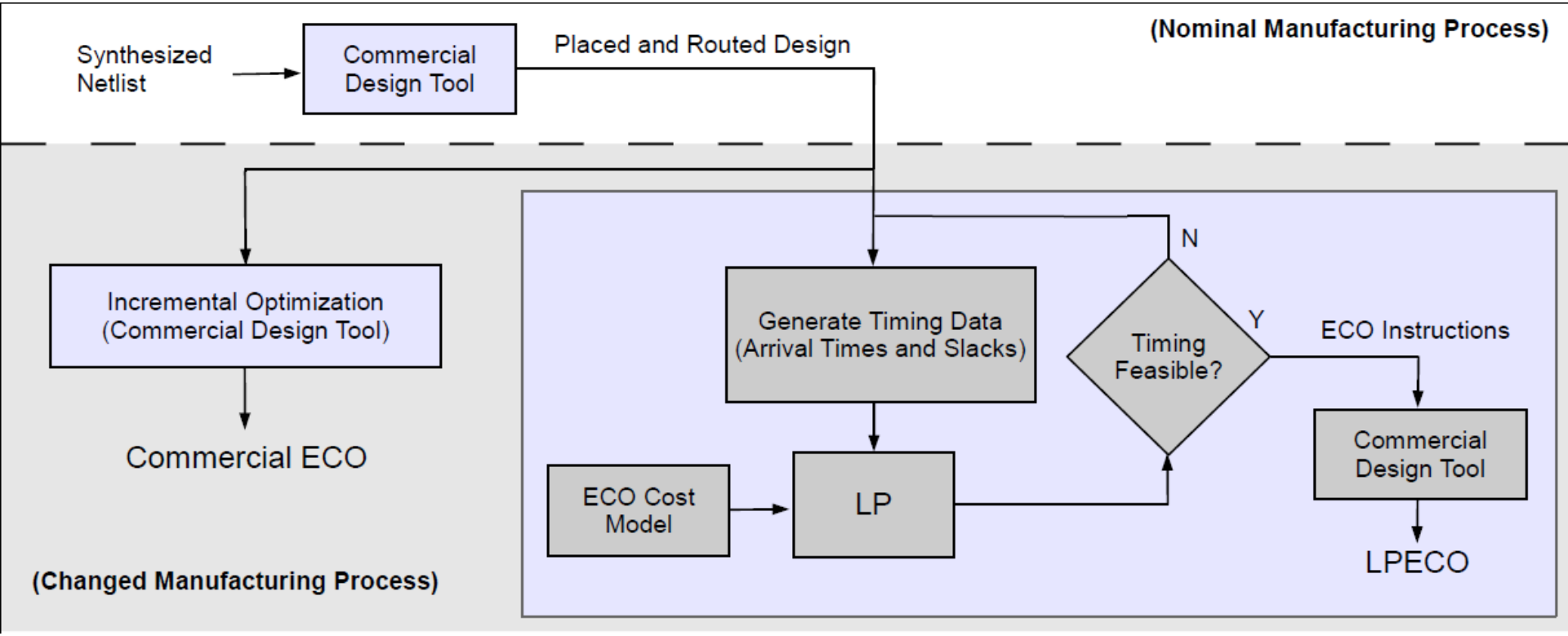
- 45nm Nangate Open Cell Library
- Manufacturing process change:

	Nmos	Pmos
V_{th}	-10%	-5%
t_{ox}	+5%	-5%
C_{gate}	+10%	+10%
l_{eff}	+5%	+5%

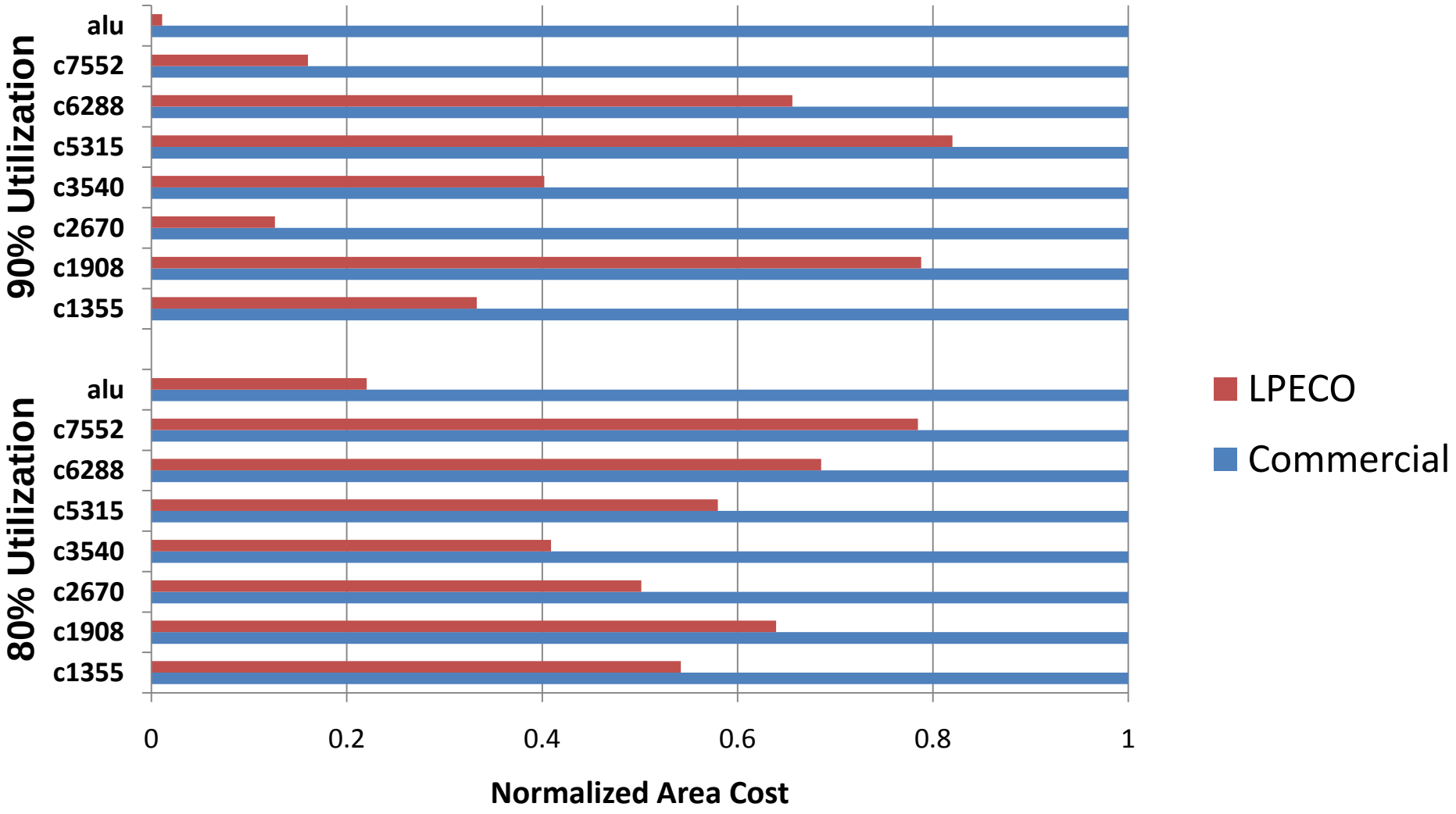
- ECO's are performed by a leading commercial design tool
- Runtime of LPECO ~.01 to 103s

Experimental Setup

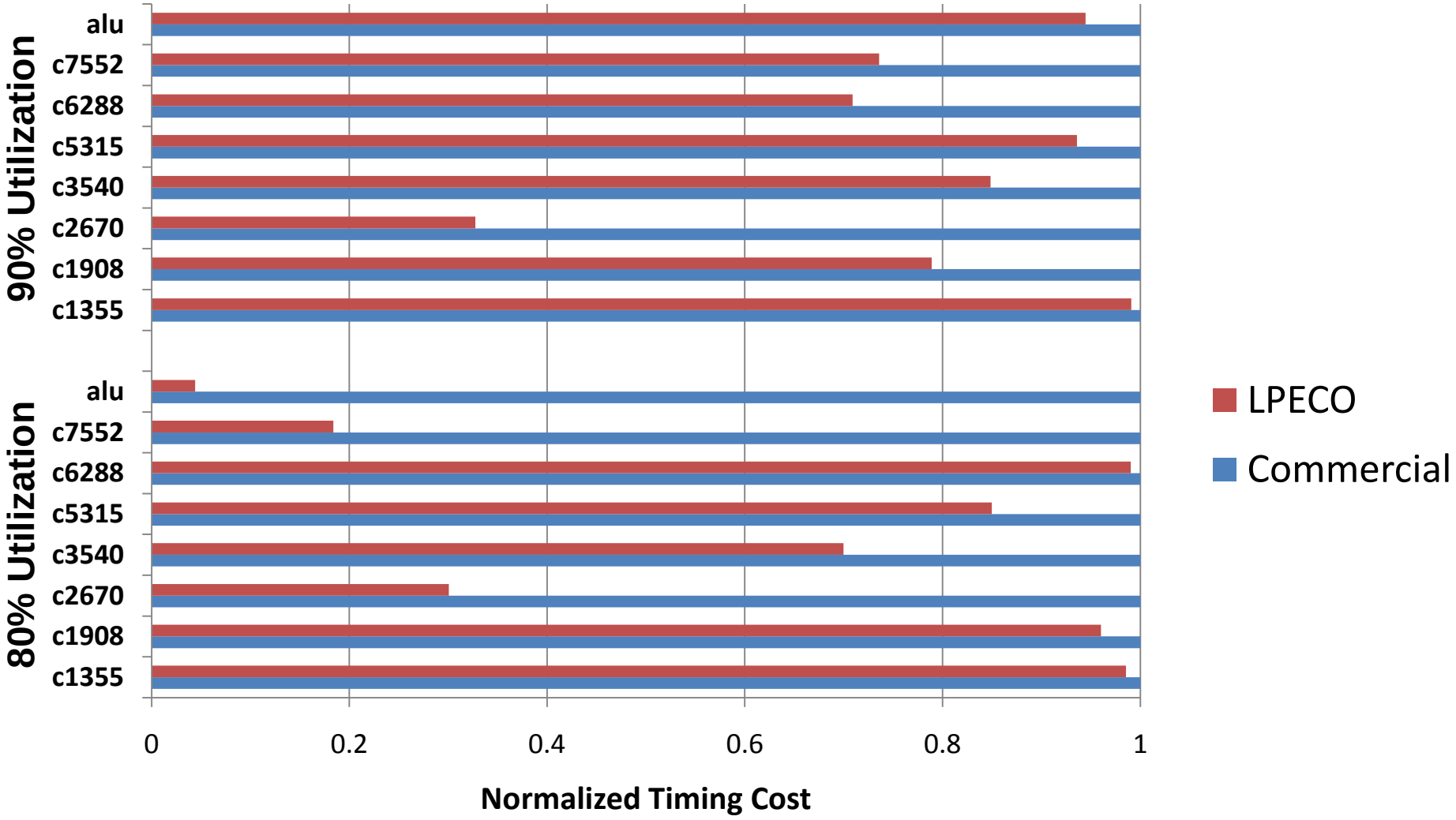
	Nmos	Pmos
V_{th}	-10%	-5%
t_{ox}	+5%	-5%
C_{gate}	+10%	+10%
l_{eff}	+5%	+5%



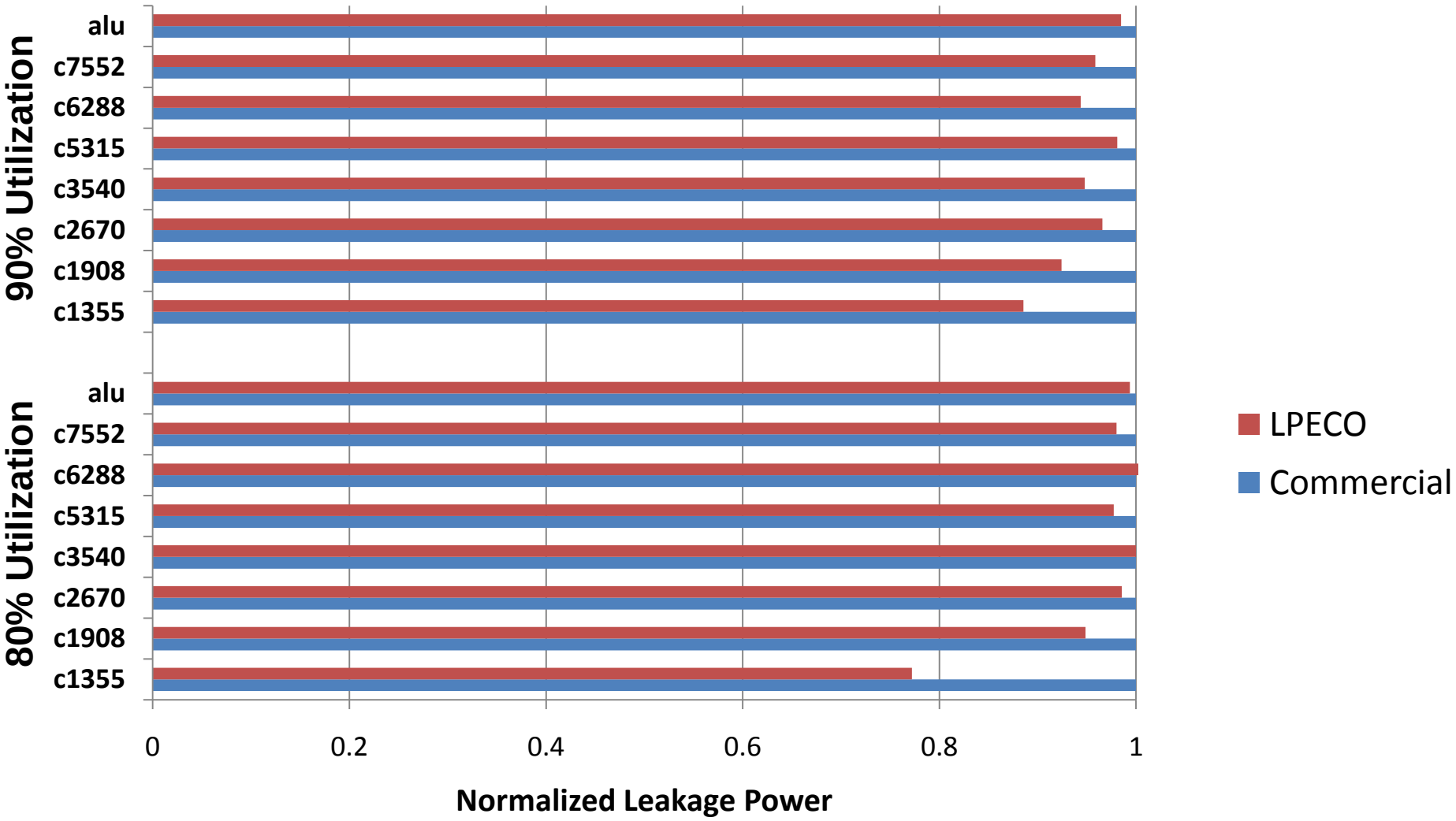
Results: Area Cost Comparison



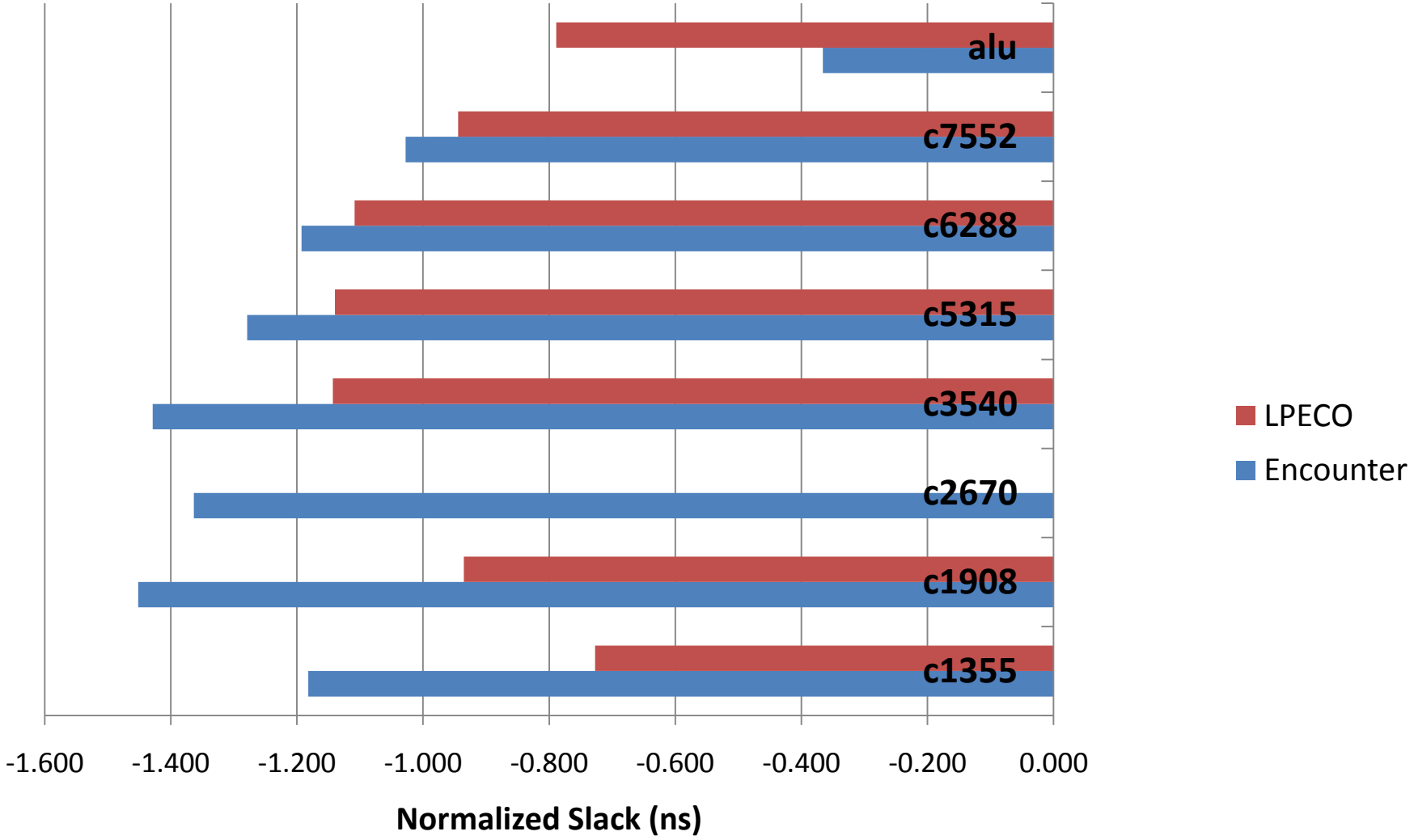
Results: Timing Cost Comparison



Results: Leakage Power



Results: Slack (Infeasible Cases)



(LP based timing closure)

Summary

- Quantified ECO Costs:
  - ECO Timing Cost
  - ECO Area Cost
- Performed incremental optimization to minimize ECO costs using LPECO
- Method performs well compared to commercial tool:
  - 22% to 88% reduction in ECO Area
  - 1% to 67% reduction in ECO Timing Cost
- Future goals:
  - Initial designs that incur small ECO penalties in the future
  - Large scale examples