UCLA

Measurement and Optimization of Electrical Process Window

Tuck-Boon Chan*, Abde Ali Kagalwalla, Puneet Gupta
Dept. of EE, University of California Los Angeles
(tuckie@ee.ucla.edu)

Work partly supported by NSF and UC Discovery IMPACT.

NanoCAD Lab

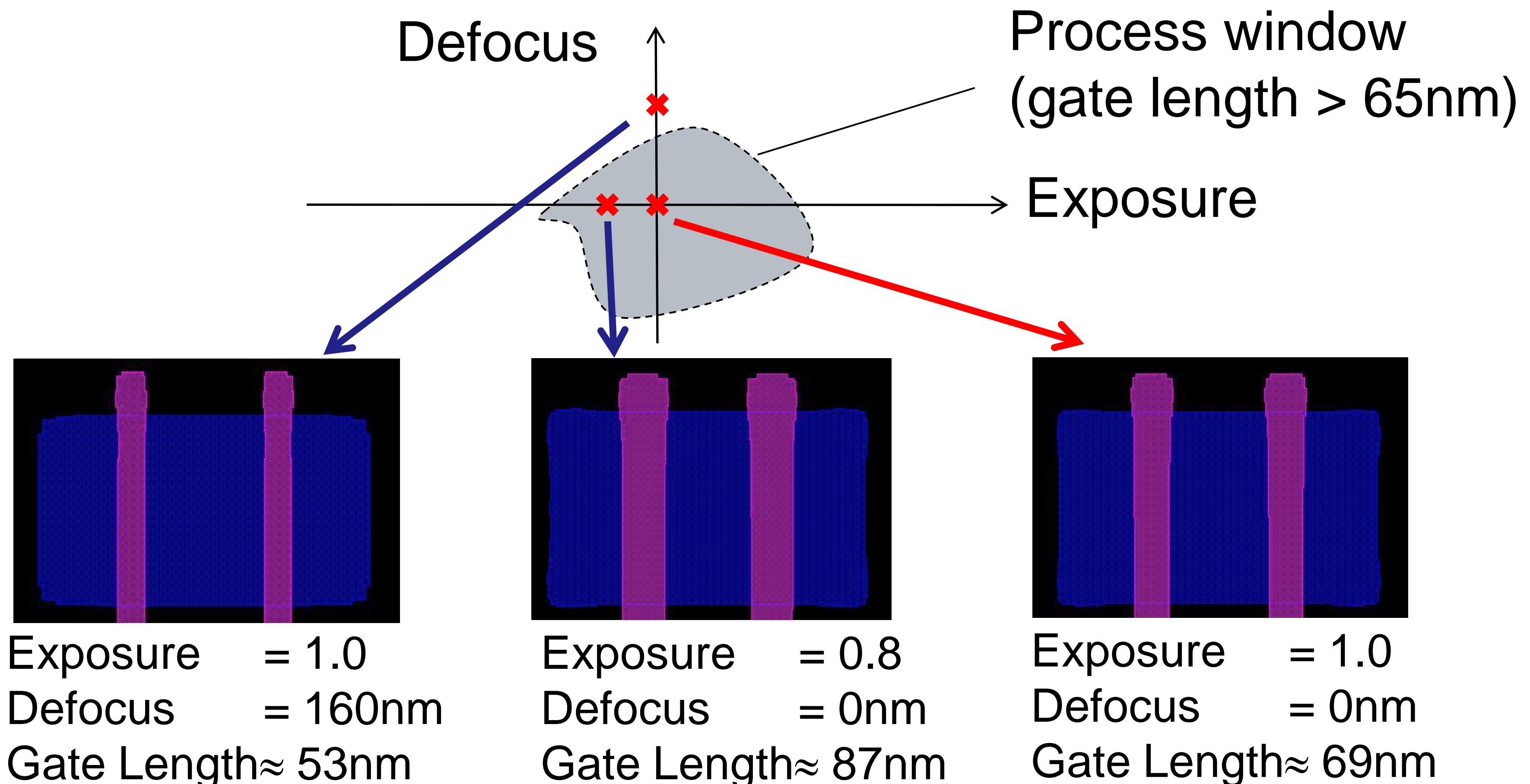
http://nanocad.ee.ucla.edu/

Outline

- Definition and evaluation of
  - Geometric Process Window (GPW)
  - Electrical Process Window (EPW)
- EPW vs GPW
- Improving EPW
- EPW Approximations

Process Window

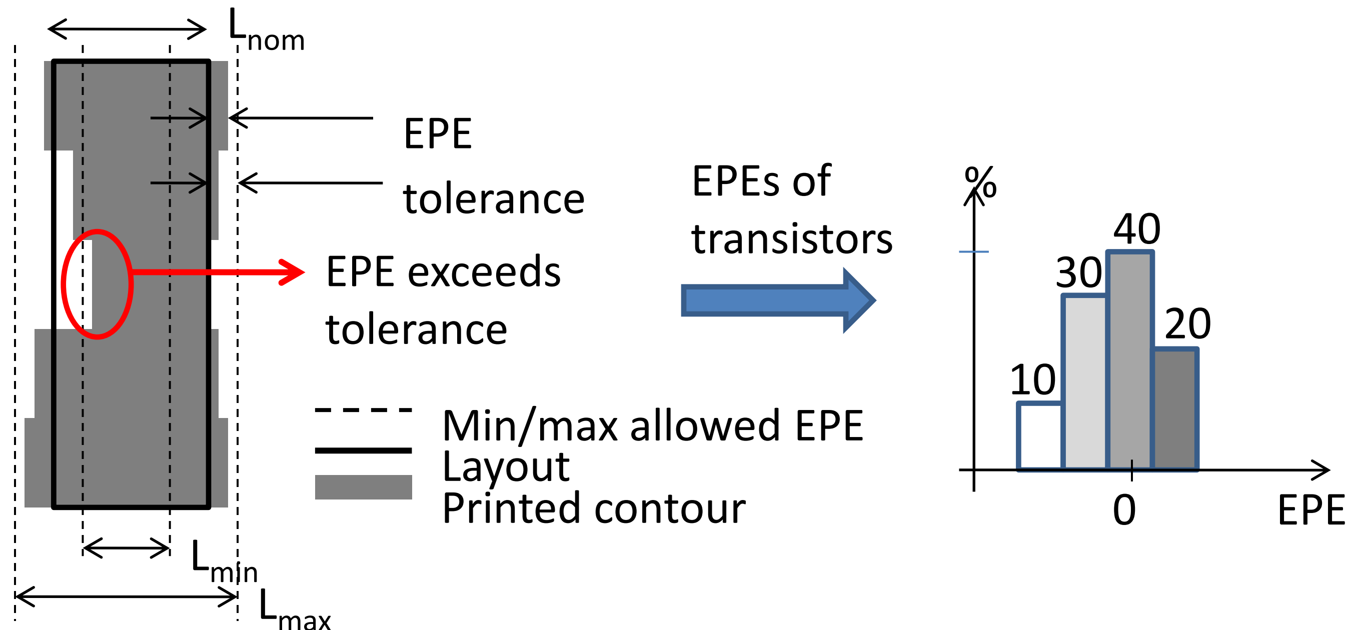
- Definition of process window:
  - The range of process parameters that allows circuits to operate under desired specifications [1].



[1] Mack, C. A., Legband, D. A., and Jug, S., "Data analysis for photolithography," Microelectron. Eng. 46(1-4), 65-68 (1999).

Geometric Process Window (GPW)

- Process parameters are within GPW iff |critical dimension (CD)| < allowed CD deviation
- Edge placement error (EPE)

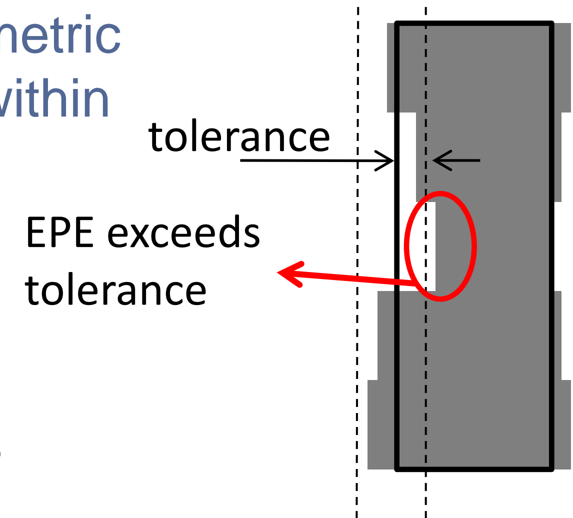


2 scenarios are considered :

1. CD = L_{nom} +/- 2*maximum EPE (W-GPW)
2. CD = L_{nom} +/- maximum EPE (A-GPW)

Problems of GPW

1. Geometric tolerance does not quantify changes in electrical specifications well.
   - ❖ Averaging across transistor segments
     - A transistor segment may violate geometric tolerance but the transistor can work within desired electrical specification
   - ❖ Averaging across multiple transistors
     - ∆Delay averages across critical path
     - ∆Power averages across all transistors



2. Not all shapes are critical but equal effort/resources are dedicated.

Electrical Process Window

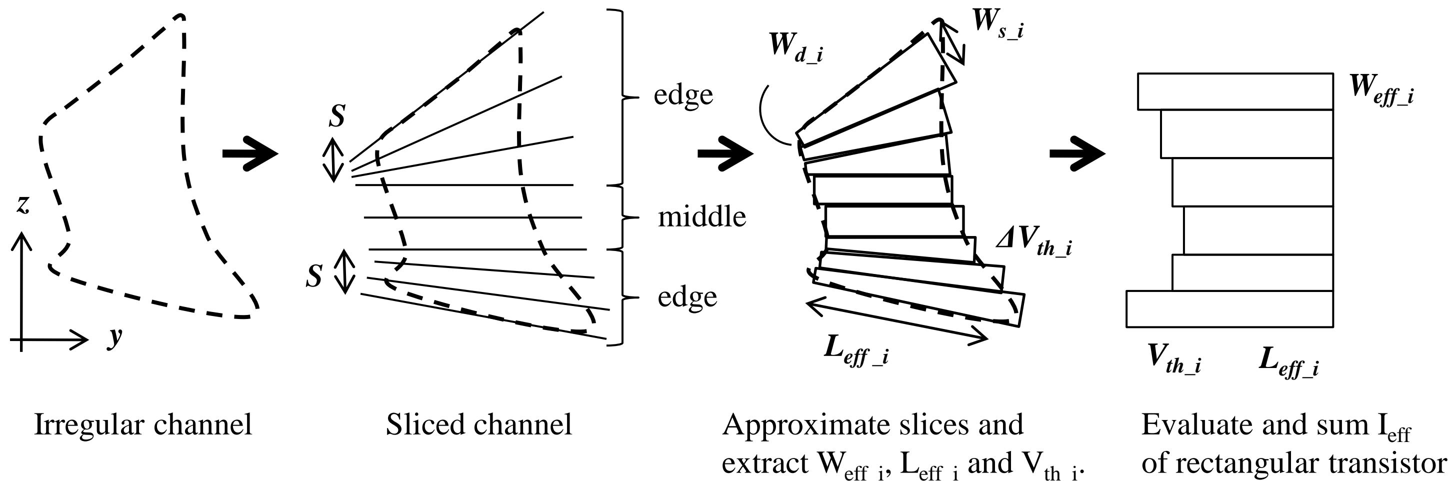
- A process point is considered within EPW iff

Lower bound of allowed circuit performance ≤ Circuit performance ≤ Upper bound of allowed circuit performance

- Need to extract circuit performance of printed contours
  - Modeling non-rectangular gate transistor
- Impact of interconnect linewidth variation is relatively smaller compared to the impact of gate length variation on transistor [2]
  - Width variation averages over long wires.
  - Resistance and capacitance change in opposite directions as line width changes.

[2] Chan, T.-B., Ghaida, R. S., and Gupta, P., .Electrical modeling of lithographic imperfections,. VLSI DESIGN (2010).

Modeling non-rectangular transistor [3]



Irregular channel | Sliced channel | Approximate slices and extract W_{eff_i}, L_{eff_i} and V_{th_i}. | Evaluate and sum I_{eff} of rectangular transistor

- Slice simulated transistor channel
- Calculate V_{th}, effective width and length of each slice
- Find the total I_{on} and I_{off}

[3] Chan, T.-B. and Gupta, P., .On electrical modeling of imperfect diffusion patterning,. *VLSI DESIGN* (2010).

Delay centric EPW (DEPW)

- A process point is considered within DEPW iff

Max(Δ path delay) ≤ Upper bound of allowed delay deviation

- Assume cell delay is inversely proportional to I_{on}

$$\text{Cell delay} = \frac{\sum_{j=1}^{N_i} I_{on-original-j}}{\sum_{j=1}^{N_i} I_{on-simulated-j}} \times \text{original cell delay}$$

Extract I_{on} from simulated contour and original layout

Obtained from timing report

- Path delay is the sum of delay of each cell

$$D_{path-simulated} = \sum_{i=1}^{M} (\text{Cell delay}_i)$$

Leakage Power Centric EPW (PEPW)

- A process point is considered within PEPW iff

Δ power ≤ Upper bound of allowed leakage power deviation

- Leakage power is proportional to I_{off}

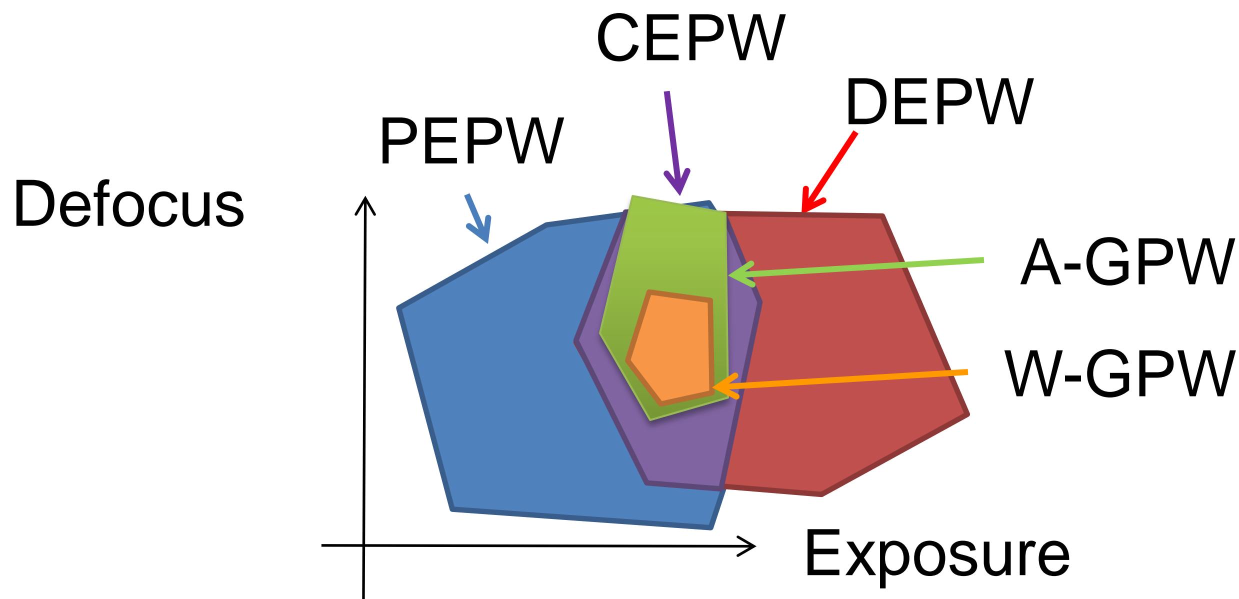
$$\Delta power = [\frac{\sum_{j=1}^{T} I_{off-simulated-j}}{\sum_{j=1}^{T} I_{off-original-j}} - 1] \times 100\%$$

Extract I_{off} from simulated contour and original layout

Combined EPW (CEPW)

- Process window of multiple electrical metrics : Intersection of EPWs

$$\text{CEPW} = \bigcap_{i=1}^{Q} (EPW_i)$$



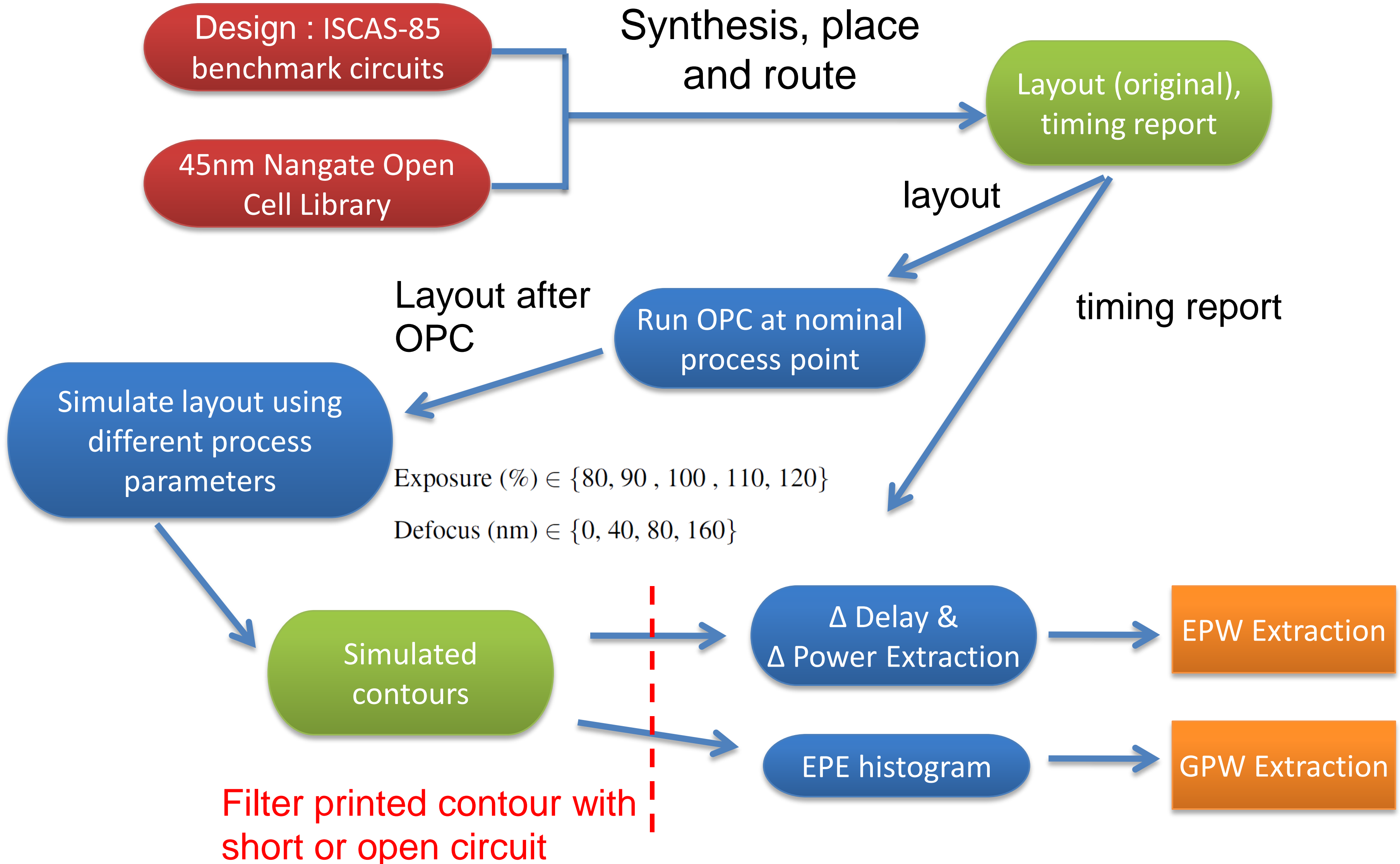
Relation between EPW and GPW

- GPW and EPW are defined differently
  - Need to know relation between them for fair comparison
- Simulate an INV (FO4) at worst case corners of W-GPW using SPICE, measure the delay and power deviation

Δ Channel length (%)	W-GPW Δ EPE (%)	A-GPW Δ EPE (%)	DEPW Δ delay (%)	PEPW Δ power (%)
5	2.5	5	11	54
10	5	10	21	311
15	7.5	15	30	2476

Use SPICE model and layout from 45nm Nangate Open Cell library (Vdd = 1.1V, Temperature = 25°C)

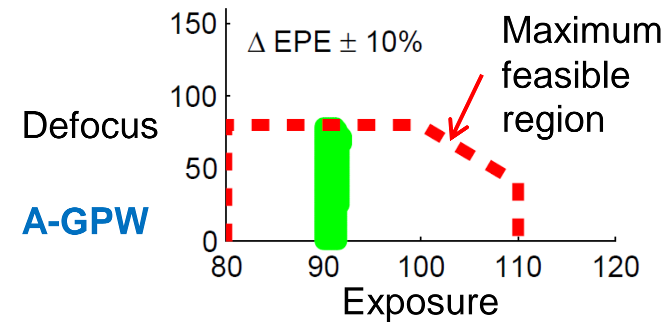
Analysis Flow

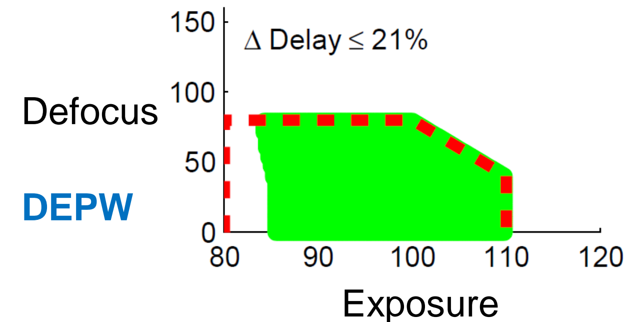


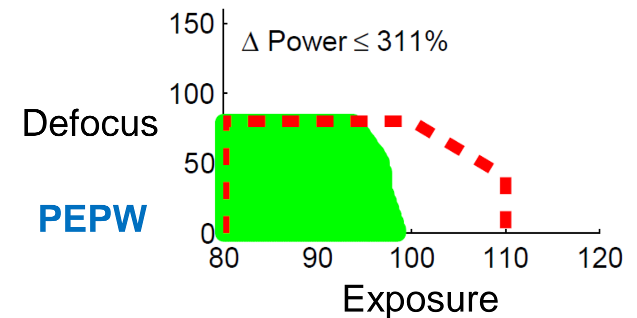
GPW vs EPW

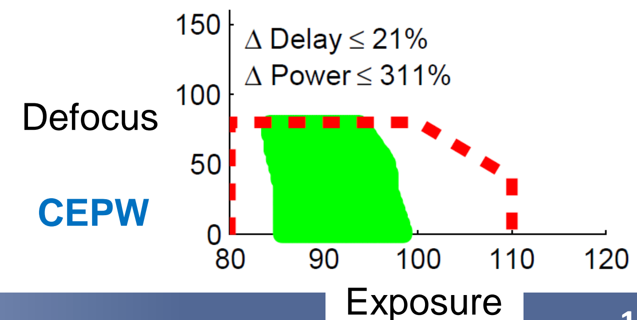
- GPW is pessimistic because
  1. GPW: Limit by worst transistor segment deviation

     EPW: Average deviation of each transistor segment
  2. Averaging across multiple transistors
     - ΔDelay averages across critical path
     - ΔPower averages across all transistors
  3. All transistors are not equally important => Delay constraint is applied on critical path only
- EPW is 1.5 to 6X larger than AGPW on average



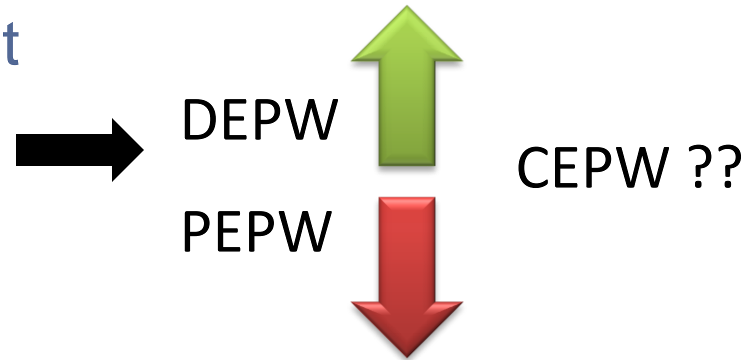






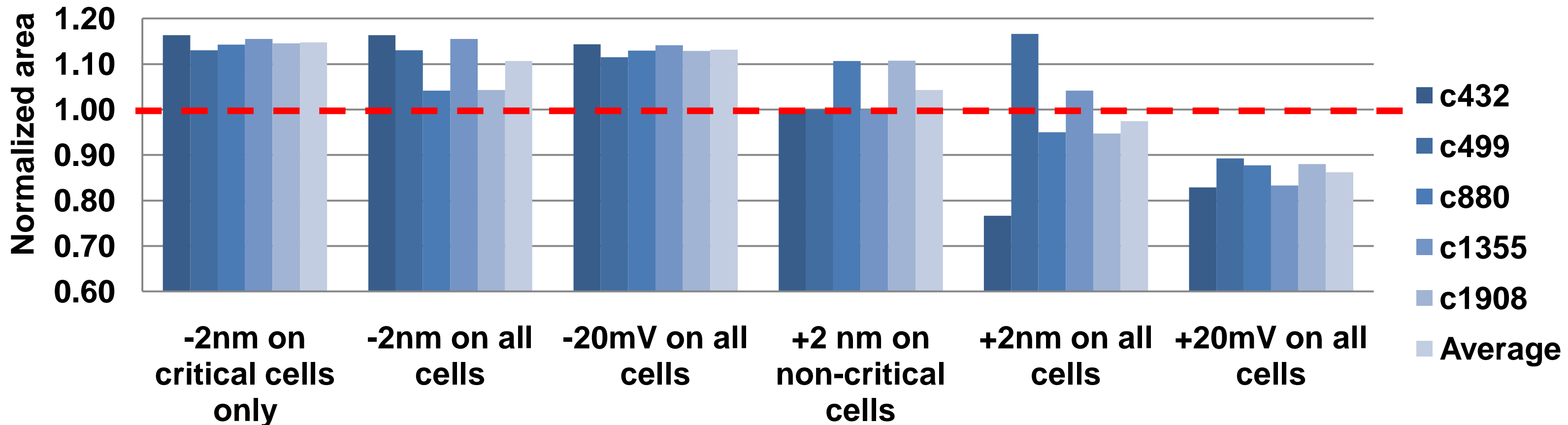
Improving EPWs

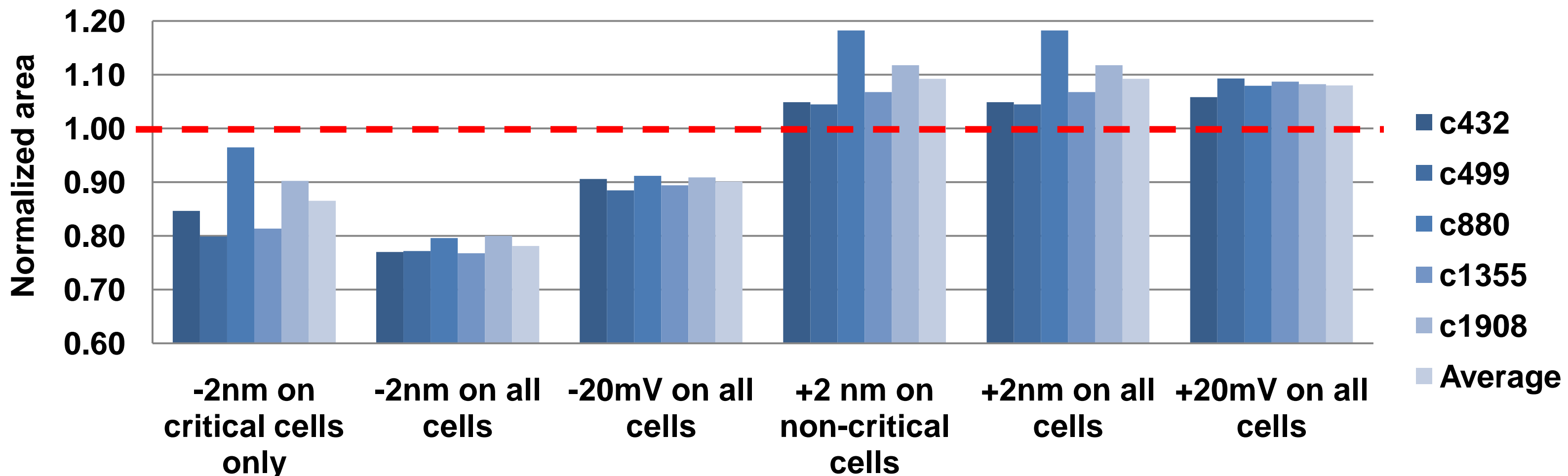
- Layout transparent process tuning
  - Avoid major change in layout
- Increasing V_{th} or gate length



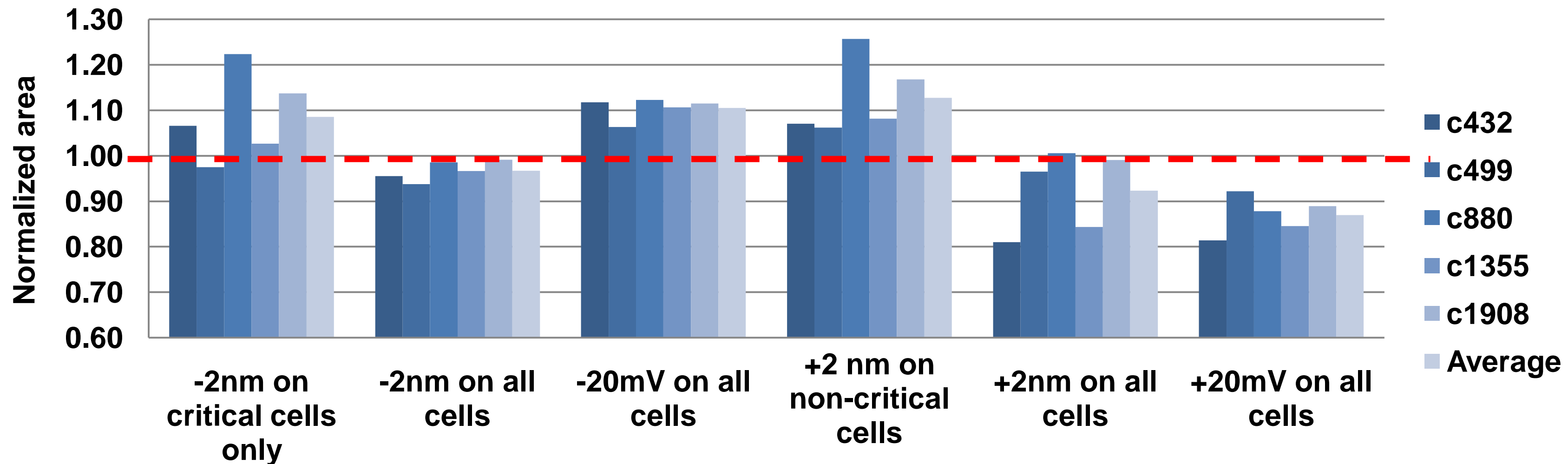
- We tried :
  - -2nm on critical cells
  - +2nm on non-critical cells
  - +/-2nm on all cells (i.e., a global CD push)
  - +/-20mV on all cells (i.e., a global Vth push)

Improved DEPW and PEPW





Improved CEPW



- Reducing V_{th} on all cells
  - Improves CEPW consistently
  - Can be done without knowing the locations of critical cells
  - -2nm gate length bias does not work as well due to increased pinching

EPW Approximation

Motivation: Critical path of a design may not be provided to lithography process

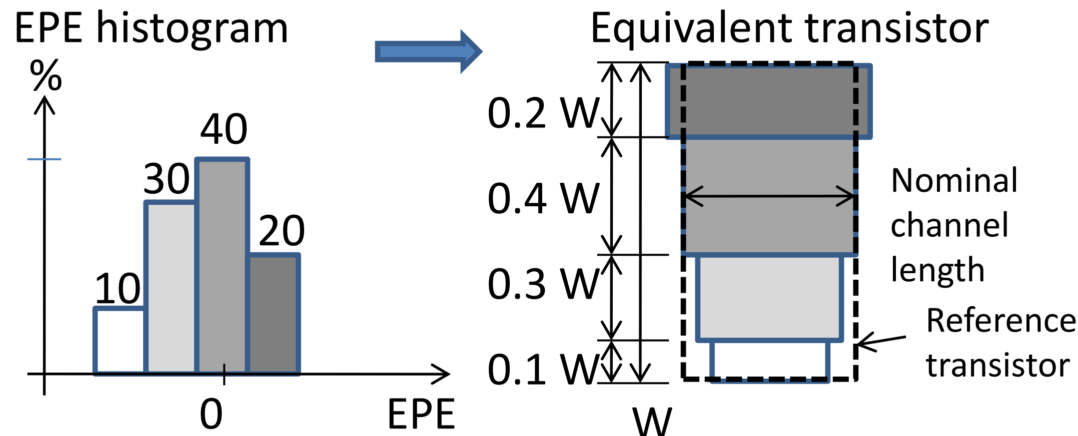
Method 1 : Use EPE histogram generated in OPC

- Estimate EPW without extracting channel shape of each transistor
- Approximate average delay and power deviation induced by EPEs of all transistors as an equivalent transistor

Process point

$$\in \text{histogram-DEPW} \Longleftrightarrow [\frac{I_{on-reference-transistor}}{I_{on-equivalent-transistor}} - 1] \times 100\% \leq \text{upper bound of allowed delay deviation}$$

$$\in \text{histogram-PEPW} \Longleftrightarrow [\frac{I_{off-equivalent-transistor}}{I_{off-reference-transistor}} - 1] \times 100\% \leq \text{upper bound of allowed power deviation}$$



Method 2 : Use the shape of every transistor

- I_{off} of each transistor is available => No approximation on PEPW
- Delay deviation of each transistor :

$$\Delta Delay = [\frac{I_{on-original}}{I_{on-simulated}} - 1] \times 100\%$$

- A process point is considered within DEPW iff

$$\underbrace{\frac{\sum_{n=1}^{R} \Delta Delay_n}{R}} \leq \text{upper bound of allowed delay deviation}$$

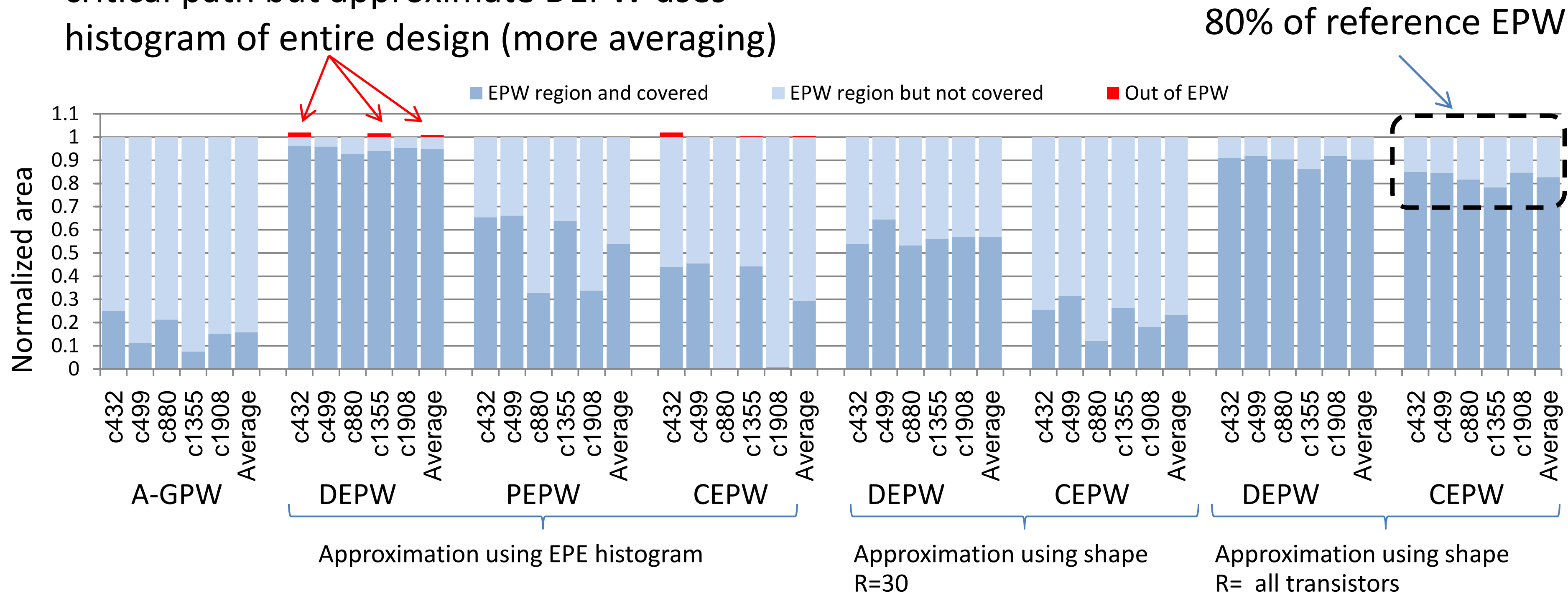
Average delay deviation of R transistors with worst delay deviation

- R= 1 , Lower bound of DEPW but too pessimistic
- R= 30, Critical path is usually more than one transistor
  => Average transistor stages along critical path
- R= Total transistors, Assume EPE distribution on critical path is similar to that of all transistor

Approximation quality

Reference DEPW only consider transistor along critical path but approximate DEPW uses histogram of entire design (more averaging)

80% of reference EPW



- All approximations have better area coverage compared to A-GPW
- Low area coverage in histogram-PEPW leads to poor coverage in histogram-CEPW
- Approximation using the shape of each transistor is the best:
  - No area out of EPW, covered 80% area of reference EPW

Summary

- We propose EPW which is a better measure of process window than conventional GPW
- Area of EPW is 1.5 to 6 times larger than that of GPW on average
- Layout transparent methods can improve EPW by 10%
- Approximation to EPW covers 80% of the area of reference EPW for all benchmark circuits
- Future work: Analyzing only representative layouts
  - Reduce lithography simulation runtime in EPW calculation
  - Can be used for OPC recipe optimization

Backup slides

Results: EPW Approximations