On Electrical Modeling of Imperfect Diffusion Patterning

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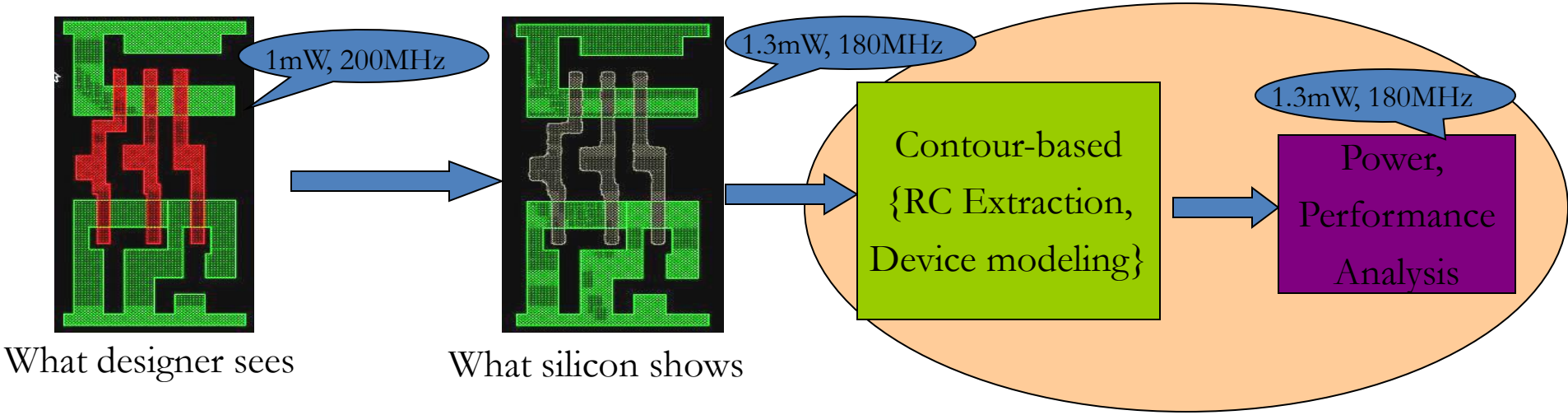
Outline

- Motivation
- Modeling Diffusion Rounding
- Parameter Extraction
- Experimental Results
- Conclusions

Lithographic WYSIWYG Breakdown



- Existing compact device models (e.g., BSIM) do not handle non-rectangular geometries.
- Sources of diffusion rounding:
  - Different channel widths with tight poly pitch
  - Power/Ground diffusion straps
- Large poly-active corner spacing is required to avoid diffusion rounding → area overhead

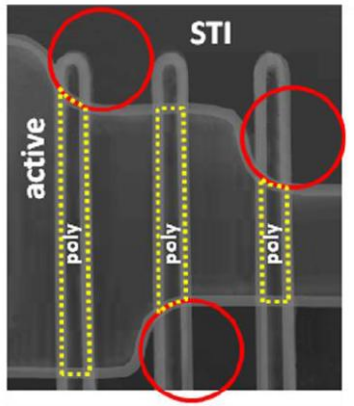


Figure from V. Moroz, M. Choi, & X.W. Lin, *SPIE* 2009.

Previous Works

- Modeled polysilicon rounding/line edge roughness only [SPIE'06, DAC'07, etc]
  - Assumed current flows in horizontal direction
  - Modeled non-rectangular gate device by slicing device's channel and connecting them in parallel
- Empirical diffusion rounding model [ASPDAC'08]
  - Fitted I_{on} and I_{off} functions based on available data
  - Did not model asymmetrical currents for drain/source side rounding

This Work

- *First* Poly + diffusion rounding model.
  - Developed ground up from fundamental physics
- Models asymmetrical currents for drain/source side rounding.
- SPICE-based calibration of the model
  - No need for silicon or TCAD simulation data.

Modeling Diffusion+Poly Rounding

Slice channel

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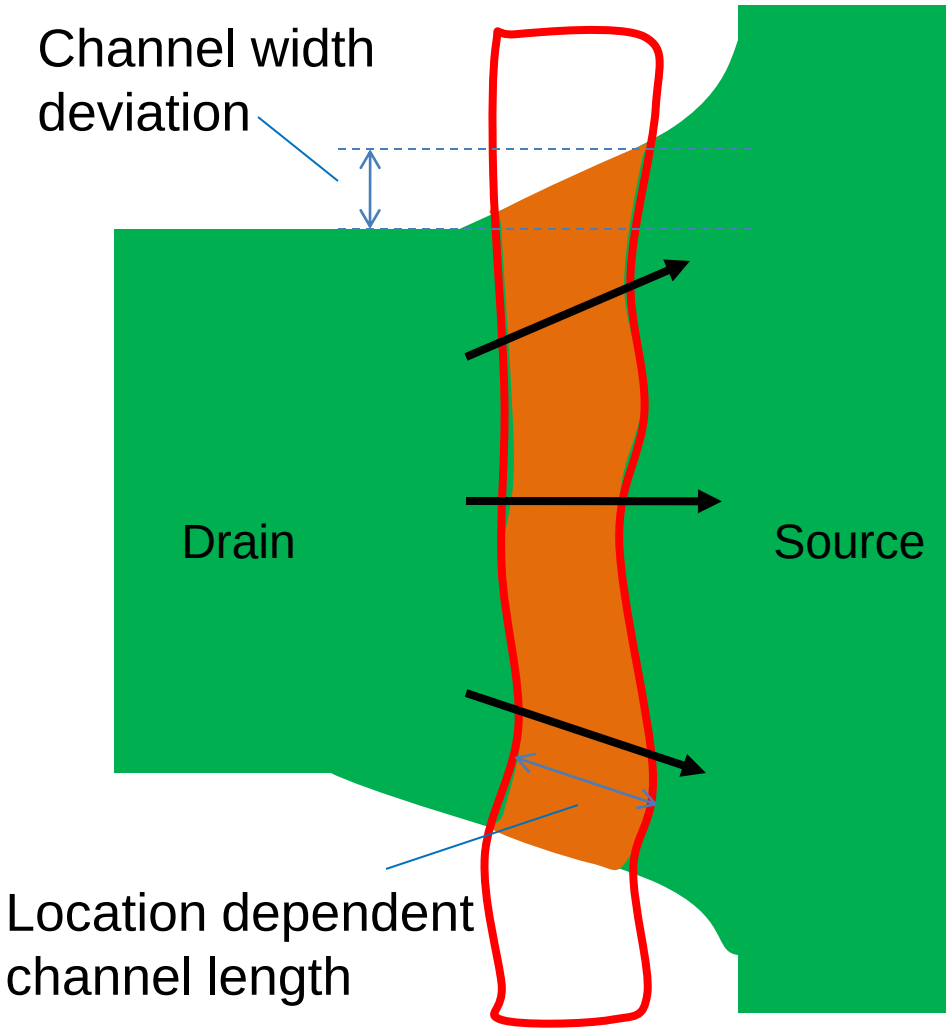
Extract parameters:
- Channel width
- Channel length
- V_{th}

↓

Obtain total current using SPICE simulation

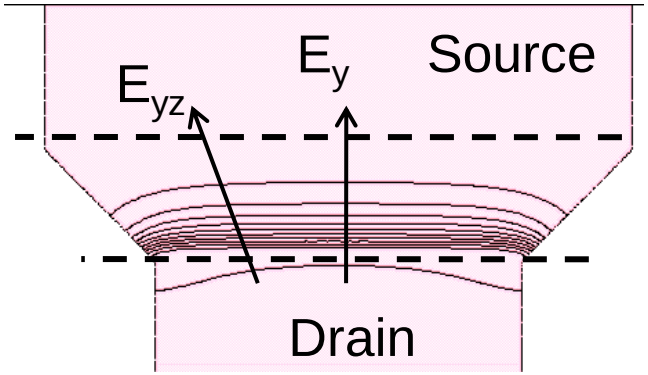
↓

Equivalent W,L,V_{th}

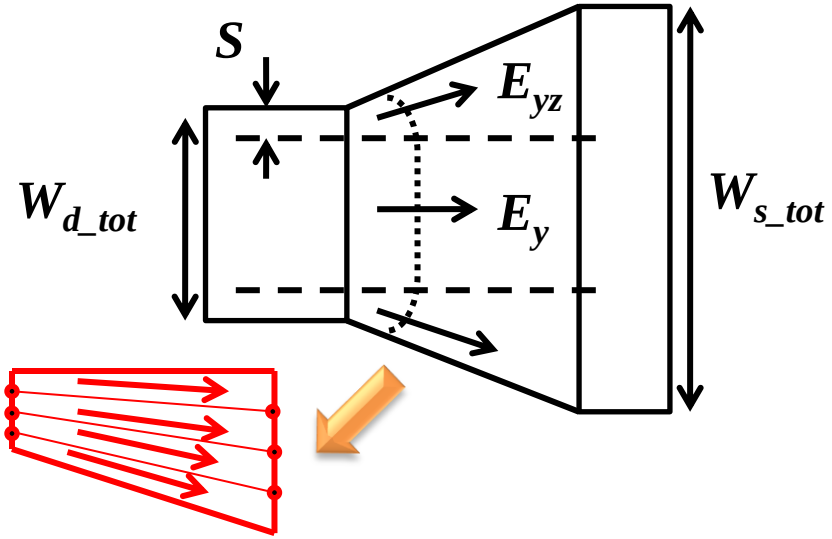


Channel Slicing

- Channel's electrostatic potential is two-dimensional
  - Changes L_{eff} and W_{eff}
- Strategy: divide channel into 3 sections.
- Assume E field is :
  - Purely horizontal in middle.
  - Changing linearly from middle to edges.



Electrostatic potential TCAD simulation



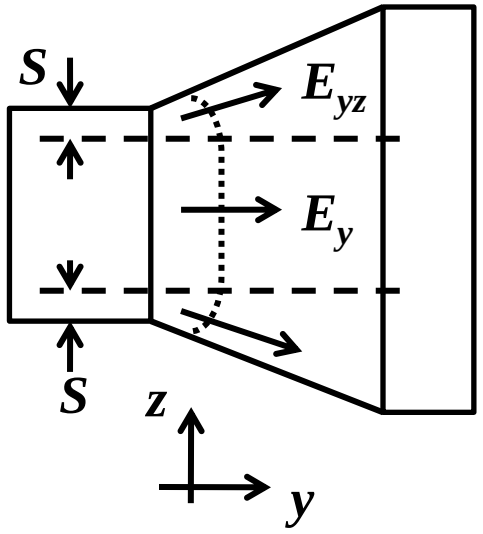
Slicing Guideline : 'S'

- a, b and $L_{eff\text{-}ref}$ are technology independent parameters extracted from TCAD data

$$S = \frac{(a + b\theta) \times L_{eff}}{L_{eff-ref}}$$

$$a = 8nm, b = 0.089nm^{\circ -1} \text{ and } L_{\text{eff}-\text{ref}} = 25nm$$

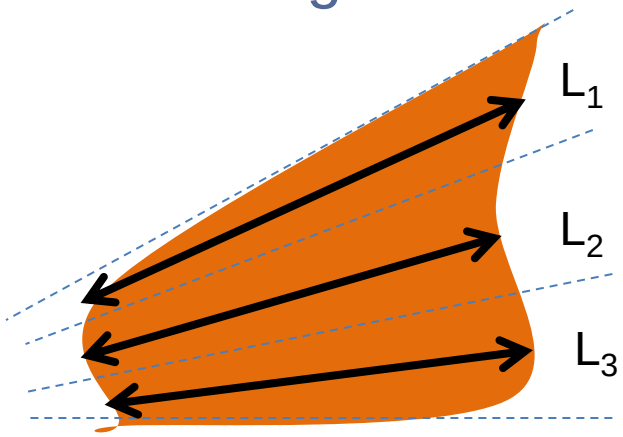
- θ and L_{eff} are geometrical parameters extracted from device's shape
- Larger θ (larger source/drain widths) leads to stronger vertical (z) E-field and a larger S

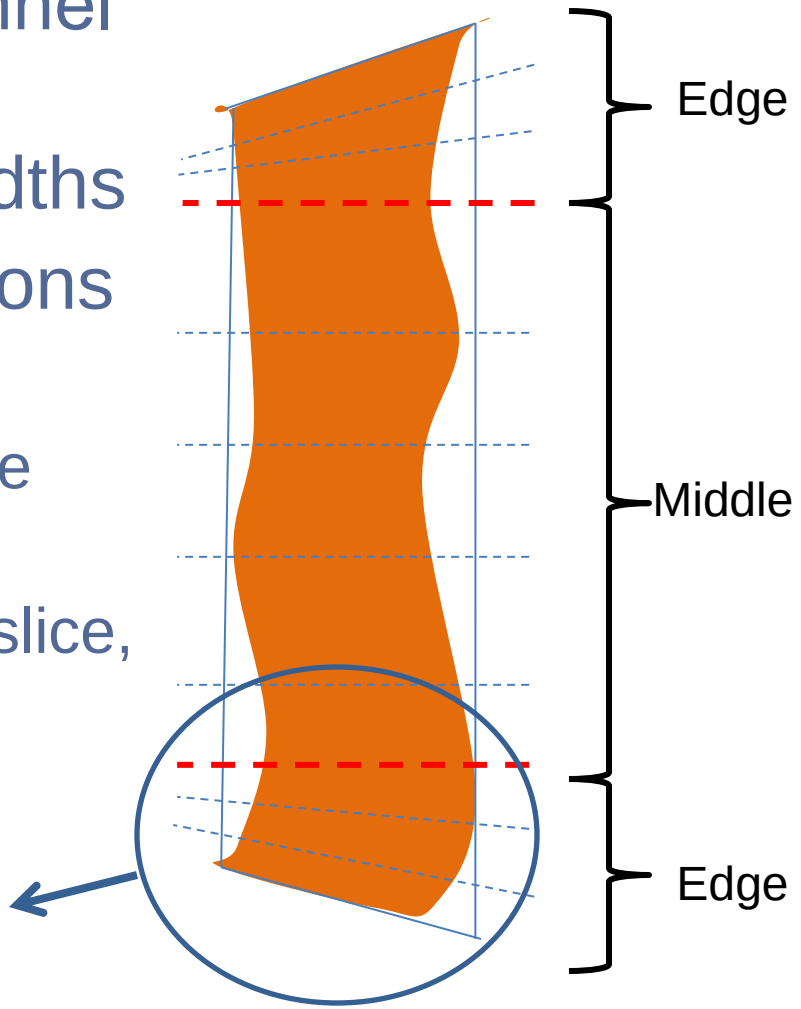


- But increased source/drain is further away from channel → vertical E-field and S weakly dependent on θ
- Horizontal(y) field changes linearly with channel length → modeled as a multiplier, $L_{eff}/L_{eff\text{-}ref}$

Effective Channel Length

- Middle section of device's channel is sliced into small transistors with equal source and drain widths
- Source and drain of edge sections are divided into slices equally
  - Assume E-field/current follows the direction of slices
  - ➢ Effective channel length of each slice, $L_{eff\text{-}i} = L_i$

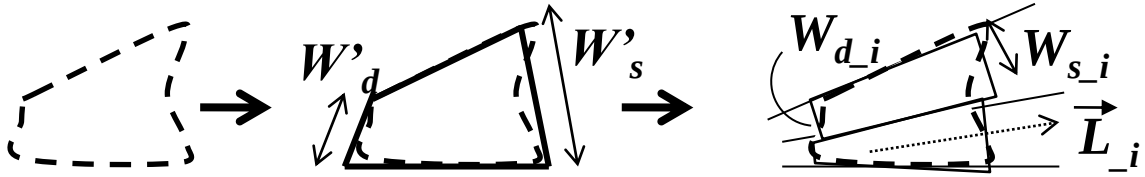




Effective Channel Width

- Effective width of sliced channel

$$W_{eff} = \frac{(W_s - W_d)}{\ln(W_s / W_d)}$$



W_{d_i} and W_{s_i} are obtained by approximating edges with straight lines orthogonal to the vector of channel length

- W_{eff} is derived based on gradual channel approximation → voltage varies gradually from drain to source

Channel width varies along channel

$$\int_0^L \frac{I_D.dy}{(W_d + (W_s - W_d)y/L)} = \int_{V_s}^{V_d} \mu Cox[V_G - V_{th} - V]dV$$

$$I_D = \frac{1}{L}\frac{(W_s - W_d)}{ln(W_s/W_d)}\mu Cox[V_G - V_{th} - \frac{V_{ds}}{2}]V_{ds}.$$

- Second order effects (DIBL, velocity saturation, etc.)
  - Considered by applying effective length, width and V_{th} in SPICE simulation with BSIM model.

ΔVth - Narrow Width Effect (NWE)

$$\Delta V_{th\text{-effective}} = \Delta V_{th-\text{Narrow width}} + \Delta V_{th-CS}$$

- Non-uniform V_{th} along channel width
  - Impact of NWE is modeled by fitting ΔV_{th} as a function of location [SPIE'06]

$$\Delta Vth(x) = \begin{cases} K_1(x-w)^2 + K_2(x-w) & 0 \le x \le w \\ 0 & w \le x \le W-w \\ K_1(W-x-w)^2 + K_2(W-x-w) & W-w \le x \le W \end{cases}$$

w is the maximum width affected by NWE

W is device's average width

K_1 = 1.65 (NMOS) 0.01 (PMOS)

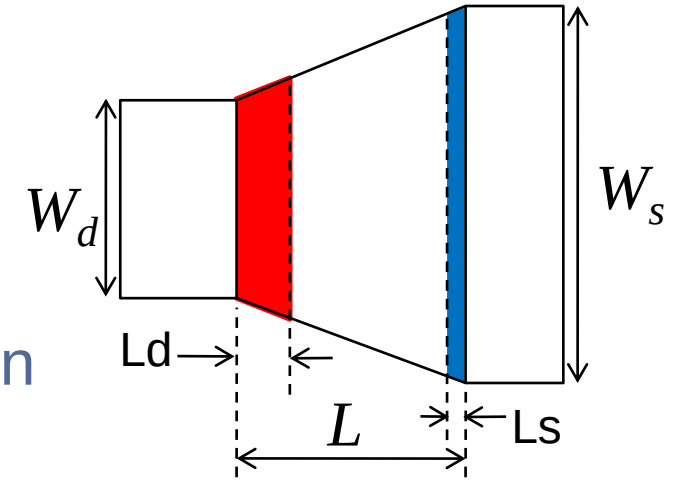
K_2 = 1.65 (NMOS) 0.01 (PMOS)

w = 5nm (NMOS) 1nm (PMOS)

Fitted based on rectangular devices data

ΔVth – Asymmetrical Source/Drain

- A portion of depletion region is shared between gate and source/drain
- Asymmetric source/drain sharing regions change effective region supported by gate alone → V_{th} variation
- Charge Sharing Model :
  - ΔV_{th} α Q_{shared},
  - Estimate Q_{shared} based on device's geometry

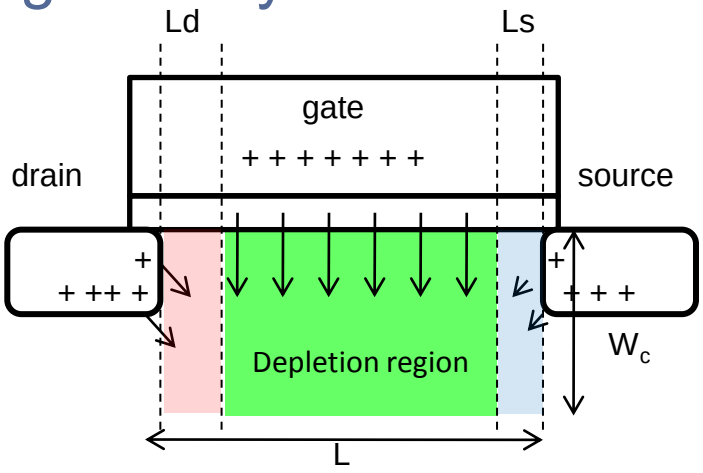


$$V_{th} = Vfb + 2\phi b + [\frac{Q_{total} - Q_{shared}}{C_{ox}WL}]$$

Asymmetrical source and drain

$$Q_{shared} = qN_a(\frac{W_c}{2})(L_dW_d + L_sW_s)$$

$$\Delta V_{th-CS} = \frac{qN_aW_c}{2LC_{ox}}\left[\frac{2(L_dW_d + L_sW_s)}{W_d + W_s} - (L_d + L_s)\right]$$



Total Currents

- Each slice can be represented by rectangular transistor with equivalent L,W and V_{th}:

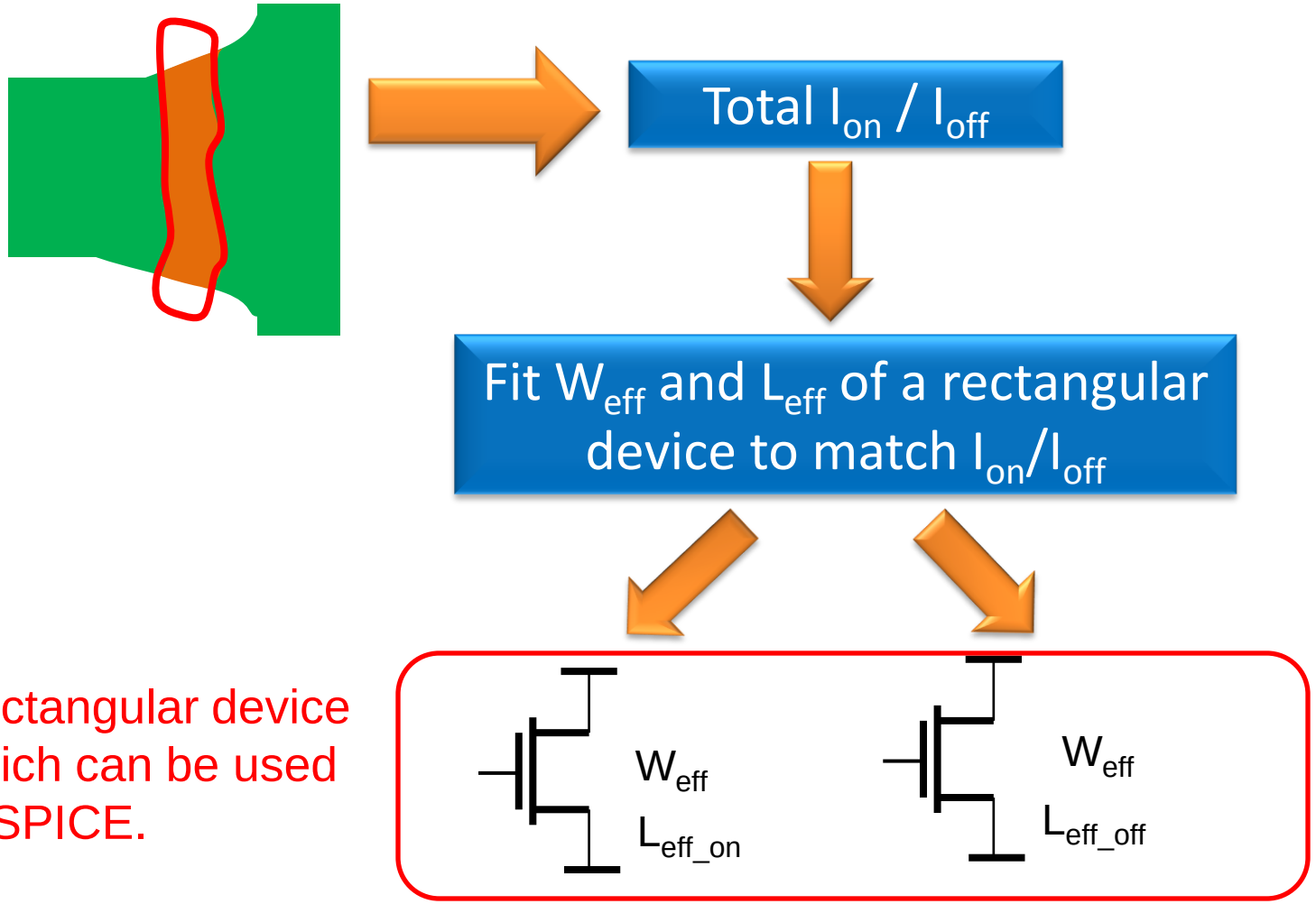
$$I_{total} = \sum_{i=1}^{n} f(L_i, W_i, Vth_i)$$

Can be obtained using conventional compact model e.g., (BSIM).

- Second order effects are implicitly considered in BSIM.
- Evaluate I_{total} at V_{gs}= 0 , V_{ds}= V_{dd} (off)

  V_{gs}= V_{dd}, V_{ds}= V_{dd} (on)

Equivalent Rectangular Transistor for Circuit Simulation



Rectangular device which can be used in SPICE.

Parameter Extraction

- Channel length and width
  - Obtained directly from shapes.
- $\Delta V_{th} = \Delta V_{th\text{-}narrow\ width} + \Delta V_{th\text{-}cs}$

$$\Delta V_{th-CS} = \frac{qN_aW_c}{2LC_{ox}}\left[\frac{2\left(L_dW_d + L_sW_s\right)}{W_d + W_s} - \left(L_d + L_s\right)\right]$$

Unknowns: charge sharing regions contributed by source and drain.

- L_d and L_s can be calibrated using
  - Silicon data or TCAD simulation results
  - SPICE (+ BSIM) simulation results

TCAD-Based Calibration

- Require I_{off} of a diffusion rounded device (forward and reverse bias)
- L_d and L_s are calibrated to minimize error between model and measured I_{off}
- I_{off} is used for calibration as it is sensitive to V_{th} variation caused by L_d and L_s

  L_d=5 nm (NMOS) 5.5 nm (PMOS)

  L_s=1 nm (NMOS) 1.0 nm (PMOS)

SPICE Based Parameter Extraction

- Extract L_d and L_s from rectangular devices.
- Perturb L and V_{ds} to obtain ΔV_{th},

Let

$$K_1 = V_{th,L1} - V_{th,L2} \quad \text{Eq. 1}$$

$$K_2 = V_{th}\big|_{V_{ds}=V_{dd}} - V_{th}\big|_{V_{ds}=0} \quad \text{Eq. 2}$$

L_d and L_s are not fully extracted but they can be substituted into ΔVth equation directly

$$\frac{qN_aW_c}{C_{ox}}(L_d) = K_1\left(\frac{L_1L_2}{L_1-L_2}\right) - \frac{K_2L_1}{2}$$

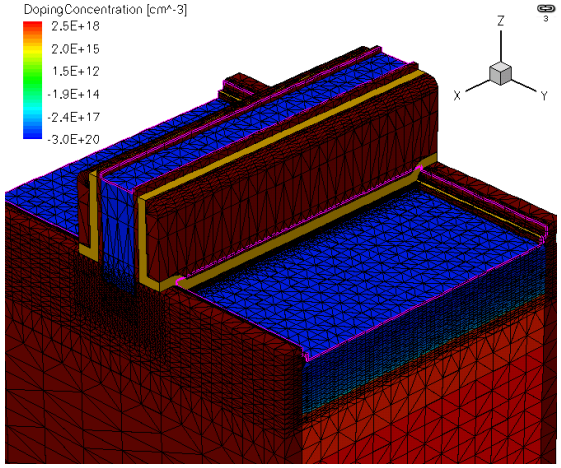
$$\frac{qN_aW_c}{C_{ox}}(L_s) = K_1\left(\frac{L_1L_2}{L_1-L_2}\right) + \frac{K_2L_1}{2}$$

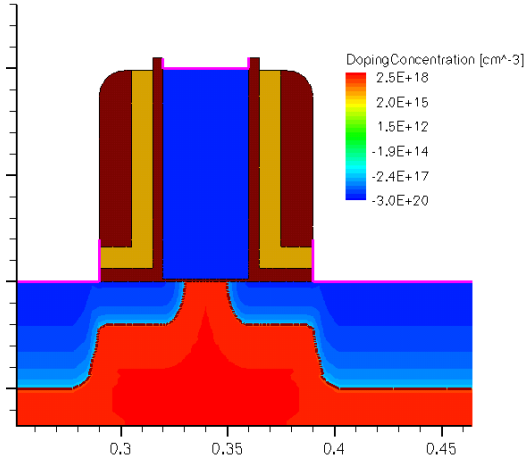
Combine Eq. 1 and Eq.2

- Extract parameters at large length and width to decouple second order effects
- Less accurate compared to TCAD based calibration as L_d and L_s are not extracted → cannot evaluate source/drain widths in charge sharing region → approximate them as source/drain widths at junctions.

Simulation Setup

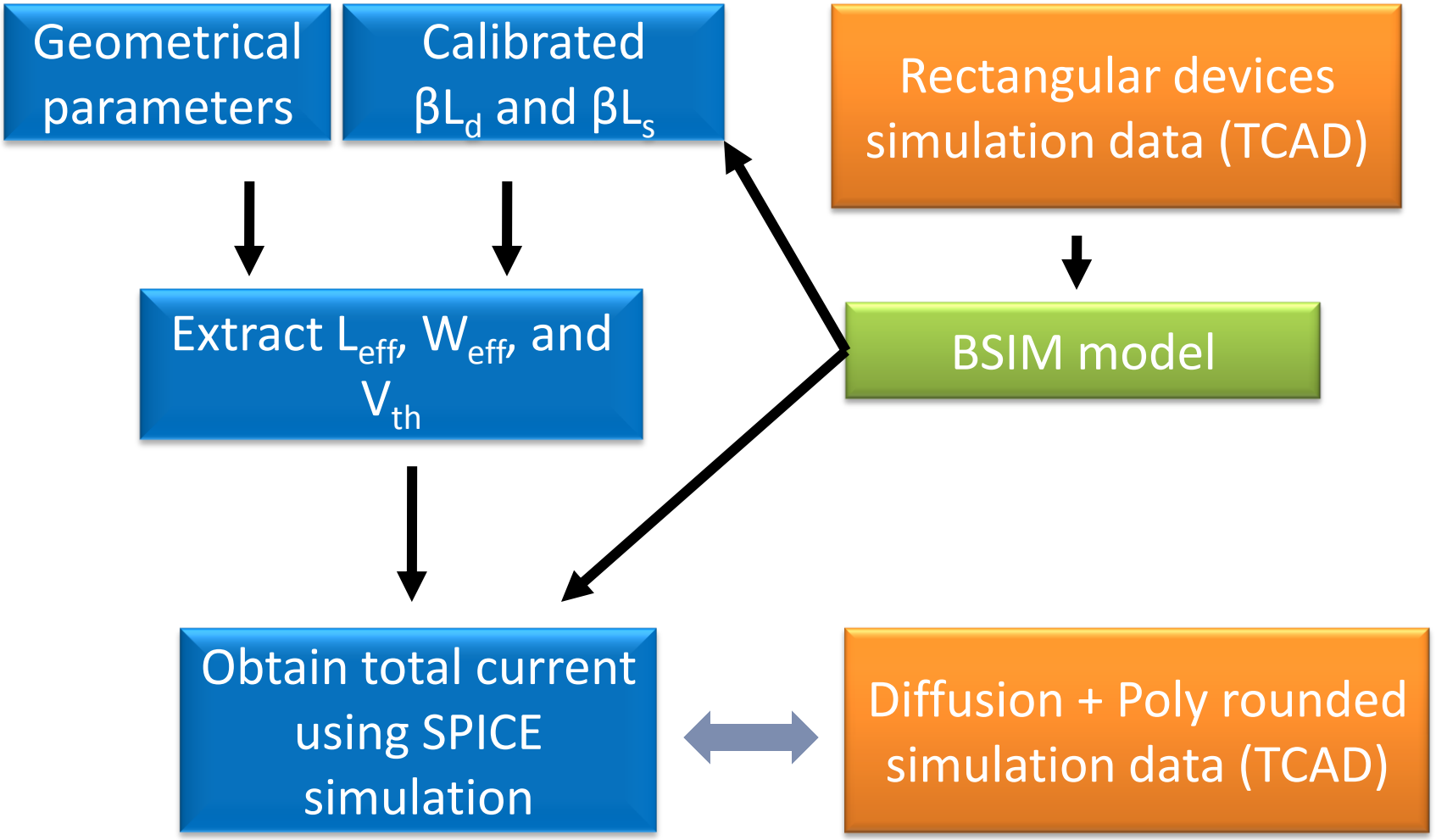
Parameters	Value
Drawn gate length	45 nm
Effective channel length	25 nm
Width (NMOS/PMOS)	110-300 / 255-500 nm
Vdd	1 V
Tox	1.5 nm
S/D doping (NMOS/PMOS)	3e20 / 2e20 cm−3
NSUB (NMOS/PMOS)	2.5e18 / 2.5e18 cm−3
Junction depth	20 nm
Line-end extension	20 nm
Spacer width	30 nm





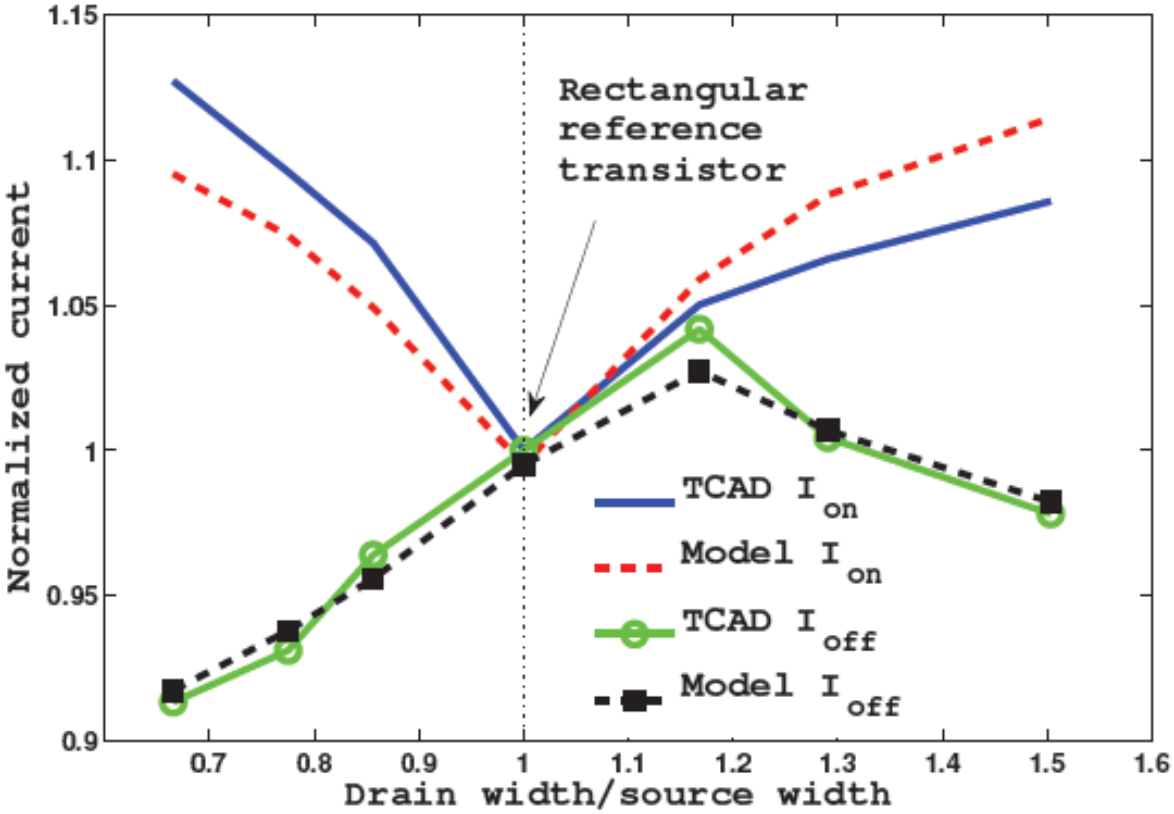
TCAD : Sentaurus 3D

Experiment Flow (SPICE calibrated)



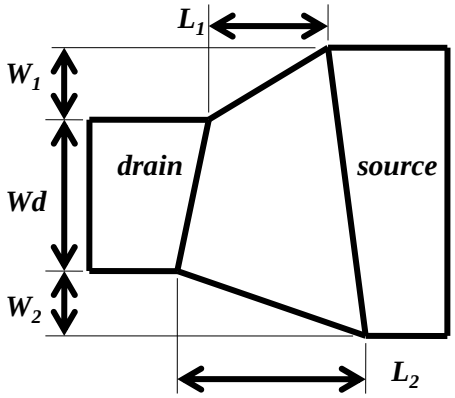
TCAD vs Model (Diffusion Rounding only)

- Asymmetrical I_{on}/I_{off} when rounding happens on Drain/Source terminals
  - ΔVth varies according to drain/source ratio.



Poly+Diffusion Rounding

	L1 (nm)	L2 (nm)	W_d (nm)	W_1 (nm)	W_2 (nm)	Error (%)			
						TCAD cal.		SPICE cal.	
						I_{on}	I_{off}	I_{on}	I_{off}
Diffusion rounding only (Source side larger)	45	45	155	26	0	-2.1	-0.8	-2.0	-0.5
	45	45	155	45	0	-2.0	0.7	-1.9	1.1
	45	45	155	78	0	-2.8	0.4	-2.7	0.7
Poly rounding only	55	45	155	0	0	NA	NA	-0.7	2.5
	35	45	155	0	0	NA	NA	-0.2	7.5
Poly+ diffusion rounding	55	45	155	45	0	NA	NA	-1.4	3.1
	55	45	155	0	45	NA	NA	-2.8	-2.7
	35	45	155	45	0	NA	NA	-2.4	0.7
	35	45	155	0	45	NA	NA	-0.7	7.8



Average error :

(Diffusion layer rounding only)

TCAD calibrated model = 1.6%

SPICE calibrated model = 1.7%

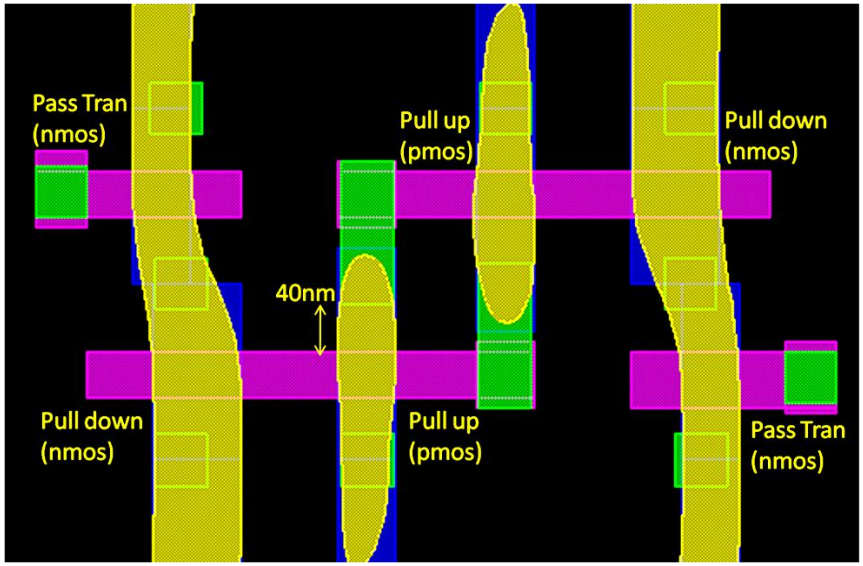
(Poly+ Diffusion layers rounding)

SPICE calibrated model =2.7%

Diffusion Rounding on SRAM

Defocus (nm)	Contact/Poly Spacing (nm)	Overlay (nm)	SNM (mV)
0	40	0	378.20
0	20	0	379.30
100	40	0	376.50
100	20	0	378.70
0	40	20	377.10

SNM for rectangular device =378.40mV

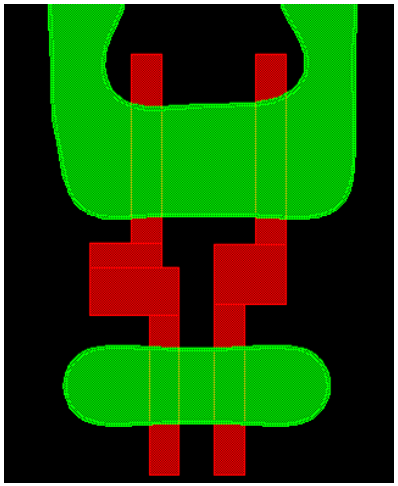


- Diffusion rounding is not significant on SRAM.
  - Second order effects are ignored (AS, PS, AD and PD)
  - Symmetrical layout suppresses SNM variation.
- Results may vary for different optical model and device.

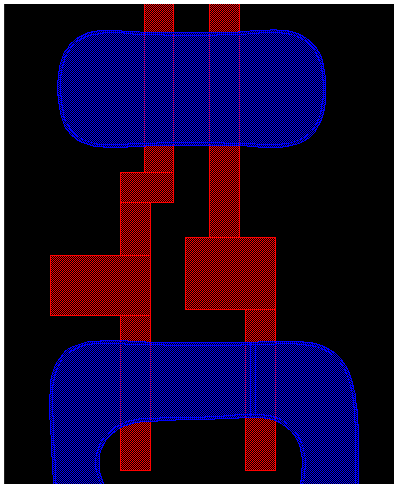
Application on Logic Cells

		NAND_X1		NOR_X1	
		Original	Spacing Reduced	Original	Spacing Reduced
Delay	nominal (no defocus)	1.00	1.00	1.00	0.99
	worst (100nm defocus)	1.05	1.04	1.05	1.05
Leakage	nominal (no defocus)	1.00	1.00	1.00	1.01
	worst (100nm defocus)	0.91	0.91	0.90	0.90
area		1.00	0.95	1.00	0.95

- At 100nm defocus
  - Δ Delay = 5%
  - Δ Leakage = 9%
- Design rule can be optimized.



NAND2_X1



NOR2_X1

Sources of inaccuracies

1. Source/drain widths of charge sharing regions vary according to L_d and L_s. Exact L_d and L_s are not decoupled in SPICE-based calibration
2. Drain side width changes when device is under saturation
3. Piece wise modeling error in channel's electric field distribution

Future work

– Captures channel width variation in saturation by estimating channel length modulation

– Extract capacitance related parameters :

- Diffusion area and perimeter (AD,PD,AS & PS in BSIM)

Conclusions

- Diffusion rounding affects channel length, width and V_{th}.
- Modeling error for poly+diffusion rounding are 2.3% (I_{on}) and 1.0% (I_{off})
- Model can be calibrated using SPICE.
- Applications:
  - Post-lithography circuit analysis.
  - Design rules exploration.