Single-Mask Double-Patterning Lithography

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Outline

- Introduction to Shift-Trim DPL (ST-DPL)
- Design Rules for ST-DPL Compatibility
- Example ST-DPL Implementation
- Results
- Pros and Cons of ST-DPL
- Conclusions

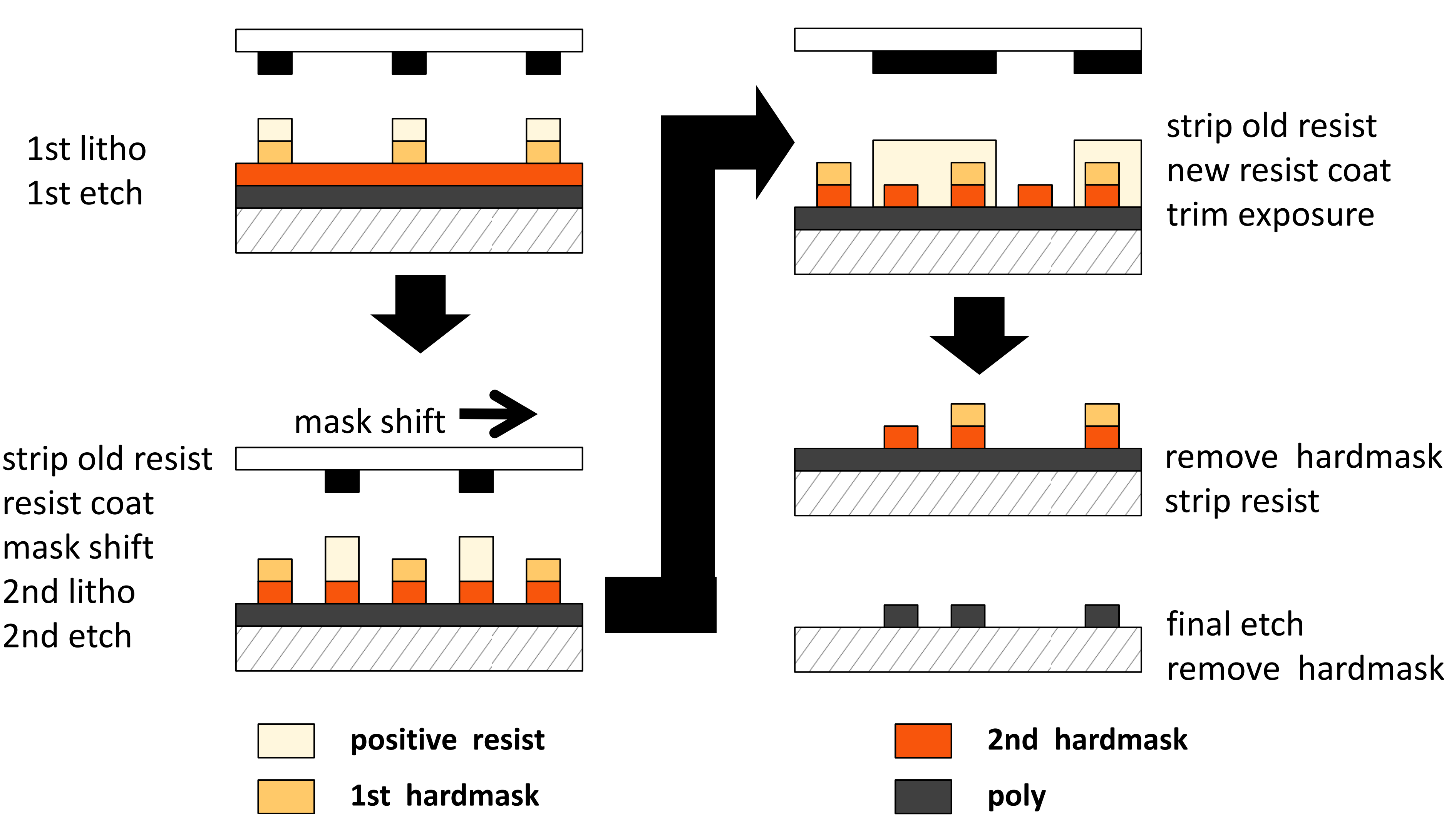
Motivation

- DPL is one of the most likely solutions for scaling beyond 32nm node
- DPL has 4 major impediments:
  - high mask-cost (two critical photomasks)
  - reduced fabrication throughput (extra processing steps)
  - tight overlay budget (overlay translates directly into line or space CD variability which has a 3x tighter budget)
  - So-called CD “bimodal” problem → tough for circuit design tools and flows to handle

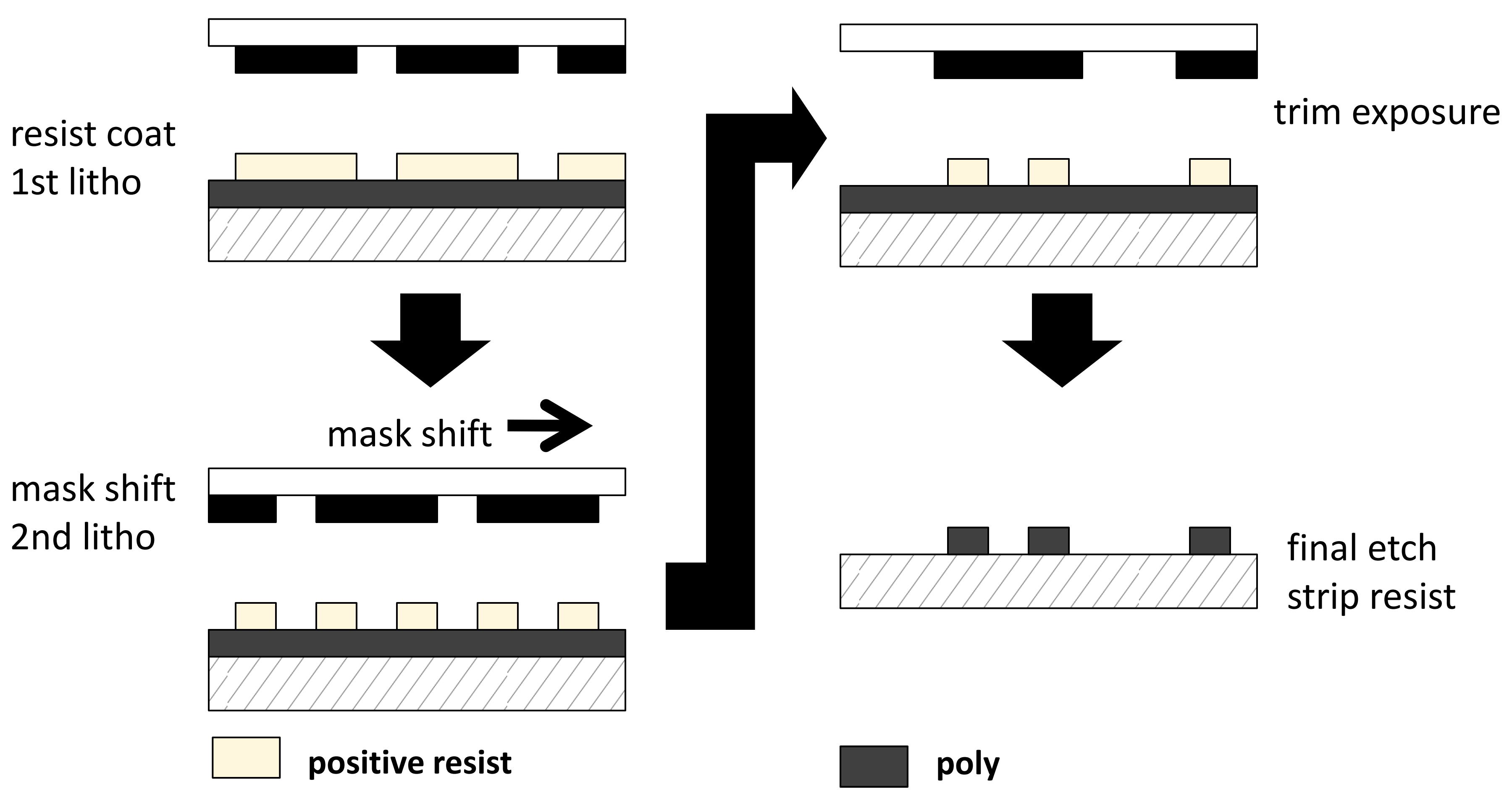
Shift-Trim DPL

- Use a single mask to achieve 2x pitch relaxation
- ST-DPL involves the following steps:
  - print the first pattern as in standard DPL processes;
  - shift the photomask of step 1 by minimum gate pitch X and print the second pattern;
  - apply a non-critical trim (a.k.a. block) exposure to remove unnecessary features

LELE Process – Positive Dual-Line



LLE Process – Negative Dual-Trench

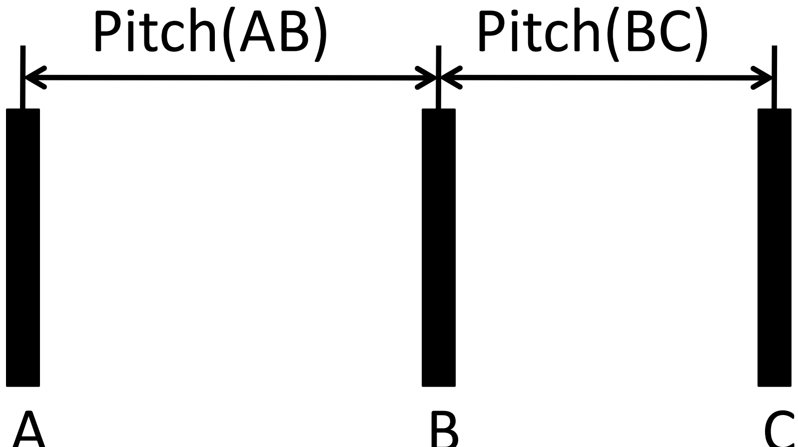


- Wafer stays in exposure tool chuck

Layout Restrictions and Challenges

- Basic layout restrictions are imposed (X is amount of mask-shift, X_0 is min gate pitch of single patterning):
  - Restricted gate-pitch: every other gate, pitch is either X or X_0 (see *)
  - Min gate spacing = contacted-gate spacing

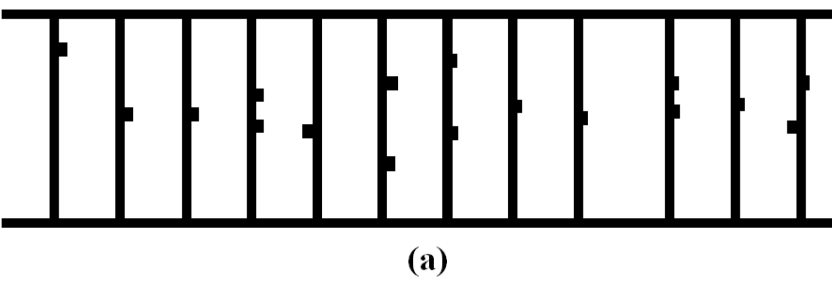
*If Pitch(AB) < X_0 but different than X_0, then Pitch(BC) is restricted to either X or X_0



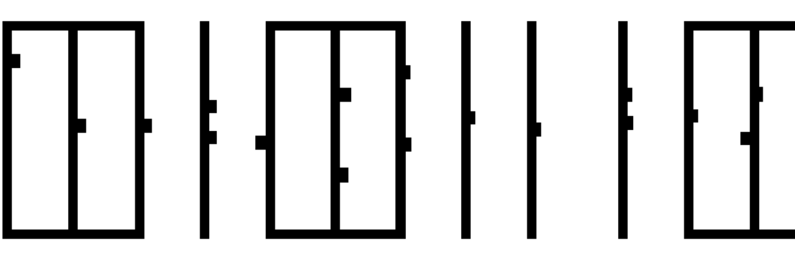
- Poly routing is restricted to cell top/bottom routing channels
- To guarantee a simple trim-mask, other DR restrictions may be necessary (e.g., line-end to field-poly spacing and line-end gap)

ST-DPL Layout-Implementation

- For fixed pitch grating → straightforward, no redesign
- 1D-poly with non-fixed pitch
  - Pitch adjustment might be necessary to enforce 1st layout restriction (met easily in real designs because majority of gates are at contacted-pitch – equal to X – from at least one of its two neighbors)
  - Mask consists of simple 1D-lines with 2x min pitch of single patterning
- 2D-poly
  - "wrong-way" poly in top/bottom routing channels
  - Option (b): "wrong-way" lines only when needed (less rounding, but less regularity)
  - Complication from contact landing pads (not an issue with trench-contacts)
- Layout decomposition is trivial

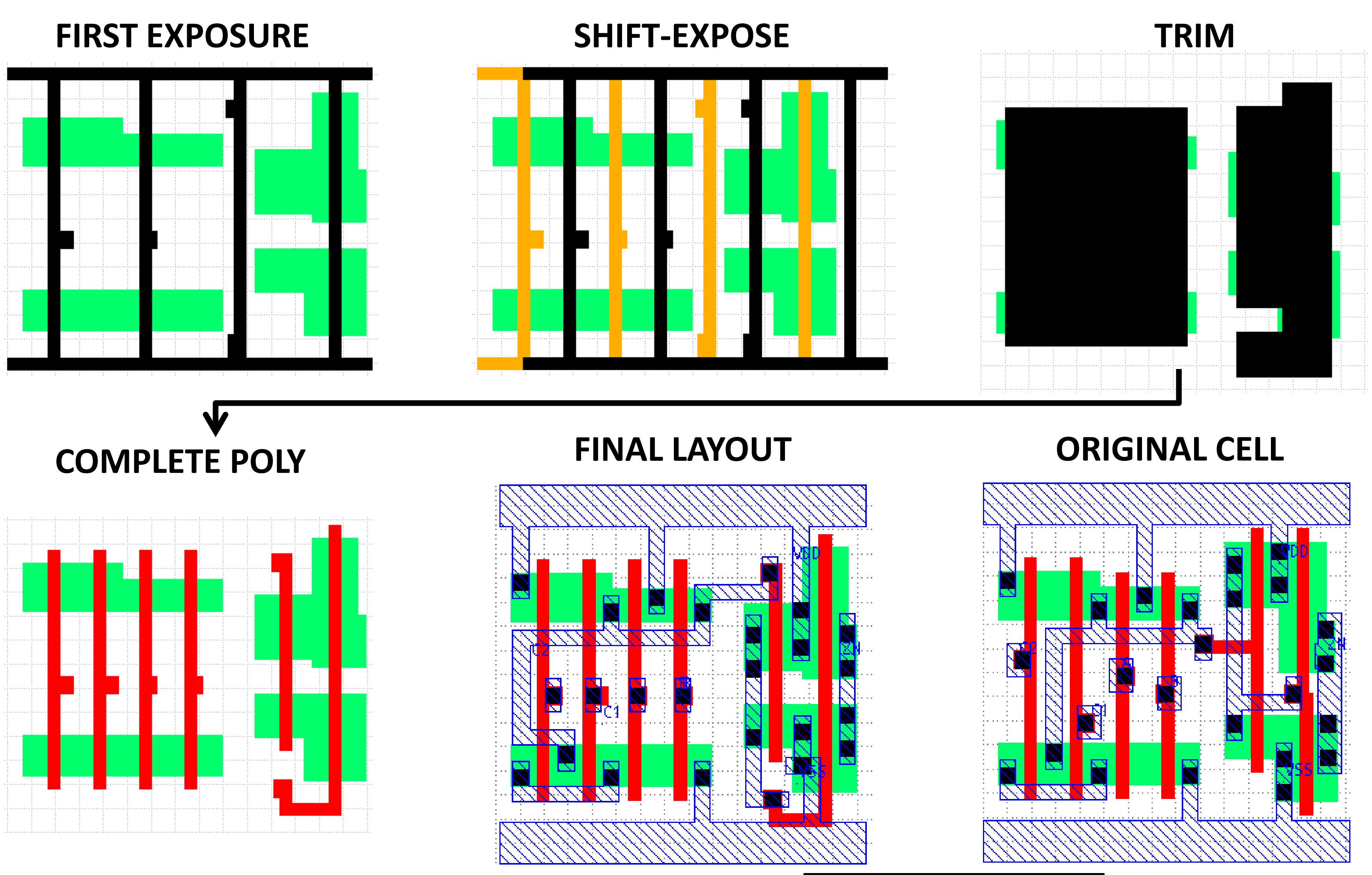


(a)



(b)

An Example – 4-Input OAI



no area overhead

ST-DPL Compatible Cell-Library

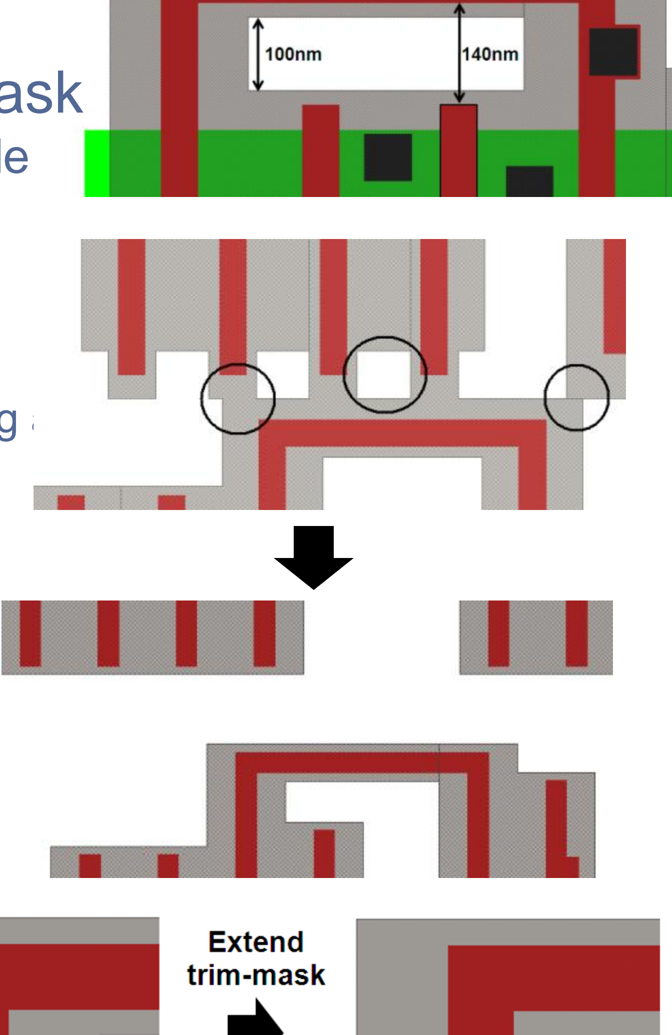
- Manual layout migration of Nangate open cell library using FreePDK 45nm process DRs
- Most cells are made compliant to ST-DPL technology with no area overhead and little or no redesign effort
- Layout migration of large cells with poly-routing requires more time and effort
  - contact landing pads printed in shifted exposure whether needed or not
  - pitch-adjustment between some lines is necessary

Critical-Mask Layout Generation

- Automated layout decomposition into first and second exposures (C++ program based on OpenAccess 2.2 API)
  - If pitch with previous line is X, the line is assigned to the shifted-exposure and previous line is assigned to 1st exposure;
  - If pitch with previous line is $< X_0$ and different than X, the line is assigned to 1st exposure, previous line is assigned to 2nd exposure;
  - If pitch with previous line is $> X_0$, line can be assigned to either of the two exposures

Trim-Mask Layout Generation

- DR restrictions to guarantee simple trim-mask
  - to ensure min hole dimension: poly line tip-to-side and tip-to-tip within-cell spacing rules are increased (from 75nm to 140nm)
  - To get rid of holes at cell-boundaries
    - top/bottom “wrong-way” poly lines used for routing pushed 35nm toward the center of cell
  - Restrictions specific to FreePDK 45nm
    - might not be needed for other processes and for cells designed from scratch
- Final simplification step by notch-filling
- Simple, composable trim mask generation for entire design:
  - for each cell-instance, copy features from corresponding cell in the library to the instance location in the design



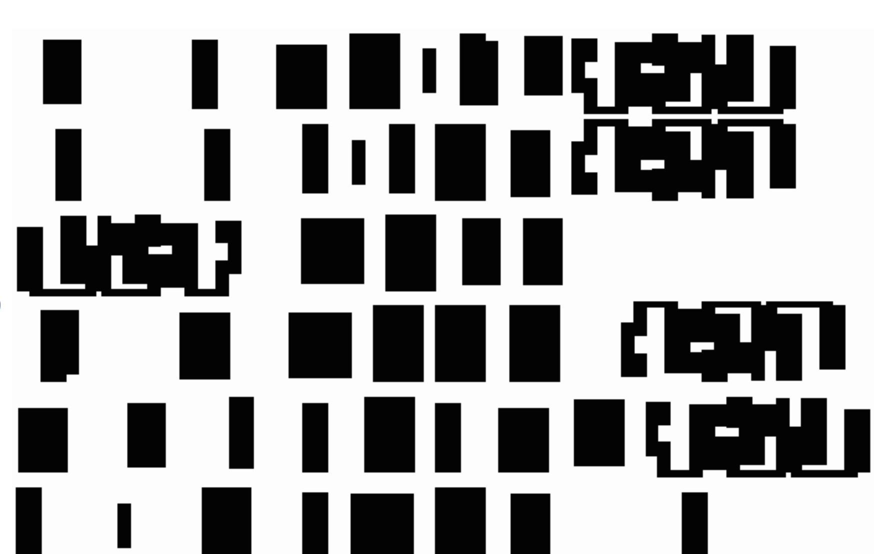
Results – Area

- Developed ST-DPL 45nm cell library (42 cells) with no area overhead except for 3 cells (INV_X4/8/16)
  - overhead caused by layout restrictions imposed to simplify trim-mask (could be avoided for reasons discussed earlier or if option (b) of base mask-structure is used)
- Synthesized 3 designs with ST-DPL library then placed/routed
- Cell-area overhead for all designs is negligible (< 0.34%)

	Description	Cell instances	Cell-types	Flip-flops	INV/BUF	Cell-area $[um^2]$	Area overhead
mips789	processor core	10529	35	2011	1465	22867.5	0.02%
or1200	combinational logic	3070	35	0	890	3014.8	0.34%
usb	com. controller	478	31	93	52	880.2	0%

Results – Trim-Mask

- Simple blocks with few vertices correspond to cells with 1D-poly and more complex shapes correspond to flip-flops with 2D-poly
  - Trim for purely 1D-poly designs have extremely simple features



	Line-width [nm]	Notch Size [nm]	Hole dimensions [nm]	Overlay margin [nm]	Trim-mask fractures	Post-OPC poly fractures
mips789	$\geq$ 90	$\geq$ 70	$\geq$ 190 x 145	20	78597	367633
or1200	$\geq$ 90	$\geq$ 70	$\geq$ 380 x 100	20	5189	43150
usb	$\geq$ 90	$\geq$ 70	$\geq$ 190 x 145	20	2770	14404

- minimum dimensions are fairly large compared to min feature size
  - Listed dimensions not to be compared directly to dimensions of critical-mask because trim-mask features do not define patterns but rather protect existing patterns by larger coverage
- # of fractures is 5x to 8x smaller than that of post-OPC poly-layer

Cost, Overlay and Throughput Benefits

- Critical mask reuse → mask-cost cut to nearly half that of DPL
- For negative LLE process (wafer can remain in tool-chuck between exposures), overlay error of the two patterns is virtually (also, saves alignment time)
- Reticle/mask related overlay components that are eliminated for all processes:

Source	Benefit
All sources	almost eliminated in case of -ve LLE
Reticle/mask related	eliminated for all ST-DPL processes
Reticle alignment	reduced for all ST-DPL processes
Wafer stage	not affected

  - Reticle alignment error is reduced due identical layouts
  - Image placement error completely correlated → does not matter
- Time spent on mask loading/unloading and reticle alignment is saved

Alleviating CD Bimodality Problem

- Two independent exposures in DPL → Bimodal CD distributions → can have severe implications for design flows
- Same mask is used for both exposures in ST-DPL → mask CDU (important contributor to the overall CD variation) no longer affects bimodality
- Distribution of CD difference has

$$\mu_{diff} = \mu_a - \mu_b$$

$$\sigma_{diff} = \sqrt{\sigma_a^2 + \sigma_b^2 - 2\sigma_m^2}$$, where σ_m std deviation of mask CDU

  – Using line-CDU breakdown values for LELE positive 32nm, σ_{diff} reduced from 1.49nm to 1.34nm (10.3% reduction)

Comparison with Popular Patterning Techniques

	Subtractive-litho [18]	Standard-DPL	ST-DPL
Mask-cost	best	worst	intermediate
Trim	yes	no	yes
Pitch doubling	no	yes	yes
Area overhead	worst	best	best
Designing effort	worst	none	intermediate
Layout decomposition	none	tough	trivial
Variability	best	worst	intermediate
CD bimodality	no	yes	reduced
Same-layer Overlay	no	yes	reduced
Throughput	best	worst	intermediate

- OPC for the two exposures has to be identical in ST-DPL
  - other correction methods are needed (e.g. dose mapping) to resolve any differences

Conclusion and Future Work

- ST-DPL is a viable and promising technique to achieve 2x pitch relaxation
- It allays major DPL impediments including cost, overlay control, bimodality, and throughput
  - ST-DPL correct layouts are compatible with spacer-litho as well
- Challenges:
  - layout redesign effort
  - Different OPC for the two exposures forbidden
  - Overhead of trim exposure and its associated processing steps
- Future work includes:
  - implementation of ST-DPL for metal layers, contacts, and vias
  - ST-DPL aware layout solutions

Thanks!

- Questions ? : Feel free to email puneet@ee.ucla.edu

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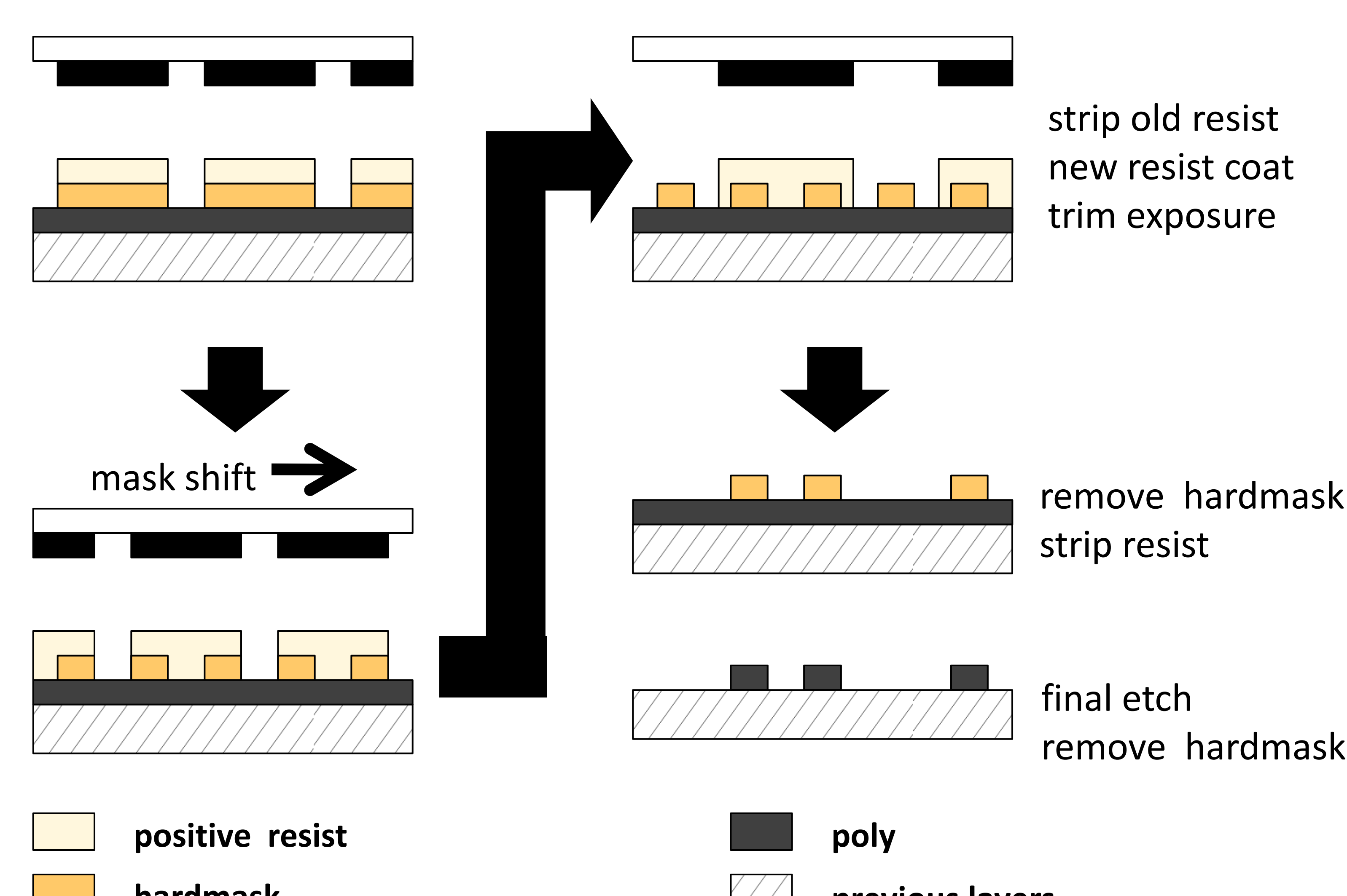

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