UCLA

Design-Overlay Interactions in Metal Double Patterning

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Electrical Evaluation – Testing Setup

- Overlay model:

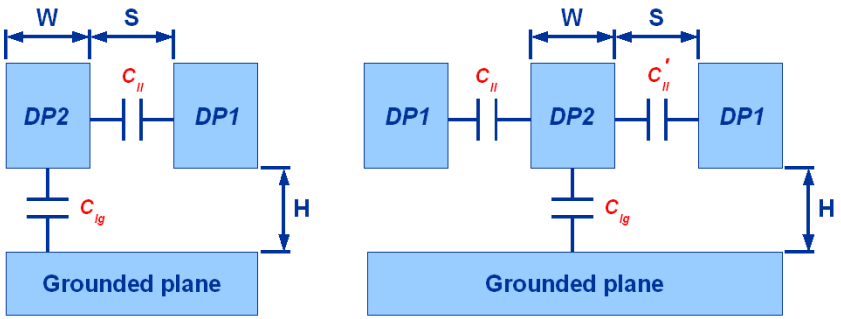
$$\delta_x = T_x + M_{wx} \times X - R_{wx} \times Y + M_{fx} \times x - R_{fx} \times y + Res_x$$

$$\delta_y = T_y + M_{wy} \times Y + R_{wy} \times X + M_{fy} \times y + R_{fy} \times x + Res_y$$

- 6.4nm total 3σ overlay (20% of 32nm tech node):
  - 50% un-modeled terms lumped into *Res.*
  - 50% imperfect correction of linear correctables.
- Evaluation of change in coupling capacitance (ΔC) and RC product (ΔRC) when overlay is applied to test structures at different locations in the design.
- Wafer of 63 33x26mm fields each containing 4 copies of the same design.
- ΔC and ΔRC are averaged out for all design copies of the fields across the entire wafer.
- ½ pitch = 32nm, aspect ratio = 1.9 (*source ITRS*).

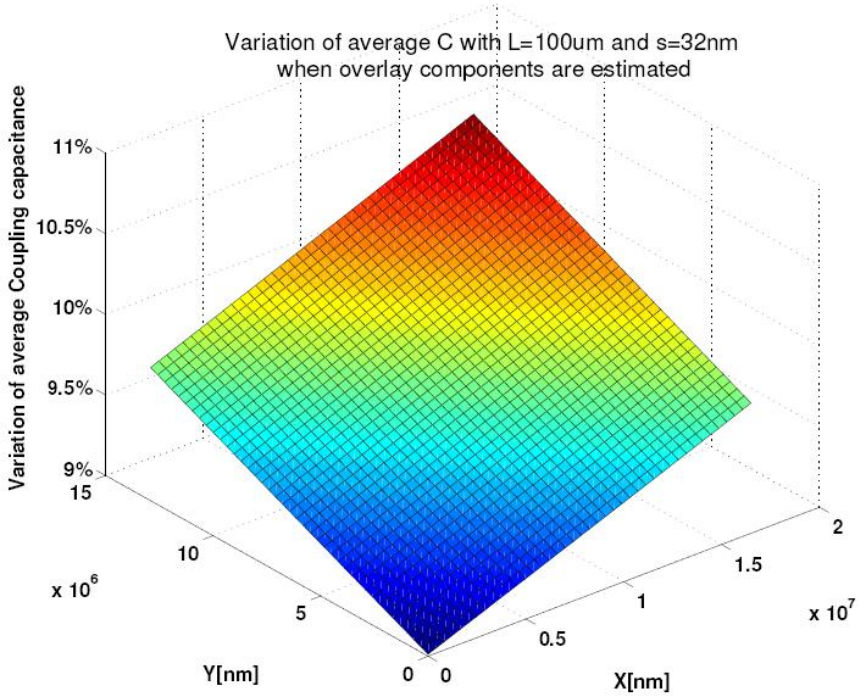
Test Structures

- 2 and 3 line structures with single grounded plane on layer below
- DP1 fixed, DP2 overlaid
- 2-line struct: $C = C_{ll} + C_{lg}$
- 3-line struct: $C = C_{ll} + C'_{ll} + C_{lg}$



Experimental Results – Positive-Tone DPL

- Positive tone litho → wire cap (*C*) affected.
- 11.5-13.6% ΔC_{ll} and 9-10.6% ΔC_{avg} according to location of structure in (x,y) design coordinates (avg over wafer).
- 21.2% ΔC_{ll} and 16.6% ΔC_{avg} at worst case location in wafer.



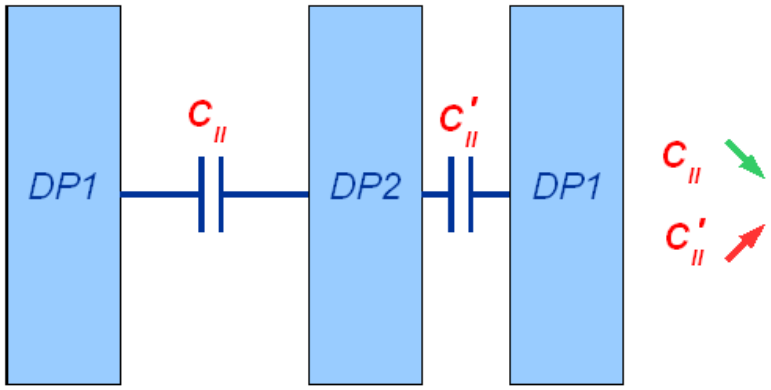
Experimental Results – Positive-Tone DPL

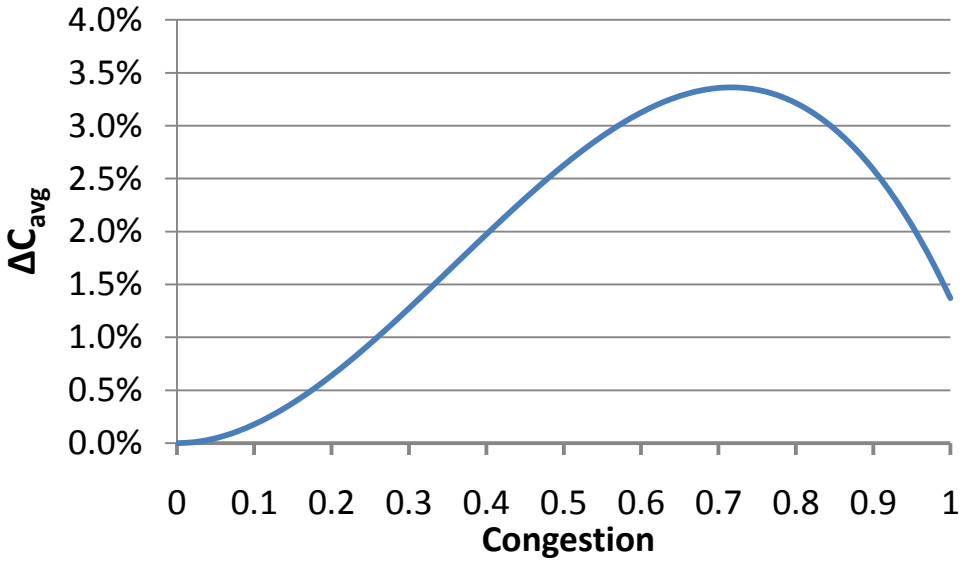
- *T*, *M*, and *R* contributions:
  - Only *T* considered → 19.6% ΔC independent of location in design.
  - Only *M* considered → 6.2-11.6% ΔC.
  - Only *R* considered → 6.75-11% ΔC.
- Insignificant difference in these impacts for worst case ΔC.
- Cancellation effect of *M* and *R* → less ΔC :
  - Their directions can be opposite in some wafer/field locations.
  - Each has opposite direction on the two sides of the field.

	2-line structure				3-line structure			
	Avg variation		Worst variation		Avg variation		Worst variation	
	ΔCu	ΔC	ΔCu	ΔC	ΔCu	ΔC	ΔCu	ΔC
Estimated components	11.5-13.6%	9-10.6%	21.2%	16.6%	1.5-1.6%	1.4%	3.2%	2.8%
Translation extreme	25%	19.6%	25%	19.6%	4.2%	3.7%	4.2%	3.7%
Mag extreme	7.9-14.8%	6.2-11.6%	24.9%	19.5%	1.5-2%	1.3-1.7%	4.1%	3.6%
Rotation extreme	8.6-14%	6.75-11%	23%	18%	1.4-1.8%	1.2-1.6%	3.6%	3.2%
Wafer extreme	15-15.9%	11.8-12.4%	21.8%	17.1%	1.8-1.9%	1.6-1.7%	3.3%	2.9%
Field extreme	11.6-19.6%	9.1-15.3%	23.9%	18.7%	1.4-2.4%	1.2-2.1%	3.9%	3.4%

Congestion Helps

- In positive-tone DPL, ΔC is alleviated due to cancellation effect between C_{II} and C'_{II}.
- When congestion is considered, ΔC_{avg} significantly reduced to at most 3.4% (for 72% congestion), compared to around 10% for 2-line structures.





Length Does Not Matter, Spacing Does

- Negligible effect of wire length (*L*) on *C* variation for L<1000μm (typical M1/M2 wires).
- 20% reduction of wire spacing (*s*):
  - ➢ *ΔC* increases by 35-38%.

Average over wafer

	S = 25.6nm	S = 32nm	S = 38.4nm
L = 10 μm	13.28%	9.82%	7.67%
L = 100 μm	13.28%	9.82%	7.67%
L = 1000 μm	13.28%	9.82%	7.67%

Worst case in wafer

	S = 25.6nm	S = 32nm	S = 38.4nm
L = 10 μm	22.91%	16.60%	12.81%
L = 100 μm	22.90%	16.60%	12.81%
L = 1000 μm	22.86%	16.57%	12.78%

Experimental Results – Negative-Tone DPL

- Major effect on interconnect resistance (*R*).
- Minor effects on coupling capacitance (*C*).
- ΔRC virtually independent of location
- Worst case very close to average variation

	Avg variation		Worst variation	
	ΔRCu	ΔRC	ΔRCu	ΔRC
Estimated components	12.5-12.7%	9.8-10%	13.9%	10.9%
Translation extreme	25%	19.6%	25%	19.6%
Mag extreme	11.2-11.9%	8.8-9.3%	13.6%	10.7%
Rotation extreme	11.1-11.7%	8.7-9.2%	13.1%	10.3%
Wafer extreme	15.4-15.6%	12.1-12.2%	16.5%	12.9%
Field extreme	15.1-16.2%	11.8-12.7%	16.9%	13.3%

Estimating Overlay Requirements

- Overlay requirement is likely to be determined based on worst case variation affecting timing and crosstalk noise.
- E.g.: 10% $\Delta CD \rightarrow$ 3.7nm 3σ overlay

  10% $\Delta C \rightarrow$ 4.2nm 3σ overlay (positive tone DPL)

  10% $\Delta RC \rightarrow$ 6nm 3σ overlay (negative tone DPL)