An Analysis of Power and Performance Improvements from Low-Temperature Operation of Processors using PROCEED-LT

Zhichao Chen
ECE Department
University of California, Los Angeles
Los Angeles, CA, United States
Email: zhichaochen@ucla.edu

Ali H. Hassan
ECE Department
University of California, Los Angeles
Los Angeles, CA, United States
Email: aehassan@ucla.edu

Sudhakar Pamarti
ECE Department
University of California, Los Angeles
Los Angeles, CA, United States
Email: spamarti@ucla.edu

Chih-Kong Ken Yang
ECE Department
University of California, Los Angeles
Los Angeles, CA, United States
Email: yangck@ucla.edu

Puneet Gupta
ECE Department
University of California, Los Angeles
Los Angeles, CA, United States
Email: puneetg@ucla.edu

***Abstract*— Low-temperature (LT) conditions can potentially lead to lower power consumption and enhanced performance in circuit operations by reducing the transistor leakage current, increasing carrier mobility, reducing wearout, and reducing interconnect resistance. We develop PROCEED-LT, a pathfinding framework to co-optimize devices and circuits over a wide performance range. Our results demonstrate that circuit operations at low temperature (LT, -196°C) reduce power compared to room temperature (RT, 85°C) by 15X to over 23.8X depending on performance level. Alternatively, LT improves performance by 2.4X (high-power, high performance) - 7.0X (low-power, low-performance) at the same power point. These gains are further improved in low-activity circuits as well as when using multi-voltage configurations. Meanwhile, we highlight the need for improvement in V_{th} variation to leverage benefits at cryogenic temperatures.**

Keywords—Cryogenic computing, circuit optimization, FinFET, Pareto optimization, process variations, transistor aging, 77K.

I. Introduction

The rapid growth of AI and Deep Learning is driving an unprecedented computing demand, while performance gains from technology scaling have stagnated. Challenges such as increased leakage currents limiting threshold voltage (V_{th}) reduction and dynamic power constraining supply voltage (V_{dd}) scaling hinder performance improvements. Additionally, raising clock frequencies further exacerbates power consumption [1]. Innovative approaches are required to address these limitations and meet the escalating demands.

Low-temperature (LT) computing, operating systems at liquid nitrogen temperatures (e.g., 77K), offers promising performance and power efficiency improvements. LT conditions enhance transistor subthreshold slopes, reduce leakage currents, and enable lower V_{th} and V_{dd}, maintaining performance with reduced power consumption [2]. For interconnects, LT reduces resistivity, allowing thinner wires with lower capacitance. However, challenges such as bandgap widening at LT increase V_{th}, potentially limiting frequency scaling [12].

Circuit-level advancements leverage LT benefits through optimized microarchitectural designs, innovative non-SRAM technologies (e.g., STT-MRAM [5], GC-eDRAM [6], 1T Floating Body RAM [7]), and novel interconnect materials [8]. Despite these advances, manual Design Technology Co-Optimization (DTCO) processes for V_{dd} and V_{th} tuning are time-intensive and limited in scope. These processes involve adjusting V_{th} to balance leakage current and performance, followed by determining the minimal V_{dd} for power-delay tradeoffs, but they are impractical for comprehensive analysis due to significant manual effort.

PROCEED addresses these challenges by automating V_{dd}, V_{th}, and transistor sizing optimization, delivering configurations in under a minute and generating Pareto-optimal solutions. However, the existing framework is limited to certain technologies and configurations [14]. This study introduces PROCEED-LT, an enhanced tool supporting FinFET-based designs and LT conditions, incorporating device wear-out, IR drop, and reliability factors. Key contributions include:

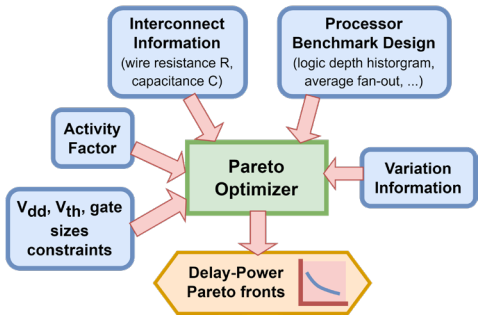


Fig. 1. The PROCEED framework.ssss

- Incorporation of advanced interconnect and device wear-out models, enabling automated multi-voltage configurations.
- Power-delay optimization under LT conditions considering aging effects and IR drop.
- Exploration of LT power improvements (7.97X~21.88X) across benchmarks, with peak performances >2X compared to RT.
- Identification of the challenge of the higher V_{th} variation sensitivity at LT due to the process variation and the scaled-down operating voltages.

Using PROCEED-LT, we evaluate LT benefits in a microprocessor (ARM Cortex M3) and neural network accelerator (ACOUSTIC [12]), demonstrating significant power-delay tradeoffs. Energy efficiency at LT must offset cooling costs, requiring a 10.65X power reduction compared to RT [3].

II. Desirable Traits of LT Circuit Operations

A. Potential of Leakage Current Reduction

LT computing, which is known as cryogenic computing as well, aims to operate computers at exceedingly low temperatures. Thanks to the temperature decreasing, the leakage current shrinks exponentially, which significantly reduces the static power and enables continuous reduction of both V_{dd} and V_{th} with no performance loss [15].

B. Potential of Improved Interconnect

Global interconnects that communicate signals across the chip are difficult to scale in length, and their latencies are mostly maintained [20]. Fortunately, the resistivity of some metal materials (e.g. copper) can linearly decrease with temperature. As a result, the latency of the interconnect is substantially reduced, thereby allowing for a safe increase in clock frequencies under LT conditions. Additionally, as the resistance in the interconnect lowers, the IR drop shows promising improvement.

C. Potential of Circuit Wear-out Slowdown

Device aging, caused by bias temperature instability (BTI) and hot carrier injection (HCI), leads to irreversible V_{th} shifts and mobility degradation over time [16]. These effects exhibit an exponential dependence on channel temperature T_c, as described in Eq. 1 and 2, with parameters derived from characterization [22].

$$\Delta V_{th}(BTI) \propto V_{gs}^{m_1} \cdot e^{-\frac{E_a}{kT_c}} \cdot t^{n_1} \qquad (1)$$

$$\Delta V_{th}(HCI) \propto V_{gs}^{m_2} \cdot e^{-\frac{E_a}{kT_c}} \cdot t^{n_2} \qquad (2)$$

Lowering operating temperatures significantly impacts aging. Research shows that at low temperatures (LT), BTI-induced ΔV_{th} is mitigated in both planar and FinFET devices under the same voltage stress [23]. However, HCI degradation may worsen at cryogenic temperatures, particularly for NFETs [24]. Reducing V_{dd} at LT offsets some HCI effects, lowering V_{ds} and power consumption. LT computing reduces leakage currents, static power, and thermal stress, enabling lower V_{dd} while maintaining performance. This decreases voltage stress and slows wear-out, reducing V_{th} shifts.

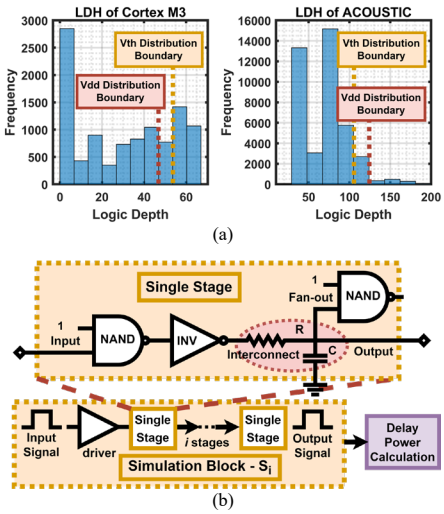


Fig. 2. (a) Logic path depth histogram and the example of V_{dd}, V_{th} distribution. (b) Circuit schematic of the single stage used for simulation and optimization.

III. Optimizing Circuits for LT Operations with PROCEED-LT

A. PROCEED Framework

Fig. 1 presents an overview of the PROCEED framework. The input of PROCEED is the interconnect information, the processor benchmark design, the operating activity factor, the variation information, and constraints. The output is a Pareto curve of power-delay (PD), where each point represents a specific V_{dd} and V_{th} configuration. Rather than relying on time-consuming RTL simulations, PROCEED estimates power-delay tradeoffs using essential design metrics. LDH is extracted from the synthesized processor benchmark to predict path delays, dividing the logic paths into n bins based on depth. Each bin corresponds to paths of similar delay stages, modeled by simulation blocks (e.g., S_i) with i gate stages, interconnect loads, and logic gates of specific sizes. Increasing the number of bins improves accuracy but raises computation time. Fig. 2(a) illustrates the LDH for Cortex M3 and ACOUSTIC, where the deepest path in Cortex M3 (67 stages) is divided into $n = 10$ bins. Fig. 2(b) shows that the delay of bin i is approximated by simulating i repeated single-stage circuits, including gate and interconnect models.

However, PROCEED requires users to manually define multi- V_{dd} and multi- V_{th} distributions before Pareto point searching. Users must decide which bins to assign to $V_{dd1}(V_{th1})$ or $V_{dd2}(V_{th2})$ to maximize the improvement of the performance.

B. Improvements of PROCEED-LT

PROCEED-LT is a calibrated framework for circuit optimization at 77K, building on PROCEED with added support for FinFETs, an accurate interconnect model, and a device wear-out model. It uses SPICE parameters from a commercial 14nm FinFET LVT cell library and features core algorithms written in MATLAB. Upgrades in detail are described below.

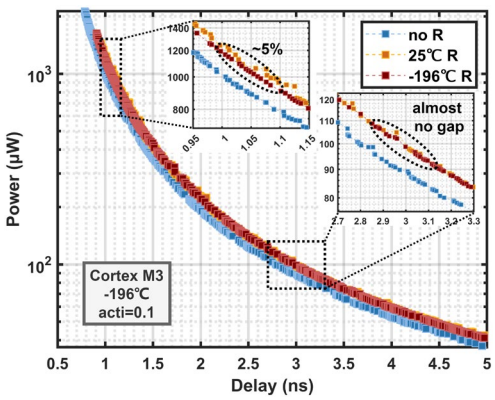


Fig. 3. The PD curves for Cortex M3 at -196°C, using 1vt,1vd configuration, along with aging effects, and various interconnect models: (a) no R: excluding interconnect resistance; (b) 25°C R: original PROCEED interconnect model; (c) -196°C R: accurate interconnect model.

1) *Accurate Interconnect Model:* Unlike PROCEED's basic interconnect model, PROCEED-LT incorporates detailed interconnect data from physical synthesis, including metal layer lengths, resistance per unit length, and temperature coefficients of resistance (TCR). These inputs enable relatively precise calculation of total resistance and capacitance, essential for evaluating LT computing.

2) *Device Wear-out Model:* PROCEED-LT integrates HCI and BTI aging effects using Cadence RelXpert [20], which estimates V_{th} shifts based on temperature, time, and voltage conditions. HCI effects are modeled as drain current (I_d) degradation, converted into V_{th} shifts for both PFETs and NFETs. These shifts are applied in worst-case power and delay evaluations.

Besides, PROCEED-LT supports discrete width evaluation for FinFET devices by converting effective width into the number of fins. It introduces automated multi-voltage optimization, enabling independent tuning of PFET and NFET V_{th}, as well as multi-V_{dd} and multi-V_{th} distribution based on logic path depth. This reduces manual intervention and improves efficiency for optimizing diverse designs.

C. Calibration of PROCEED-LT

To validate PROCEED-LT at low temperatures, we used a commercial synthesis tool to compare its PD predictions. The framework was first calibrated at 85°C and then applied to predict power and delay at -196°C across various V_{dd} and V_{th} configurations. PROCEED-LT achieves power prediction errors under 7%, closely matching RTL compiler results under LT conditions. PROCEED-LT evaluates each voltage configuration in under a minute and optimizes a PD curve within hours, enabling efficient analysis across a wide performance range.

IV. Experiment Results

To evaluate the advantage of LT computing and how different temperature-dependent factors affect the circuit-level optimization for LT computing, we present the experiment results generated by PROCEED-LT. A typical activity factor of 0.1 is set as the default in our benchmarks given that real digital systems often have idle components. We use 10 bins in the optimization. We compare the PD curves of the processor at 85°C and at -196°C under different circumstances. We show the importance of using accurate models to comprehensively evaluate the benefits of LT computing.

A. Impact of Accurate Interconnect Model

An accurate interconnect model can better show the advantage of LT computing. The reduction in the metal resistance per unit length and via resistance of different levels of Cortex M3 at LT and RT is shown in Table I. Due to the reduction in metal and via resistances as temperature decreases, the interconnect resistance at -196°C decreases by 32% when compared to its value at 85°C.

Fig. 3 shows PD curves under -196°C for three scenarios: no interconnect resistance, a simple interconnect model in PROCEED, and an accurate model in PROCEED-LT. At -196°C, utilizing the PROCEED-LT interconnect model registers approximately 5% less power consumption at the high-performance range than the original PROCEED interconnect model, which bases its calculations only on room temperature parameters without accounting for the precise resistance of different metal layers and vias. At lower performance, both models converge, indicating minimal impact of interconnect resistance discrepancies. As shown in Table II, at 1.5ns and 85°C, PROCEED-LT's interconnect model shows ~2% higher power consumption than the original model. Between -196°C and 85°C, power improvements range from 12.18X to 12.54X, highlighting that LT benefits in signal delay are less influenced by interconnect resistance. However, the reduced interconnect resistance at LT plays a more significant role in the benefits of improved IR drop, as will be demonstrated in Section IV.

B. Impact of the Aging Model

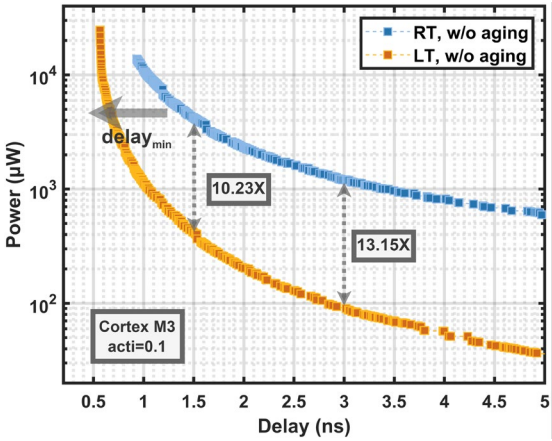
As discussed in Section II-C, LT conditions can mitigate processor aging effects. Fig. 4 shows the PD curves of Cortex M3 at 85°C and -196°C with and without the aging effect. At high performance (e.g., 1ns), power at RT increases rapidly due to aging, whereas at LT, the impact is negligible (~1%). The difference in aging effects at RT and LT is attributed to the fact that the aging effect is not only influenced by temperature but also ($V_{dd} - V_{th}$). To achieve high performance, a larger ($V_{dd} - V_{th}$) is required to increase switching speeds, which exacerbates the influence of HCI. Conversely, at -196°C, it is

TABLE I. Reduction in the metal resistance of per unit length and via resistance of Cortex M3 at -196°C compared to 85°C.

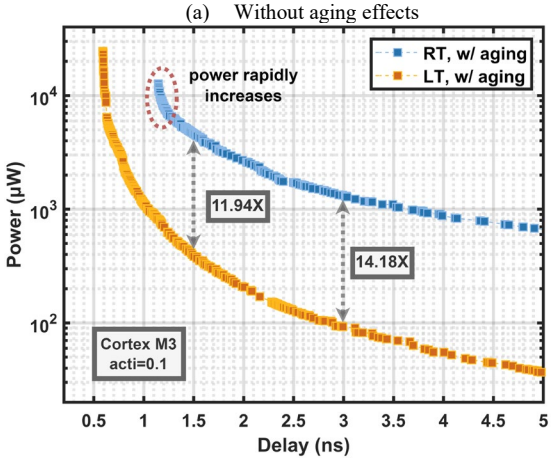
Metal Level	ΔR_w	Via Level	ΔR_v
M1	43.6%	V1	14.6%
M2	43.6%	V2	16.3%
M3	43.6%	V3	15.5%
M4	51.8%	V4	16.3%
M5	50.0%	V5	16.3%
M6	57.9%	V6	17.3%

TABLE II. Power comparison of Cortex M3 between -196°C and 85°C using different interconnect models with the activity factor of 0.1 at 1.5ns circuit latency.

Interconnect Model	Power (mW) and improvement		
	85°C	-196°C	*Improvement*
no R	4.748	0.364	13.04X
PROCEED	5.140	0.422	12.18X
PROCEED-LT	5.242	0.418	12.54X



(a) Without aging effects



(b) With aging effects

Fig. 4. The PD curves of Cortex M3 at 85°C and -196°C with and without the aging effect, using 1vt,1vd configuration along with an accurate interconnect model.

possible to substantially reduce the voltage stress without compromising performance, thereby alleviating the impact of HCI. Furthermore, aging restricts performance at 85°C (<1.1ns), whereas at -196°C, performance limits are only evident at extreme speeds (<0.7ns). This highlights LT computing's advantages for high-performance, long-term stable applications.

C. Impact of Activity Factors in LT Operations

At LT, reduced leakage currents make processor power predominantly dynamic, while at room temperature (RT), leakage power remains significant at low activity factors. This makes LT computing more advantageous for low activity factors.

Fig. 5 shows PD curves for Cortex M3 with activity factors of 0.1 and 0.01 at 85°C and -196°C. LT conditions are observed to substantially elevate peak performance across multiple activity factors, more than doubling it with comparable power usage, facilitating low delays under 1ns. As the activity factor decreases to 0.01, Cortex M3 achieves a 13.43X improvement in power efficiency at LT rather than 11.86X with an activity factor of 0.1 at 1.5ns. Table III shows the power of various activity factors at 85°C and -196°C for Cortex M3 and ACOUSTIC. These results demonstrates that LT processors gain more benefits at lower activity factors than at RT.

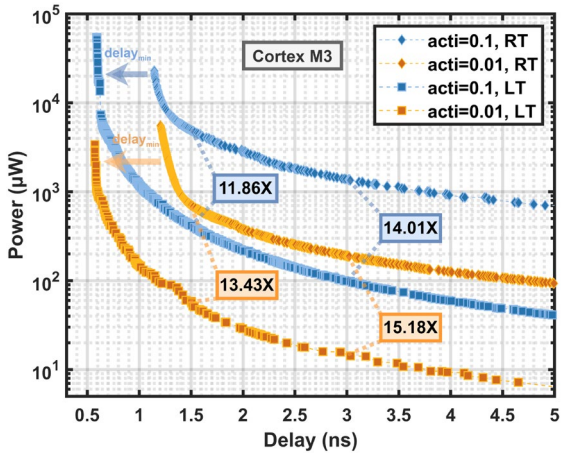


Fig. 5. The PD curves of Cortex M3 using 1vt,1vd at 85°C and -196°C with different activity factors.

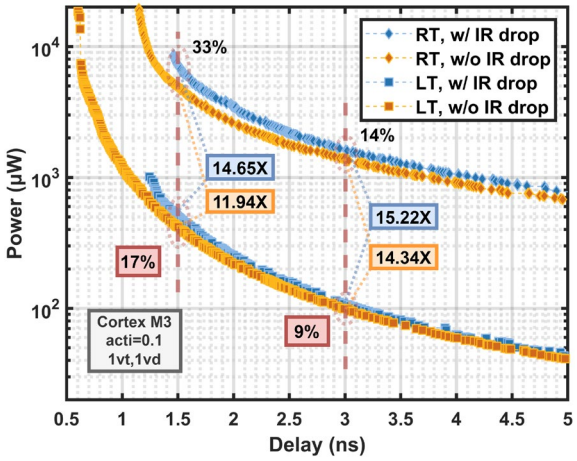


Fig. 6. The PD curves of Cortex M3 using the accurate interconnect model, 1vt,1vd configuration, and an activity factor of 0.1, considering aging effects, with and without IR drop at 85°C as well as -196°C.

D. Potential Improvement of IR Drop at LT

The static IR drop, often overlooked in cryogenic computing, arises from current flow through resistive paths,

TABLE III. TOTAL POWER COMPARISON OF VARIOUS ACTIVITY FACTORS BETWEEN -196°C AND 85°C AT 1.5NS CIRCUIT LATENCY.

(a) Cortex M3

Activity factor	Power (mW) and improvement		
	85°C	-196°C	*Improvement*
0.2	10.164	0.803	12.66X
0.1	4.957	0.418	11.86X
0.05	3.032	0.231	13.12X
0.01	0.685	0.051	13.43X
0.001	0.132	0.007	18.86X

(b) ACOUSTIC

Activity factor	Power (mW) and improvement		
	85°C	-196°C	*Improvement*
0.5	24.532	3.076	7.97X
0.3	16.615	1.531	10.85X
0.1	6.367	0.578	11.02X
0.01	0.920	0.069	13.25X
0.001	0.189	0.009	21.88X

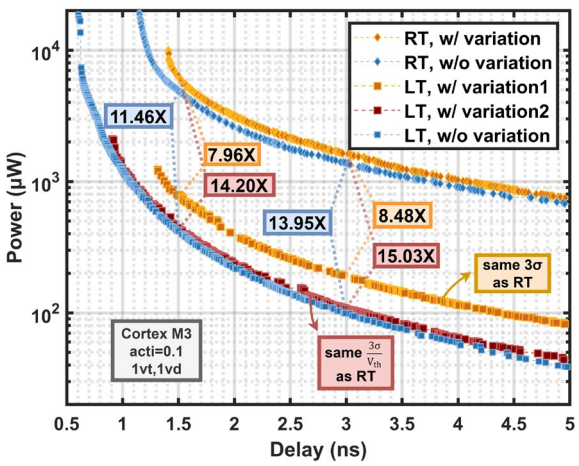


Fig. 7. The PD curves of Cortex M3 using the accurate interconnect model, 1vt,1vd configuration, and an activity factor of 0.1, considering aging effects, with and without V_{th} variation under RT and LT. Variation1: the same 3σ as RT in V_{th} variation; Variation2: the same $\frac{3\sigma}{V_{th}}$ as RT in V_{th} variation; w/o variation: excluding V_{th} variation influence.

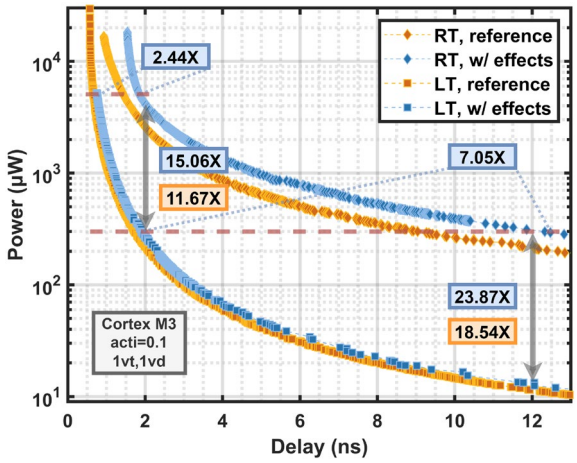


Fig. 8. The PD curves of Cortex M3 using the accurate interconnect model and 1vt,1vd configuration at 85°C and -196°C. Reference: without considering any other effect; W/ effects: considering effects of aging, IR drop, and V_{th} variation.

potentially causing timing issues and suboptimal thermal behavior [25]. At LT, reduced interconnect resistance mitigates IR drop [26].

We compare the PD curves of Cortex M3 using the 1vt1vd configuration with and without IR drop at 85°C and -196°C in Fig. 6. Assuming a 10% supply voltage drop at 85°C, effective resistance and corresponding IR drop are calculated for LT using TCR and average current at an activity factor of 0.1. At lower frequencies (3–4ns), LT reduces IR drop impact by ~5% compared to RT. At higher performance, LT's lower required $(V_{dd} - V_{th})$ reduces operating current. The effect of IR drop is more pronounced at 85°C, with a 33% increase in power at lower delays, almost 2X of the 17% increase observed at -196°C for equivalent performance (1.5ns). Overall, with the same circuit architecture, LT computing demonstrates greater resilience to IR drop.

E. Impact of V_{th} Variation at LT

Attention should be paid to the V_{th} variation of the devices, which can result from a variety of process factors in manufacturing. We utilize Monte Carlo simulations in Cadence to get the 3σ of V_{th} shift of the device.

The impact of V_{th} variation on PD curves of Cortex M3 at RT and LT can be seen in Fig. 7. At LT, the same 3σ variation doubles power at a given performance, compared to a 17% increase at RT. The comparable 3σ ΔV_{th} values have a tangible impact on the PD characteristics, with more significant effects at cryogenic temperatures. This amplified impact at LT arises from scaled-down V_dd and V_{th}, making circuit characteristics more sensitive to V_{th} changes. Hence, a comparable V_{th} variation imposes a greater impact at LT. In Fig. 7, if the V_{th} variation at LT maintains an identical $\frac{3\sigma}{V_{th}}$ value as RT's (variation2), the PD curves can have a power penalty (around 10%) with no variation case. To mitigate the effect of V_{th} variation, it is necessary to improve the current process to reduce the 3σ ΔV_{th} variation as the V_{dd} and nominal V_{th} are scaled down. This adjustment is crucial for ensuring that LT circuits can leverage the LT benefits without disproportionately suffering from the adverse effects of V_{th} variations.

F. Peak Performance Improvement at LT

High peak performance is essential for applications demanding real-time processing and high-speed data analysis. LT computing can achieve higher peak performances even by considering multiple effects such as the aging, the IR drop, and the V_{th} variation.

In Fig. 8, we compare the performance at RT and LT under equivalent power limitations. We apply an identical $\frac{3\sigma}{V_{th}}$ value as RT to assess the V_{th} variation at LT. A high operational voltage stress is necessary to satisfy the high-performance requirement at RT, exacerbating the aging and the IR drop effects and leading to a sharp increase in power consumption. In contrast, at LT, these factors, which often degrade performance at higher temperatures, are more effectively mitigated. Under equivalent power constraints in the reference case, for example, 5 mW, the improvement in performance at LT compared to RT can reach 2.15X. This advantage becomes more pronounced when multiple effects are considered, achieving a 2.44X improvement. As the power limitation decreases, the performance gap between LT and RT enlarges. Notably, the achievable peak performance at LT increases to 1.65X that of RT, while this improvement rises to 2.04X with a 3.51X power improvement when considering these effects similarly. In conclusion, the experiment results demonstrate that the circuit operations under LT conditions are more resilient against various performance-degrading factors.

V. Conclusion

In summary, in order to reveal the circuit-level advantages and challenges of LT computing a wide power-performance range, this work develops PROCEED-LT, a Pareto-based device-circuit co-optimization tool for low-temperature computing, adding support for temperature-dependent interconnect model, an aging model, and FinFET devices. LT

computing promises lower interconnect resistance, slowed down device wear-out, low leakage, and high drive current at lower voltages. For high-performance regimes, LT delivers 10X power improvement compared to RT which improves further to nearly 12X when reduced aging is accounted for. When improved IR drop due to improved interconnect resistance and reduced currents are taken into account, the LT-RT energy difference increases to 14X. Low leakage in LT operation for low-activity factor scenarios further improves its energy benefit over RT to as much as 21X. Furthermore, achievable peak performance in LT can improve by over 2X compared to RT. Our results further indicate that control of V_{th} variation to the same percentage levels as RT is critical to preserve LT benefits.

ACKNOWLEDGMENT

This work is funded by the Defense Advanced Research Project Agency (DARPA) under Low Temperature Logic Technology (LTLT) project. Any opinions, findings, or conclusions expressed in this material are those of the authors and do not necessarily reflect the views of DARPA.

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