On Comparing Conventional and Electrically Driven OPC Techniques

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ABSTRACT

This paper compares the range of accepted layouts produced by conventional Shape Driven Proximity Correction (SDOPC) and Electrically Driven Optical Proximity Correction (EDOPC). For SDOPC, correction is repeated until the geometry matches a target layout. In EDOPC, correction is repeated until the electrical properties meet electrical requirements.[1–6] Using electrical objectives results in a smaller fragmentation requirement for an equivalent current accuracy as SDOPC. Number of candidate OPC solutions accepted by EDOPC is orders of magnitude higher than SDOPC leading to potentially much faster convergence. Moreover, due to additional flexibility in EDOPC, it is able to correct several layouts which are not correctable by SDOPC under the same fragmentation.

Keywords: Electrical OPC, Electrically Driven OPC, Performance Driven OPC, EDOPC.

1. INTRODUCTION

In the manufacturing process, both wavelength (λ) of light and the numerical aperture (N.A.) have largely stagnated while the critical dimension (CD) of printed technology has decreased. Better resolution has come from using Resolution Enhancement Techniques (RET) such as OPC. At modern technology nodes, OPC runtime and fragmentation is growing faster than the critical dimension is shrinking. In order to reduce OPC complexity, electrical information can be fed into the OPC flow. By passing electrical information of a design to the manufacturer, the functionality of the resulting printed circuit can be the primary goal of OPC, while the layout is used as a general target. It has been suggested that this change in the target of OPC produces an increase in electrical accuracy, a decrease in the fragmentation size, and a faster algorithm runtime.[1–6,8]

In a typical edge-based SDOPC flow, a mask is generated and the simulated contour is examined and compared to the design layout. All edges are examined to see if they are within a tolerable distance from the intended position. Any edges outside this range are considered Edge Placement Errors (EPE).[12,14] The EPE information is fed back into the OPC algorithm, the mask is corrected, and the process repeats until the mask is error free. In a typical EDOPC flow, the EPE check is replaced with an electrical test. The lithography simulation usually results in non-rectangular images, therefore, more complex transistor modeling is needed. In the poly region, for example, a sliced-transistor model can be used to estimate the ON current of a transistor. In the sliced-transistor model,[13] a non-rectangular transistor is represented by many constant length transistors in parallel. The current of each slice is added up to determine the current of the entire transistor.

Previous publications on the benefits of EDOPC have shown a reduction in mask complexity compared to SDOPC, ranging from 33-93%.[2,5,6] Additionally, an 11% to 97% reduction in performance variation[5] has been measured, which supports the possibility of guardband reduction.[1] EDOPC can allow correction to be skipped or minimized on non-critical circuit elements. As an extreme example, SDOPC will wastefully correct the printing of company logos drawn in metal layers on circuits.[8] Many or all of these improvements have been seen simultaneously. The cost of EDOPC is that the designer must feed forward the electrical information of circuit elements to the OPC process.

This paper compares EDOPC to SDOPC both experimentally and mathematically. The geometrical setup is described in section 2. The mathematical and experimental models are described in sections 3 and 4 respectively. Finally, the results are examined to see how EDOPC compares with SDOPC in terms of fragmentation, ON current accuracy, and solution count.

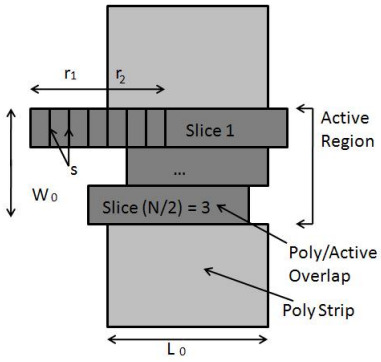

Figure 1. Geometry of layout representing all OPC solutions for a fragmentation with N = 6 edges. The poly/active overlap region is cut in to 3 slices, with each slice having two edges. Possible edge placements are shown for the left edge of the first slice.

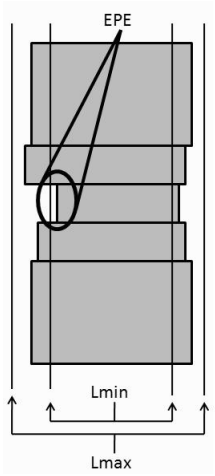

Figure 2. Example of post-lithography contour. There is an edge placement error on the middle left fragment.

2. GEOMETRICAL SETUP

Consider a simple gate represented by the overlap of the poly and active layers. The geometry of the layout is shown in Figure 1. The overlap is fragmented into N edges and each edge is allowed to be shifted in steps of S inward in a range of r_1 or outward by in a range of r_2 for a total range of R for OPC. This setup results in roughly $(\frac{R}{S}+1)^N$ possible layouts (i.e. candidate OPC solutions).

The number of candidate OPC solutions (expected to be proportional to OPC runtime) increase exponentially with fragmentation. Using a 1 nm step size, Table 1 shows the number of possible OPC solutions at $R = 4nm$ and $R = 14nm$. These values are determined by small test layouts used to establish a baseline positioning for the edges in the experiment. Table 2 contains a very rough estimate of how much time a single layout would spend in the lithography simulator (assuming exhaustive enumeration of all candidate solutions). Examining this data makes it clear that using 8 fragments for this experiment would be infeasible for layouts that use anywhere near the 14 nm maximum range of motion. This occurs for more than half of the test layouts. To compensate for this, when 8 fragments are used, the step size is increased to 2.5nm. All further references to N = 8 layouts in this paper refer to an N = 8 layout using 2.5nm step size, while the other layouts are done at 1nm step size. Although comparing results with different step sizes is not a fair comparison, the results are included to present a general idea of what happens at N = 8.

Table 1. Number of test cells in solutions for different values of N and R at 1 nm step size.

N	$R = 4nm$	$R = 14nm$
2	16	196
4	256	38416
6	4096	7529536
8	65536	1475789056

After lithography simulation, each printed contour must be checked for geometrical and electrical accuracy. A geometrically correct model is one that has no Edge Placement Errors (EPEs). An error threshold is set, where if the distance error of each edge is within this threshold then the edge is correctly placed. A good design is one with no EPE's. Figure 2 shows an example of a slice that has an EPE since its edge falls outside of the Lmin to Lmax region. Equations (1 - 4) contain the

Table 2. Approximate run time for different values of N and R at 1 nm step size.

N	$R_{min} = 4nm$	$R_{max} = 14nm$
2	1 min	1 min
4	1 min	10 min
6	15 min	7 hours
8	2 hours	2 months

derivation of the edge placement boundaries from ON current boundaries.

$$I_{MIN} < I_X < I_{MAX} \tag{1}$$

$$k * \frac{W_0}{L_0}(1-\epsilon) < k * \frac{W_0}{L_x} < k * \frac{W_0}{L_0}(1+\epsilon) \tag{2}$$

$$\frac{L_0}{(1+\epsilon)} < L_x < \frac{L_0}{(1-\epsilon)} \tag{3}$$

$$L_{MIN} = \frac{L_0}{(1+\epsilon)}, L_{MAX} = \frac{L_0}{(1-\epsilon)} \tag{4}$$

EDOPC uses electrical information directly when analyzing the correctness of a layout. With a transistor slicing model,[13] a transistor with varying length can be divided into smaller width transistors of constant length. Figure 3 shows a sliced transistor. Each transistor is effectively modeled as many smaller width transistors in parallel. The total current across the transistor is the sum of the currents of each of the smaller transistors.

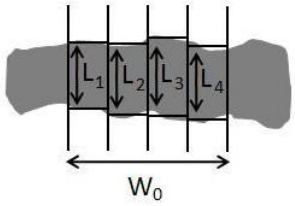

Figure 3. Transistor sliced into 4 equal width segments. Each slice is approximated as a rectangular transistor.

In SDOPC, both experimental and mathematical models attempt to find the difference between the actual edge placement and the ideal edge placement in order to identify the existence of EPE's within a layout. For EDOPC, both models attempt to find the effective ON current of each device using a transistor slicing model and compare to the target ON current.

3. MATHEMATICAL MODEL

The goal of the mathematical model is to provide insight in to the differences between SDOPC and EDOPC in a clear and simple manner. Mask Error Enhancement Factor (MEEF)[9–12] is used to model lithography. MEEF is intended to quantify the movement of mask edges when there is an error in the mask. For example, if OPC causes a mask edge to be moved by a distance X_{mask} then the edge on the printed contour will move a distance of X_{mask}*MEEF.

For SDOPC, this mathematical model uses Edge-based SDOPC. Therefore, every edge must be placed within the edge placement boundaries derived in Equation (4). Beginning with edge placement limits and assuming MEEF to be constant, Equations 4 - 10 derive a closed form expression to approximate the percent of accepted solutions for SDOPC. Let $\frac{L_x}{2}$ be half the target length ($\frac{L_0}{2}$) plus some variation determined by OPC edge movement and lithography. Equation 7 shows the substitution where Δ represents the OPC perturbation and MEEF represents the effects of lithography on the edge movement. The OPC perturbation is modeled as a uniformly distributed random variable on the range $-r_1$ to r_2. The

product $MEEF * \Delta$ is the edge deviation in the printed contour. To simplify the integration, it is assumed that the range of motion of each edge is large enough such that both edges can cause EPE's.

$$\frac{L_0}{(1+\epsilon)} < L_x < \frac{L_0}{(1-\epsilon)} \tag{5}$$

$$\frac{L_0}{2*(1+\epsilon)} < \frac{L_x}{2} < \frac{L_0}{2*(1-\epsilon)} \tag{6}$$

$$\frac{L_0}{2*(1+\epsilon)} < \frac{L_0}{2} + MEEF * \Delta_x < \frac{L_0}{2*(1-\epsilon)} \tag{7}$$

$$\frac{L_0}{2*MEEF} * (\frac{1}{(1+\epsilon)} - 1) < \Delta_x < \frac{L_0}{2*MEEF} * (\frac{1}{(1-\epsilon)} - 1) \tag{8}$$

$$\text{SDOPC acceptance probability} = \int_{\frac{L_0}{2*MEEF} * \frac{\epsilon}{(1+\epsilon)}}^{\frac{L_0}{2*MEEF} * \frac{\epsilon}{(1-\epsilon)}} PDF(\Delta_x) \tag{9}$$

$$\text{For N edges: } (\frac{L_0}{MEEF*(r_1+r_2)} * \frac{\epsilon^2}{1-\epsilon^2})^N \tag{10}$$

We use a similar technique to solve for the number of acceptable solutions produced by EDOPC. Beginning with the ON current equation from transistor slicing (Equation 11), we derive the boundaries of integration for the PDF to solve for the final probability.

$$\frac{W_0}{L_0} * (1-\epsilon) < \sum_{i=1}^{\frac{N}{2}} (\frac{W_0/\frac{N}{2}}{L_i}) < \frac{W_0}{L_0} * (1+\epsilon) \tag{11}$$

$$\frac{(1-\epsilon)}{L_0} < \frac{1}{\frac{N}{2}} * \sum_{i=1}^{\frac{N}{2}} (\frac{1}{L_i}) < \frac{(1+\epsilon)}{L_0} \tag{12}$$

$$\frac{(1-\epsilon)}{L_0} < \frac{1}{\frac{N}{2}} * \sum_{i=1}^{\frac{N}{2}} (\frac{1}{L_0 + MEEF_{L,i} * \Delta_{L,i} + MEEF_{R,i} * \Delta_{R,i}}) < \frac{(1+\epsilon)}{L_0} \tag{13}$$

Using a first order Taylor Series approximation, we get the following:

$$\frac{(1-\epsilon)}{L_0} < \frac{1}{\frac{N}{2}} * [\sum_{i=1}^{\frac{N}{2}} \frac{1}{L_0} - \frac{MEEF}{L_0} * \sum_{i=1}^{\frac{N}{2}} (\Delta_{L,i} + \Delta_{R,i})] < \frac{(1+\epsilon)}{L_0} \tag{14}$$

$$\frac{N}{2} * (\frac{(1-\epsilon)}{L_0} - \frac{1}{L_0}) < MEEF * \sum_{i=1}^{\frac{N}{2}} (\Delta_{L,i} + \Delta_{R,i}) < \frac{N}{2} * (\frac{(1+\epsilon)}{L_0} - \frac{1}{L_0}) \tag{15}$$

The uniform random variable (Δ) has the same distribution for each edge. Assuming that the values of Δ at each edge are independent of each other, the middle term of Equation 15 can be simplified to a single Gaussian Random Variable (GRV), using the Central Limit Theorem. The GRV has mean and variance equal to the sums of the means and variances of each uniform random variable and is represented by δ in equation 17. Fragmentation is small, so this approximation is less reasonable for N = 2 or 4, and more reasonable for N = 6 or 8, due to properties of the Central Limit Theorem. Assuming MEEF to be constant, it can be shifted to the limits of the integral for the Gaussian PDF, allowing for a closed form solution to be calculated in Equation 18.

$$\frac{-\epsilon*N}{2*MEEF*L_0} < [\sum_{i=1}^{2*\frac{N}{2}} \Delta] < \frac{\epsilon*N}{2*MEEF*L_0} \tag{16}$$

$$\text{EDOPC acceptance probability} = \int_{LB}^{UB} \delta(\mu, \sigma^2) \tag{17}$$

$$\text{Where LB} = \frac{-\epsilon*N}{2*MEEF*L_0}, \text{ and UB} = \frac{\epsilon*N}{2*MEEF*L_0}$$

$$\text{EDOPC acceptance probability} = (erf(\frac{UB-\mu}{\sigma}) - erf(\frac{LB-\mu}{\sigma})) \tag{18}$$

$$\text{Where } \mu = N * \mu_\Delta, \text{ and } \sigma^2 = \frac{N}{2} * \sigma_\Delta^2$$

Note that erf is the error function that is the result of integrating a Gaussian PDF. Real values for L_0, MEEF, and number of slices are inserted into Equation 18 to determine the percent of accepted EDOPC solutions. The range values r_1 and r_2 are used to find the mean and variance of the URV. Table 3 shows the numerical results of the mathematical analysis.

Table 3. Percent Accepted Solutions for EDOPC and SDOPC at Varying Fragmentation and Maximum Current Error Calculated Mathematically.

Fragmentation [N]	**ED, ϵ = 1%**	**ED, ϵ = 2%**	**ED, ϵ = 3%**	**SD, ϵ = 1%**	**SD, ϵ = 2%**	**SD, ϵ = 3%**
2	27.6%	51.9%	71.0%	0.0002%	0.0033%	0.0168%
4	38.2%	68.2%	86.5%	0.0000%	0.0000%	0.0000%
6	45.9%	77.8%	93.3%	0.0000%	0.0000%	0.0000%
8*	51.9%	84.2%	96.6%	0.0000%	0.0000%	0.0000%

It is clear EDOPC is likely to converge much faster to a solution than SDOPC. Moreover, the percent of solutions accepted by EDOPC increases with fragmentation, while for SDOPC the percent decreases with fragmentation. In EDOPC, different slices can compensate each other's error resulting in more accepted solutions with increasing framentation. For SDOPC, the number of candidate OPC solutions increases exponentially with fragmentation while the number of acceptable solutions does not, since the number of EPE checks also increases.

4. EXPERIMENTAL MODEL

To examine the OPC results experimentally, layouts are generated using OpenAcess API.[18] A layout of repeated lines with varying lengths and pitches is used to form a simple basis for rule-based OPC. This mapping is used to reduce the number of OPC solutions from Table 1 to a more manageable set.

The test layouts are generated in 65nm technology with a 72nm minimum linewidth. Five test layouts have been chosen to mimic common geometries found in the Nangate OpenCell Library.[17] Areas are taken from NAND2_X1, DFFSR_X1, and SDFF_X1 cells (Figure 4). These cells were selected because they can be commonly found in most designs. The NOR and XOR topologies are included in the NAND topology, since the poly layers in all these layouts are fairly simple and can be approximated by the same test cell. Each layout is simulated at varying pitch, from 160 to 400nm, and at varying fragmentation, from 2 to 8 fragments. Each fragmented area being examined has a dummy poly line on each side. These lines mimic the geometries from the surrounding the test areas from the library cells. Similarly, the area above and below the OPC test area is used to mimic the library cell geometry.

The layouts are run through the Mentor Calibre lithography simulator[16] and then imported back into OpenAccess. Using allowable electrical error and channel length to derive the length boundaries as in Equation (4), each test region is checked for SDOPC correctness in two ways. First, in the Edge-based SDOPC method, the midpoint of each edge is found and it is confirmed that this point lies within the edge placement boundaries. Next, in the CD-based SDOPC method, the critical dimension of each slice is determined as the difference of two edge midpoints on the same slice. This number is compared against the effective length boundaries. Finally, EDOPC is checked by determining the area of the test region and assuming that the width has not changed (since the active region is assumed to not change and the poly line extends far enough to ensure no shorts), the effective channel length can be determined by $L_{effective} = \frac{Area}{W_0}$, and is compared against the effective length boundaries.

5. RESULTS

The results of the experimental analysis are shown in Tables 4 - 7. Table 4 shows the percent of tested layouts that EDOPC and SDOPC could successfully correct. Here it can be seen that EDOPC finds an acceptable layout in 93.75% to 100% of the cases. CD-based and Edge-Based SDOPC both have noticeable difficulty correcting layouts at N=8 fragmentation. Edge-based SDOPC also has difficulty in finding a solution at tight error boundries ($\epsilon = 1\%$). In the other cases, SDOPC finds over 90.63% of the layouts to be correctable. The difficulty in correcting the N=8 test case is that it has a step size of 2.5nm, unlike other test cases that have a 1.0nm step size. The large step size makes it difficult for edges to be placed correctly. Similarly, for Edge-Based SDOPC at $\epsilon = 1\%$, there is a very small range of accepted edge positions. EDOPC, however, does not share this difficulty in finding solutions for either large step size or tight error restrictions. It is very important to keep these numbers in mind when exmaning the rest of the data tables. The results for the remaining tables are only for layouts where solutions were found by OPC. In the Edge-Based SDOPC case where ($\epsilon = 1\%$), for example, there are very few correctable layouts and therefore the mean results can be misleading since they are a mean of a smaller set than EDOPC or CD-Based SDOPC of equivalent ON current error and fragmentation.

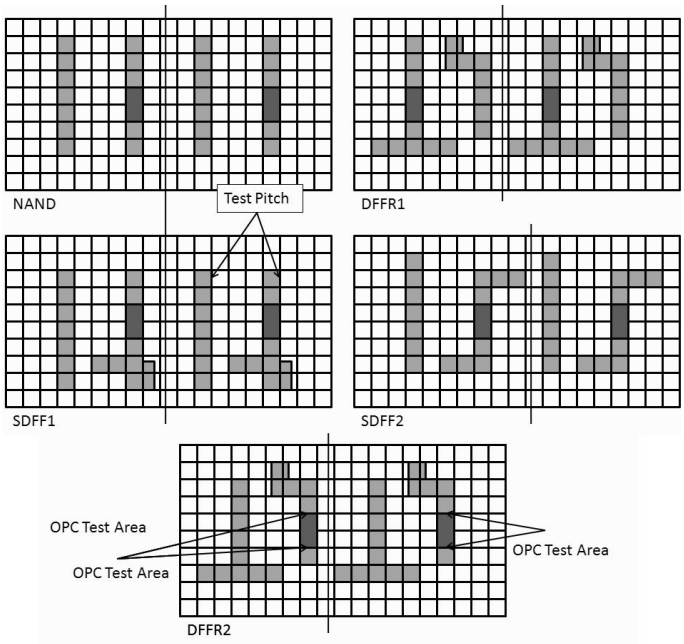

Figure 4. Test Layouts. Each image shows two consecutive test cells. The poly lines maintain the same pitch within each layout.

Table 4. Percent of correctable experimental layouts for EDOPC and SDOPC at varying fragmentation and maximum current error. Correctable means that at least one OPC layout passed either the EDOPC or SDOPC checks. *Note that $N = 8$ Fragmentation has a 2.5nm step size while other fragmentations have 1.0nm step size.

	EDOPC	**EDOPC**	**EDOPC**	**SD-EDE**	**SD-EDE**	**SD-EDE**	**SD-CD**	**SD-CD**	**SD-CD**
N	$\epsilon = 1\%$	$\epsilon = 2\%$	$\epsilon = 3\%$	$\epsilon = 1\%$	$\epsilon = 2\%$	$\epsilon = 3\%$	$\epsilon = 1\%$	$\epsilon = 2\%$	$\epsilon = 3\%$
2	93.75%	93.75%	93.75%	15.63%	92.19%	93.75%	93.75%	93.75%	93.75%
4	98.44%	100%	100%	4.69%	90.63%	95.31%	93.75%	95.31%	100%
6	100%	100%	100%	12.5%	90.63%	95.31%	93.75%	96.88%	100%
8*	100%	100%	100%	0%	23.44%	70.31%	70.31%	78.13%	92.19%

The percentage of accepted solutions is shown for varying fragmentation and maximum accepted current error in Table 5. These results show that EDOPC accepts a noticeably higher fraction of solutions. EDOPC accepts at least 14.6% of the solutions, while Edge-Based SDOPC accepts at most 10.7%. The CD-Based SDOPC results lie between EDOPC and Edge-based SDOPC, indicating that as OPC tends towards EDOPC-style analysis, the analysis will accept a larger percent of layouts as solutions. As fragmentation increases, the solution count for SDOPC decreases, but the solution count for EDOPC increases. This follows the mathematical model presented earlier. In the experimental model, the edge positions are discrete and the range of edge movement is limited by experimentation to reduce the large number of obviously invalid OPC solutions. This is likely the reason why SDOPC has a higher acceptance rate experimentally than is predicted by the mathematical model presented earlier. Although many assumptions and approximations are made in both models, a difference in accepted solutions of the order of magnitude shown in Table 5 indicates that an EDOPC-based algorithm will generally converge to a solution faster than an SDOPC algorithm and will perform better at coarser fragmentations.

Next, we examine the quality of the solutions found with the experimental analysis. In the ON current analysis (Table 6),

Table 5. Percent Accepted Solutions for EDOPC and SDOPC at Varying Fragmentation and Maximum Current Error Calculated Experimentally. The mean value is given for the percent of accepted solutions across all correctable layouts. *Note that $N = 8$ Fragmentation has a 2.5nm step size while other fragmentations have 1.0nm step size.

	EDOPC	**EDOPC**	**EDOPC**	**SD-EDE**	**SD-EDE**	**SD-EDE**	**SD-CD**	**SD-CD**	**SD-CD**
N	ϵ = 1%	ϵ = 2%	ϵ = 3%	ϵ = 1%	ϵ = 2%	ϵ = 3%	ϵ = 1%	ϵ = 2%	ϵ = 3%
2	14.6%	28.7%	43.0%	2.1%	4.7%	10.7%	13.9%	25.5%	43.2%
4	18.2%	35.1%	52.5%	0.1%	0.3%	1.6%	2.3%	5.9%	17.6%
6	19.5%	39.7%	60.9%	0.0%	0.1%	0.9%	0.6%	2.7%	12.9%
8*	9.0%	18.8%	29.9%	0.0%	0.0%	0.2%	0.1%	0.7%	4.1%

both the minimum current error and mean current error are shown. In all cases, EDOPC has better current accuracy than Edge-based SDOPC, and is comparable to CD-Based SDOPC. As the current error slack and fragmentation increase, it appears that SDOPC can achieve results close to ED-OPC. For example N=6, $\epsilon = 1\%$ case, has the same mean minimum current error as EDOPC, while achieving a better mean mean current accuracy. This is likely because Edge-Based SDOPC is more selective and therefore selects layouts with good current accuracy.

Table 6. Minimum percent ON current error and mean percent ON current error for EDOPC and SDOPC at varying fragmentation (N) and Maximum Current Error (ϵ) averaged over all correctable layouts. The values in the boxes are percentages. *Note that $N = 8$ Fragmentation has a 2.5nm step size while other fragmentations have 1.0nm step size.

	EDOPC	**EDOPC**	**EDOPC**	**SD-EDE**	**SD-EDE**	**SD-EDE**	**SD-CD**	**SD-CD**	**SD-CD**
N	ϵ = 1%	ϵ = 2%	ϵ = 3%	ϵ = 1%	ϵ = 2%	ϵ = 3%	ϵ = 1%	ϵ = 2%	ϵ = 3%
2	0.15/0.16	0.15/0.21	0.15/0.39	0.96/ 0.96	0.86/ 1.12	0.49/ 1.32	0.69/ 0.97	0.44/ 1.15	0.20/ 1.2
4	0.04/0.17	0.04/0.41	0.04/0.82	0.15/ 0.15	0.33/ 0.67	0.10/ 0.73	0.16/ 0.62	0.07/ 0.64	0.07/ 0.77
6	0.02/0.18	0.02/0.57	0.02/1.09	0.25/ 0.25	0.15/ 0.46	0.02/ 0.5	0.08/ 0.41	0.04/ 0.49	0.02/ 0.7
8*	0.02/0.2	0.02/0.67	0.02/1.28	NA/ NA	0.25/ 0.35	0.08/ 0.31	0.07/ 0.24	0.04/ 0.28	0.04/ 0.54

The results for mask complexity are shown in Table 7. For N=2 fragmentation, where there is one fragment on each side of the test region, there are always 4 vertices. The average minimum mask-vertex count across all layouts for EDOPC stays very close to 4 vertices. At 3% ON current error EDOPC finds a 4-vertex solution for every layout that it was able to correct. By limiting the exact geometry of the printed images, SDOPC greatly limits which mask geometries can result in correct OPC solutions. EDOPC does not focus on vertex positions, rather, it focuses on the overall proportions of the shape. EDOPC can accept distorted geometries that SDOPC cannot. SDOPC also has outlier shapes that can pass both EPE and CD tests, as long as the image is printed within the boundaries at the midpoint of each edge. However, this happens much less frequently than a distorted shape being accepted by EDOPC. EDOPC and CD-based SDOPC do not have strict geometrical requirements and can find 4 vertex shapes that are not placed correctly on the layout, but have correct electrical propertes.

Table 7. Minimum mask-vertex count and mean mask-vertex count for EDOPC and SDOPC at varying fragmentation (N) and Maximum Current Error (ϵ) calculated experimentally. The mean value is given for the minimum/mean vertex count across all correctable layouts. *Note that $N = 8$ Fragmentation has a 2.5nm step size while other fragmentations have 1.0nm step size.

	EDOPC	**EDOPC**	**EDOPC**	**SD-EDE**	**SD-EDE**	**SD-EDE**	**SD-CD**	**SD-CD**	**SD-CD**
N	ϵ = 1%	ϵ = 2%	ϵ = 3%	ϵ = 1%	ϵ = 2%	ϵ = 3%	ϵ = 1%	ϵ = 2%	ϵ = 3%
2	4.0/ 4.0	4.0/ 4.0	4.0/ 4.0	4.0/ 4.0	4.0/ 4.0	4.0/ 4.0	4.0/ 4.0	4.0/ 4.0	4.0/ 4.0
4	4.1/ 7.4	4.1/ 7.4	4.0/ 7.4	4.0/ 4.0	5.5/ 6.7	4.9/ 7.0	4.9/ 7.4	4.6/ 7.3	4.2/ 7.3
6	4.1/ 10.5	4.1/ 10.6	4.0/ 10.7	8.3/ 8.3	6.3/ 10.0	5.2/ 10.6	5.9/ 10.7	5.2/ 10.7	4.7/ 10.7
8*	5.0/ 12.6	4.2/ 12.7	4.0/ 12.9	NA/ NA	12.5/ 13.8	8.9/ 13.4	8.2/ 12.8	6.8/ 12.9	5.9/ 12.8

6. CONCLUSIONS AND FUTURE WORK

The results of our experiments support that Electrically Driven OPC can simultaneously achieve better convergence and better ON current accuracy than Shape Driven OPC. Also, current accuracy can be traded for mask complexity, where

EDOPC also shows an improvement on SDOPC. The results indicate that well-implemented EDOPC can be on the order of tens to hundreds of times faster than SDOPC and can simultaneously yield better electrical accuracy. EDOPC is more likely to successfully proximity correct a layout, especially in worse test conditions such as coarser edge placement step size or coarser fragmentation. The ON current accuracy improvements are also significant in that they indicate that EDOPC with a smaller fragmentation can have the same current accuracy as SDOPC with a larger fragmentation.

In future work, the experiment will expand to cover OPC on metal layers. Currently, the analysis only discusses the poly/active overlap region. Therefore, the results may change slightly when field-poly correction is also taken into account. Further analysis will also include a comparison of leakage current, since it is being targeted more often as a primary electrical objective.

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