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Defect Avoidance for Extreme Ultraviolet Mask Defects using Intentional Pattern Deformation

A thesis submitted in partial satisfaction
of the requirements for the degree
Master of Science in Electrical and Computer Engineering

by

Yoo-Jin Chae

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ABSTRACT OF THE THESIS

Defect Avoidance for Extreme Ultraviolet Mask Defects
using Intentional Pattern Deformation

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Master of Science in Electrical and Computer Engineering
University of California, Los Angeles, 2018
Professor Puneet Gupta, Chair

Extreme ultraviolet (EUV) lithography has been adopted as the next generation lithography solution to sub 10nm technology node with many companies claiming to be ready for production by late 2018. Despite the technology's maturity for production, EUV lithography still faces a number of challenges and mask blank defect is a major challenge.

Defect avoidance method has been proposed to allow the mask defects to be tolerated by hiding them under the absorber patterns. By moving the design pattern relative to the defects' positions, more defects can be mitigated with the given absorber pattern. Past works have demonstrated usefulness of some degrees of freedom, however, pattern deformation has not been a subject of study. Hence, this thesis explores the extended benefits of utilizing pattern deformation, including linear asymmetric magnification and second-order deformation, by using new proposed method based on constraint programming.

In the first part of the thesis, we propose a constraint programming based method that can explore pattern shift, small angle rotation, and deformation for defect avoidance. We model the degrees of freedom as a displacement in relative defect location to the absorber, then construct a constraint programming model that takes inputs of defect location, prohibited regions, and ranges of allowed degree of freedom. The framework returns the maximum number of mitigated defects and corresponding degrees of freedom values.

In the second part of the thesis, we utilized this proposed method to explore the benefit of pattern deformation. We intentionally deform the absorber pattern on the mask to allow for

maximum defect avoidance, then this deformation is reversed during its printing on to the silicon wafer through scanner operations. The types of deformation explored in this thesis are linear asymmetric magnification (absorber patterns are magnified to a different x and y value) and second-order deformation where deformation is calculated as a polynomial function of the location on the pattern.

The thesis of Yoo-Jin Chae is approved.

Lei He

Subramanian Srikantes Iyer

Puneet Gupta, Committee Chair

University of California, Los Angeles

2018

To my parents.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGMENT

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Lastly, I want to express my greatest gratitude to my family for their unconditional love and support. I feel incredibly blessed to have such a loving family, especially during this difficult time of our loss.

CHAPTER 1
Introduction

1.1 Motivation

In the past few decades, the semiconductor industry has largely benefited from scaling technology node. Smaller technology node allows for more transistors to be placed on a single chip, reducing the cost for chips per wafer. This exponential rate of growth, known as the Moore's Law, is threatened as scaling technology node becomes more difficult and expensive.

Lithography is the key technology to the next scaled node. Optical lithography has been used for semiconductor manufacturing as it is a reliable and economical mechanism for mass production. Currently, deep ultraviolet (DUV) lithography with 193nm wavelength is being used for mass production. However, it is becoming more difficult to achieve the necessary resolution needed for sub-10nm technology node with DUV. Thus, extreme ultraviolet (EUV) lithography, using 13.5nm wavelength, has gained traction to be the next generation lithography.

EUV production lines are under constructions by Samsung and TSMC. Despite the maturity of the industry for this technology, mass production of sub-10nm is still a challenge. As denoted by the International Technology Roadmap for Semiconductors 2.0 (ITRS) [1], EUV mask defect is a serious bottleneck for the advancement of this technology to mass production.

1.1.1 EUV Mask

Conventional lithography uses light source that passes through a mask and prints a pattern on to a photoresist. However, 13.5nm wavelength used in EUV is absorbed by most materials, making it impossible to use the conventional transparent mask. Thus, reflective masks and optics are used in EUV lithography systems as shown in Figure 1.1.

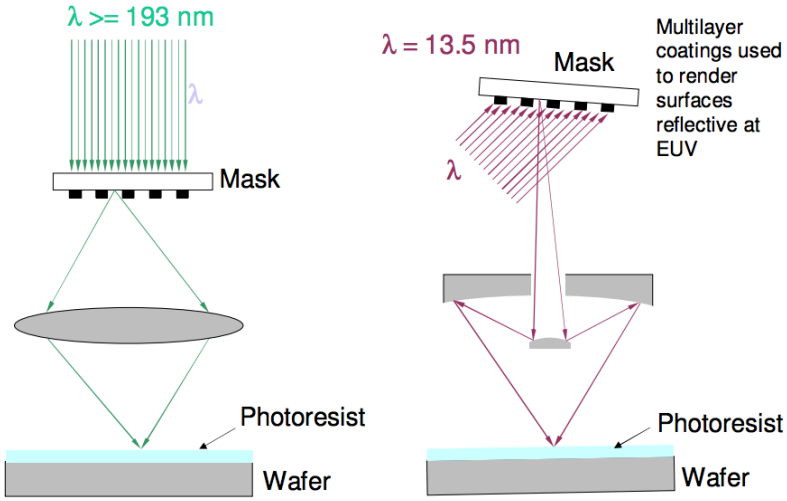

Figure 1.1: Conventional 193nm lithography versus EUV lithography system [2]

To achieve an adequate level of reflectivity, EUV mask blanks are made of multilayers of alternating molybdenum and silicon. These 40 to 50 multilayer structure allows EUV to utilize the principle of Bragg reflectors to maximize the reflection of the 13.5nm wavelength. However, this multilayer structure poses a great difficulty in manufacturing defect-free mask blanks. Multilayer mask blanks are susceptible to buried particle defects which are caused by substrate surface pits or particles introduced during the deposition process.

Buried defects affect the local reflectivity of the mask, causing a critical dimension change in the printed image on silicon wafer. Previous studies have shown that 3.5nm high defect can cause a 20nm change in critical dimension (CD) on the wafer [3]. While defects with less than 10% CD impact are considered printable [4], large change in CD may cause a short in a circuit as shown in Figure 1.2.

1.1.2. EUV Mask Defect Mitigation Methods

In the past, much efforts have been devoted into developing techniques and methods to repair mask blank defects. As shown in Figure 1.3, defect mitigation method can be largely categorized into pre-mask write and post-mask write. Pre-mask write means that the defect mitigation is performed prior to writing the absorber pattern on to the mask blanks, while as post-mask write means the method is performed after the absorber pattern has been written on the mask blank.

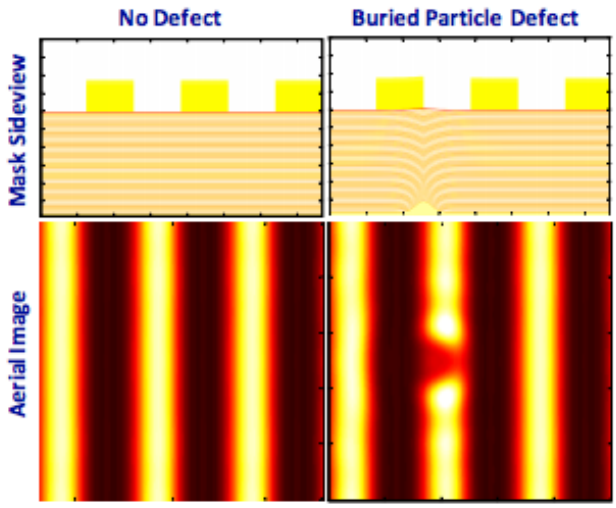

Figure 1.2: EUV mask sideview and its aerial image showing the impact of buried defect [5]

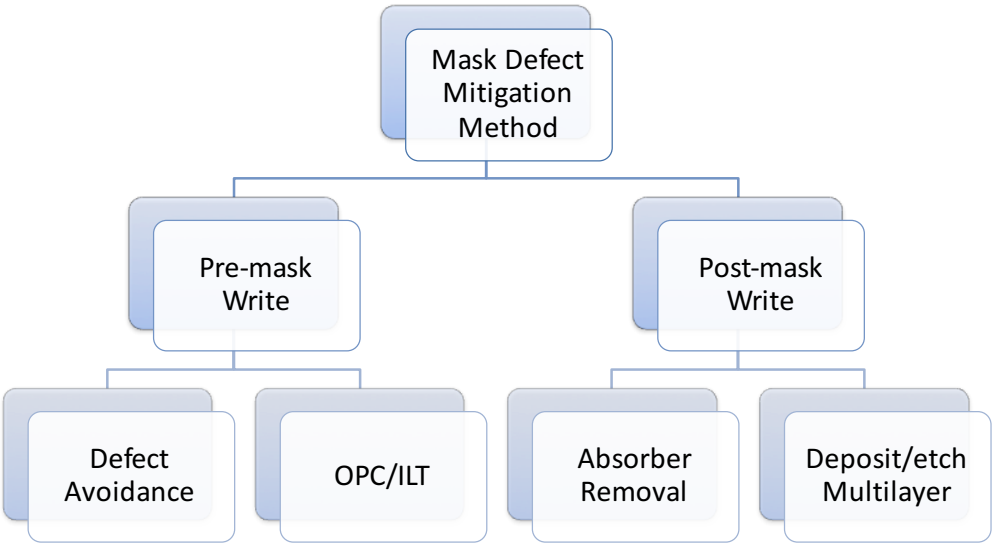

Figure 1.3: Mask defect mitigation methods

Post-mask write methods such as absorber removal and deposit/etch of multilayer are repair methods that physically target the defects. [6] Although these repair methods are available, there is a significant risk of damaging the structure of the mask since the defects are buried under multilayers. [7] Pre-mask write methods, however, utilizes absorber patterns to minimize the impact of defect on printings on silicon wafer. It has been found that aligning the absorber pattern with the defect can mitigate the impact of defect on CD. [8] We can either choose to hide the defect under the absorber pattern or place them far away from absorber edges so that reflectivity around the pattern edges is not compromised. Figure 1.4 shows the flow of pre-mask write defect avoidance method.

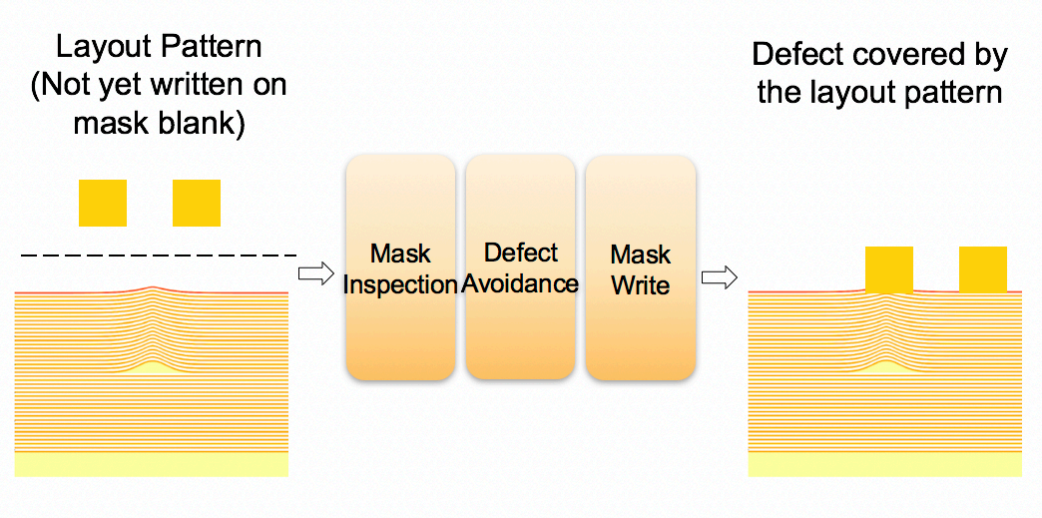

Figure 1.4: Pre-mask write defect avoidance flow

Defect avoidance method uses given absorber pattern to align with the defects, while using of optical proximity correction (OPC) [9] require a modification on the pattern without having functional impact on the chip. In this thesis, we utilize this defect avoidance method to further investigate the benefit of mask defect mitigation using intentional pattern deformation as added degree of freedom to previous works.

1.2. Previous Work on Defect Avoidance

There have been several prior studies that looked at methods to exploit defect avoidance. Zhang et al. proposed a prohibited region method that constructs regions around the edges where defects cannot be placed (Figure 1.5). It models the impact of buried defects on critical dimension and

determines the distance the defect must be placed from the edge to formulate these prohibited rectangles. Kagalwalla et al. proposed simulated annealing method [10] and random walk + gradient descent based solution method [11] that explore pattern shift, small angle rotation and mask floorplanning as part of degree of freedom. Elayat et al. summarized and outlined the cost-benefit analysis of these pre-mask write methods [12].

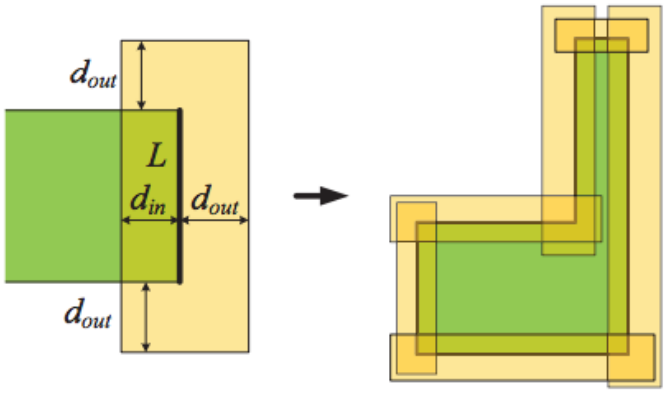

Figure 1.5: Definition of prohibited region [13]

While pattern shift is a sufficient defect avoidance measure for irregular patterns, it is ineffective for regular and unidirectional layout patterns. Kagalwalla et al. provides a pattern shift aware critical density analysis where the results indicate that regular layouts are inadequate to tolerate mask defects through pattern shift. [14] This is due to linear and uniform change in defect location relative to mask pattern in pattern shift. Thus, for regular and unidirectional patterns (such as polysilicon layer in our experiment), non-linear degree of freedom such as rotation and magnification is needed.

Previous studies have also noted that achieving a good accuracy for defect location is a challenge for defect avoidance. Algorithmic approach to address this inspection inaccuracy has been studied by Du et al. [15] and Kagalwalla et al. suggested a design-aware mask inspection methodology to assign criticality to different mask features based on their design impact [16].

1.3 Thesis Outline

Previous studies have looked at pattern shift, rotation, and mask floorplanning as part of their degree of freedom, however, intentional pattern deformation has not been a subject of study as a degree of freedom. In this thesis, we study the feasibility and added benefit of pattern deformation for defect avoidance, by selected sub-aspects – magnification and second order deformation.

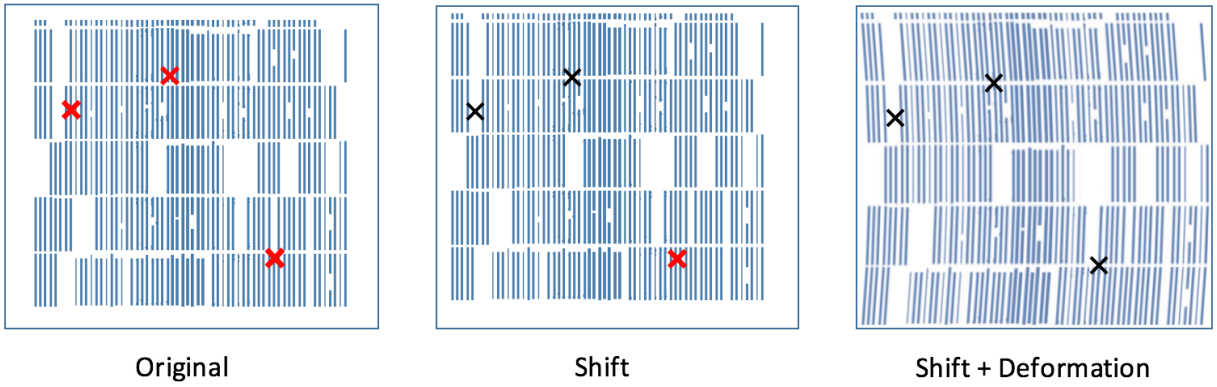

Figure 1.6: Summary example showing benefit of pattern deformation

The key contribution of this thesis are as follows:

- We explore the benefit of intentional pattern deformation for defect avoidance.
- We developed a constraint programming based methodology to compute optimal values for degrees of freedom – pattern shift, rotation and high-order deformation.

This thesis is organized as follows. Chapter 2 describes the degree of freedom used in our study and its conceptual benefit for defect avoidance. Chapter 3 outlines the algorithm and methodology developed to explore the benefit of intentional pattern deformation. It outlines the experimental setup and results using the developed method. It also shows the validation of these results using prohibited region method. Finally, Chapter 4 concludes the thesis.

CHAPTER 2
Degree of Freedom for Defect Avoidance

Defect avoidance allows mitigation of buried defects by minimizing the local change in reflectivity surrounding them. This is achieved by aligning absorber pattern with the defects and hiding them under the absorber. In order to do so, we must compute an optimal alignment value that accommodates for the location of the defects on each mask blank. In this paper, we explore combination of a few different degrees of freedom - pattern shift, rotation and deformation - to find the optimal solution for defect avoidance.

There are constraints that must be satisfied to ensure the manufacturability of the final mask. They limit the degree of freedoms and are dependent on:

1. Size of the usable area of the mask compared to entire mask field size
2. Capability of the lithography tools to correct for deformation
3. Accuracy of lithography tools that determines the resolution for degrees of freedom

These translate to mathematical constraints in problem formation which is further discussed in Chapter 3.

2.1 Pattern Shift

Pattern shift is a degree of freedom that allows the shift of the absorber pattern in x and y direction relative to the mask blank. It is allowed by the available space between the mask field (the absorber pattern) and the usable mask size. The coordinates of absorber pattern are shifted from (x, y) to $(x + d_x, y + d_y)$, where (d_x, d_y) are shifts in x and y directions. The benefits of pattern shift methods of implementation have been explored and developed by several prior studies [8] [13] [17].

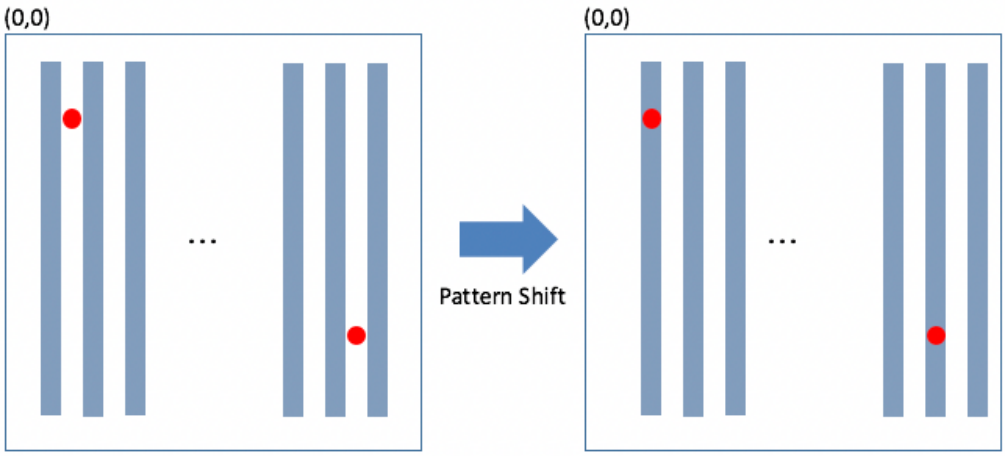

Figure 2.1: Example showing the benefits of pattern shift

While pattern shift may be beneficial in layers with irregular patterns and shapes, it can only provide very limited benefits in layers with repeated regular patterns. For example, in a polysilicon layer, the design pattern consists of equally spaced long parallel lines. This regularity of repeated shapes makes it extremely difficult for defects to be simultaneously hidden under the absorber. As shown in Figure 2.2, the defects may be spaced in a way that both of them cannot be hidden at the same time by this regular pattern. Thus, further degree of freedom must be combined with pattern shift to explore the full extent of the benefits.

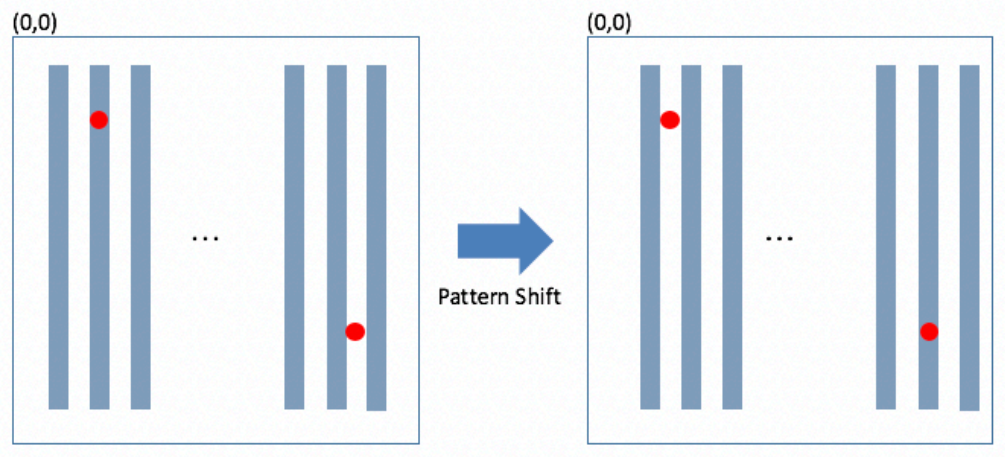

Figure 2.2: Example showing the limitations of pattern shift

2.2 Small Angle Rotation

Rotation allows the absorber pattern to rotate around the center of the mask. Since this change in relative location is not linear across the mask, it is beneficial in layers with regular patterns. Figure 2.3 shows an example of successful defect avoidance with rotation that could not be solved in Figure 2.2.

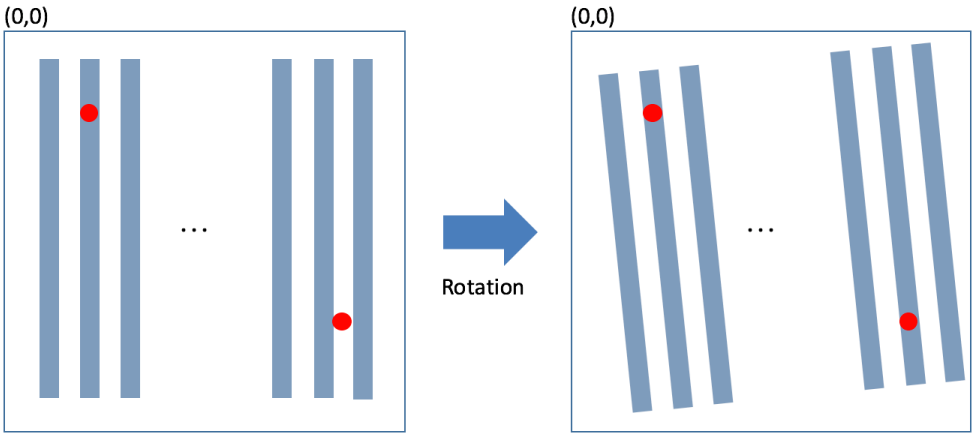

Figure 2.3: Example showing the benefits of rotation

The coordinates of the absorber pattern are shifted from (x, y) to $(x \cdot \cos(\theta) - y \cdot \sin(\theta)$, $x \cdot \sin(\theta) - y \cdot \cos(\theta))$. But since our example uses angles that are very small (less than 3 degrees), we use small angle approximation to replace the sinusoidal functions.

2.3. Pattern Deformation

Pattern deformation intentionally deforms the pattern by magnifying or curving the design to explore the benefits of defect avoidance. As shown in Figure 2.2, pattern shift has limited benefits when the absorber pattern is regular and repeated. Pattern deformation can help overcome this limitation by changing the spacing of the absorber shapes.

This mask pattern deformation is later corrected in process of printing on silicon wafer using scanner operations. Since the deformation correction is dependent on this scanner operations, there is a limitation to the maximum deformation the tools can tolerate. Reasonable limitation values for the purpose of feasibility analysis/demonstration were discussed with our industry partners and

applied in our study. Two different types of pattern deformation were studied in this thesis – magnification and second-order deformation.

2.2.1. Magnification

Magnification involves stretching the absorber pattern in x and y directions. When magnified, the coordinates of the absorber patterns are translated from (x, y) to $(mag_x \cdot x,\ mag_y \cdot y)$. We may choose to magnify the design using different x and y values – asymmetric magnification, or with same value – symmetric magnification. Figure 2.4 and 2.5 show examples in where symmetric or asymmetric magnification can provide improvements.

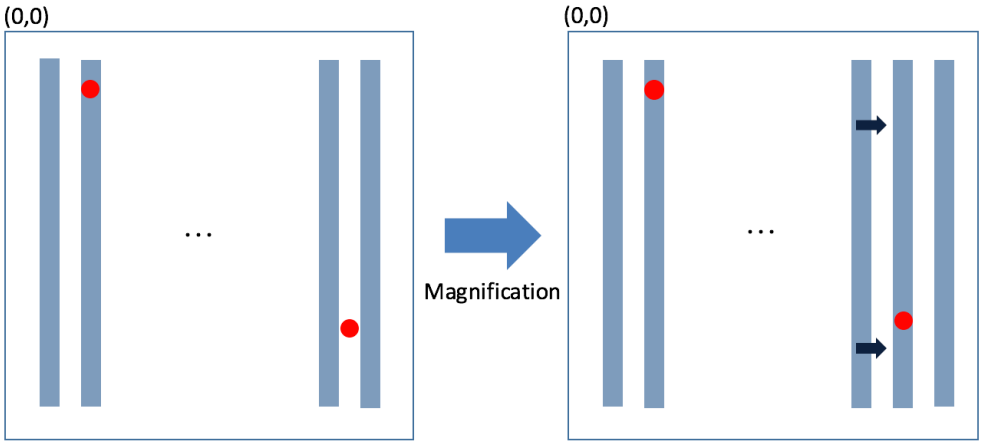

Figure 2.4: One axis relevant example – symmetric or asymmetric magnification

Figure 2.4. shows an example where only one axis is relevant in benefiting defect avoidance. As shown, if the absorber pattern is long parallel shapes, pattern shift and magnification are only relevant in one axis. In this case, symmetric and asymmetric magnification can both provide benefits as one axis becomes irrelevant to magnification. In our experiment, certain metal and polysilicon layers fell under this category as the absorber shapes were long and parallel rectangles. Figure 2.5 shows an example where both axes are relevant. The same principle as in Figure 2.4 applies to Figure 2.5, but the spacing between the defects in both axes is taken into consideration.

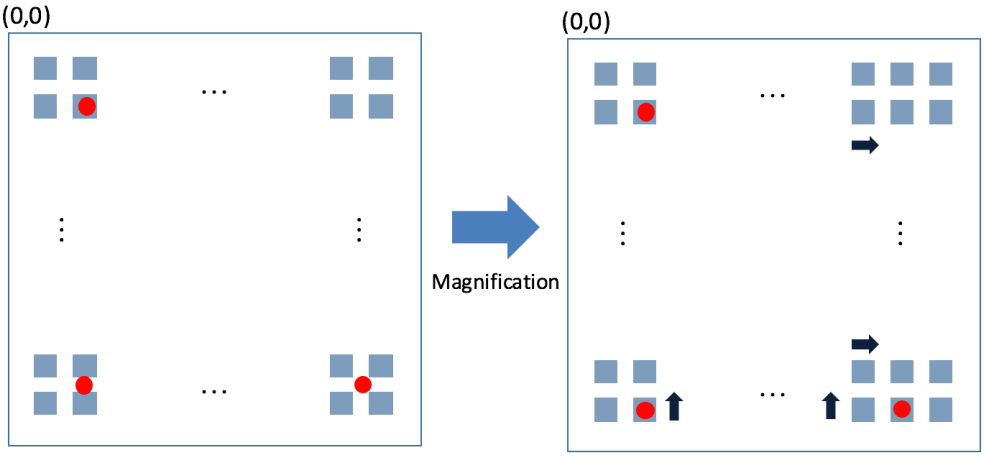

Figure 2.5: Both axes relevant example – asymmetric magnification

2.2.2. Second Order deformation

The concept of high-order deformation was suggested by Jonckheere as a form of intentional pattern deformation [18]. Second-order deformation is part of pattern deformation where the mask pattern is deformed in a bow shape as shown in Figure 2.6. In second order deformation in x axis, absorber pattern coordinates are translated from (x, y) to $(mag_x \cdot x + b \cdot y^2,\ mag_y \cdot y)$, where b is a constant.

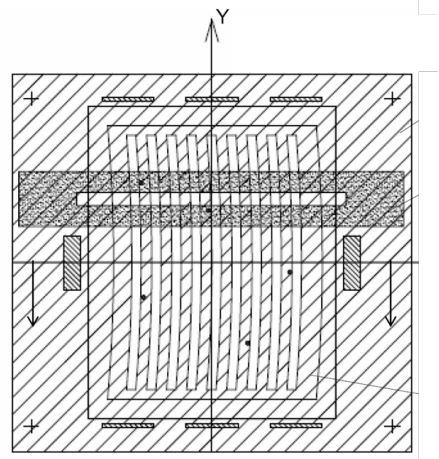

Figure 2.6: Example of intentional pattern deformation. The mask pattern in the field area, here containing vertical lines and spaces, is deformed by a bow as example of non-linear deformation.[18]

As demonstrated in previous figures, spacing of defects can be a limiting factor in pattern shift. Figure 2.7 shows an example where second order deformation can benefit defect avoidance by altering the absorber pattern's locations.

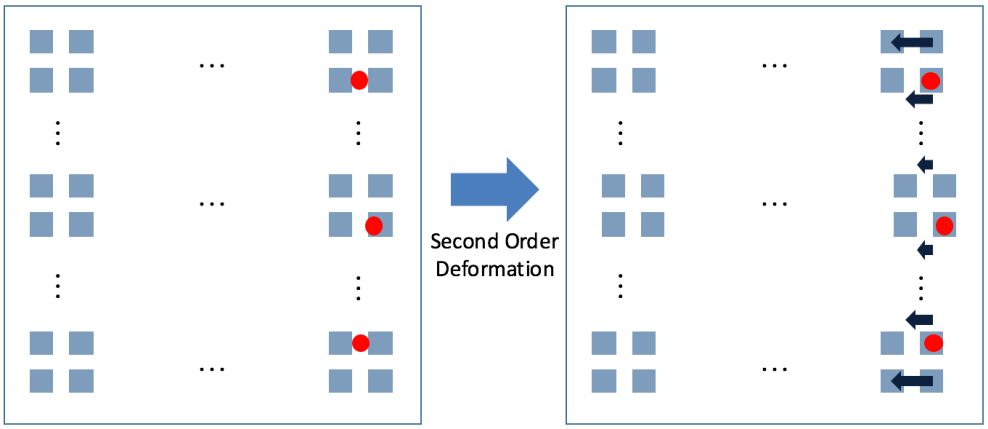

Figure 2.7: Example showing the benefits of second order deformation for defect avoidance

CHAPTER 3

Constraint Programming Method

As mentioned in Chapter 1.2, Zhang et al. modeled defect avoidance using prohibited region of the absorber pattern [13]. This methodology creates a geometric map of locations where the defects cannot be placed, then the map is combine to formulate the minimum rectangle overlapping problem which can efficiently compute for available shift for all defects. While this method is efficient in computing pattern shift, it cannot accommodate for pattern deformation as part of its degree of freedom. Thus, we need a novel approach which considers pattern deformation as well. In this Chapter, we propose a constraint programming based method to consider the added degree of freedom and explore its benefits.

3.1. Constraint Programming Method Problem Formulation

3.1.1. Modeling Pattern Deformation as Shift in Defect Location

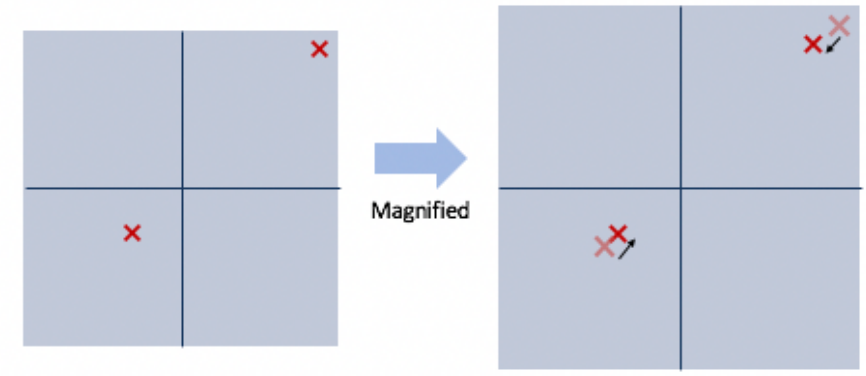

Figure 3.1: Modeling magnification as shift in relative defect locations to absorber pattern

Figure 3.1 shows how positive magnification of the absorber pattern can be seen as a shift in relative defect locations toward the origin. The relative shift is in opposite orientation to the magnification, thus the shift is modeled as an inverse of magnification to defect locations. New defect location can be written as $(\alpha_x \cdot x_{dn},\ \alpha_y \cdot y_{dn})$ where $(x_{dn},\ y_{dn})$ is the location of the original nth defect, and (α_x, α_y) is the inverse of $(mag_x,\ mag_y)$.

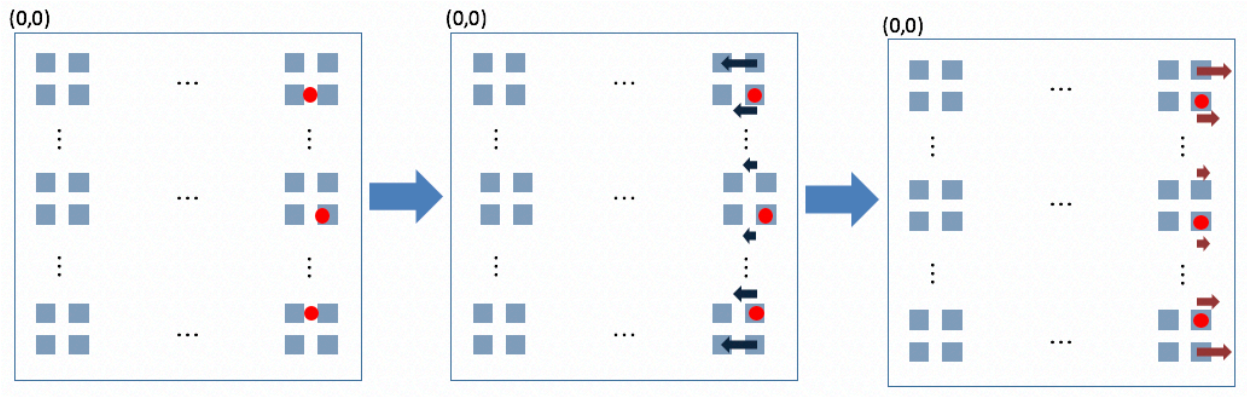

Figure 3.2: Modeling second order deformation as shift in relative defect location to absorber pattern

The same idea can be applied to second order deformation. The new relative location of the defect to absorber pattern is modeled as shift in the opposite direction of the second order deformation as shown in Figure 3.2. The new defect location can be written as $(x_{dn} - \beta_x \cdot y_{dn}^2, y_{dn} - \beta_y \cdot x_{dn}^2)$ where β is the second order deformation constant.

3.1.2 Assumptions in the Constraint Programming Method

Magnification has two impacts on the absorber patterns – it changes the location of each polygon and magnifies the size of each polygon (shown in Figure 3.3). However, only the change in locations is taken into consideration in our problem formulation. An assumption is made that the magnification does not affect the size of the polygons.

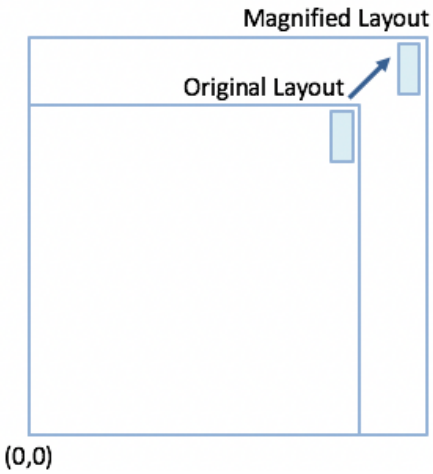

Figure 3.3: Impact of magnification on the absorber patterns

This assumption is valid for a very small magnification value. For instance, each polysilicon polygon in ARM Cortex M0 has width of 300 dbu (=30nm) and length of 15,000 dbu (=1500nm). We use 0.1% magnification to enlarge each polygon size to 300 × 15002 dbu. The width does not change as they round down to the nearest integer with small magnification value. Length changes by 2 dbu, however, this is acceptable as the difference in value is less within the safety margin (=20nm) of our prohibited region calculation. To confirm that our assumption was valid, we used prohibited region method as discussed in Chapter 1.2 implemented with C++ using OpenAccess [19] and Boost Polygon [20] to magnify the design and verify the results from both methods were identical.

3.1.3 Problem Formulation

We formulate a constraint programming based model for our defect avoidance for EUV mask defects. Our framework takes inputs of defect location, prohibited regions, and ranges of allowed degree of freedom. Then, returns the maximum number of mitigated defects and corresponding degrees of freedom values. In the following, we use notations as described in Table 1.

Table 1: Notations

Notation	Meaning
$\alpha_x(\alpha_y)$	inverse of magnification in x (y) directions
$\beta_x(\beta_y)$	second order constant x (y) direction
$d_x(d_y)$	pattern shift in x (y)direction
θ	small angle rotation
$x(y)_{dn}$	x (y)coordinate of nth defect
$x(y)_{min,n}$ $x(y)_{max,n}$	minimum and maximum x (y) coordinate of prohibited regions for nth defect
$x(y)_{rot}$	x (y) coordinate of rotated defect location
$new\_x(y)_{dn}$	x (y) coordinate of new defect location

Find $\{\alpha_x, \alpha_y, d_x, d_y, \beta_x, \beta_y, \theta\}$ (1)

s.t. $\frac{1}{mag_{max}} \leq a_{x,y} \leq \frac{1}{mag_{min}}$ (2)

$shift_{min} \leq d_{x,y} \leq shift_{max}$ (3)

$\beta_{min} \leq \beta_{x,y} \leq \beta_{max}$ (4)

$\theta_{min} \leq \theta \leq \theta_{max}$ (5)

$\sum_n x_{min,n} \leq new\_x_{dn} \leq x_{max,n}$ & $y_{min,n} \leq new\_y_{dn} \leq y_{max,n} = 0$ (6)

Equations (1) through (6) define the model. The objective function (1) represents the finding degrees of freedom for defect avoidance. Constraint (2), (3), (4), and (5) defines the range of allowed degree of freedom. Constraint (6) defines the illegal solution space for new defect locations. The rotated and new defect location is written as following:

$$(new\_x_{dn},\ new\_y_{dn}) = (\alpha_x x_{rot} - \beta_x y_{rot}^2 - d_x,\ \alpha_y y_{rot} - \beta_y x_{rot}^2 - d_y) \quad (7)$$

$$(x_{rot},\ y_{rot}) = (x_{dn}(1 - \frac{\theta^2}{2}) - y_{dn}\theta,\ \ y_{dn}(1 - \frac{\theta^2}{2}) - x_{dn}\theta) \quad (8)$$

Figure 3.3 demonstrates illegal (prohibited region) and legal solution space for a defect. Each illegal solution space (denoted as ① and ② in Figure 3.3) is added to the model as described in constraint (6) which prohibits the new defect location to be placed in such space.

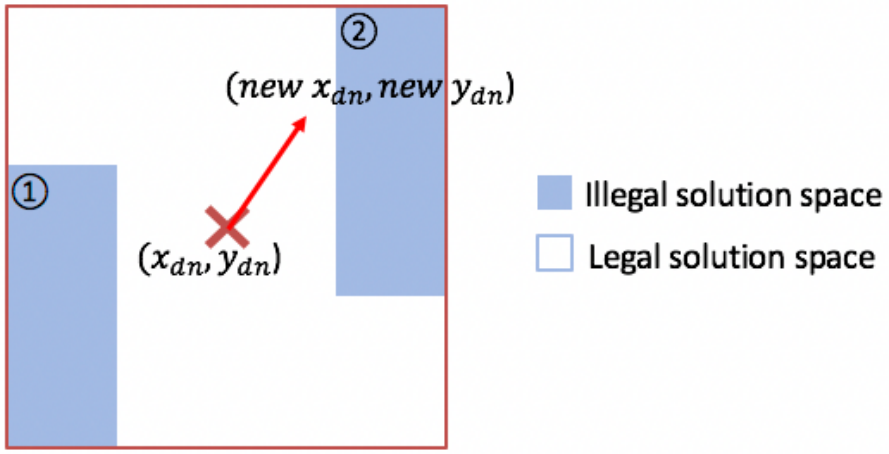

Figure 3.3: Example of defect location and its surrounding solution space

Our proposed method returns the maximum number of defects covered by the given degrees of freedom and solution space. This is achieved by returning the number of defects when the model becomes infeasible to solve. Since the constraint for each defect is added in the order of the data written in the program, the number of mitigated defects are order dependent. However, this dependency is acceptable since imec_n7 defect map was ordered from high priority to low priority. For ARM Cortex M0, 100 defect maps were randomly generated for Monte Carlo analysis which are further discussed in Chapter 3.4.

3.2 Working Example

A working example of how magnification is computed is shown in this section. Figure 3.4. shows a simple prohibited region and two defects. Solution space bounded by the allowed shift for each defect is retrieved and combined to find the final solution space. As shown, there is no solution available for this example using pattern shift.

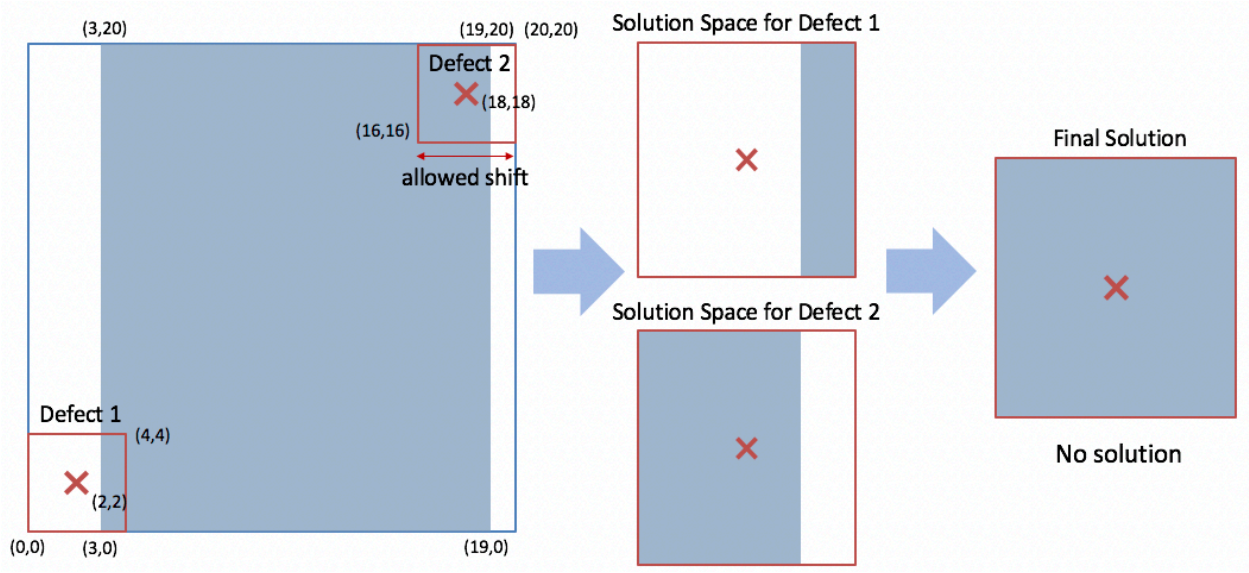

Figure 3.4: Example of defect avoidance using pattern shift

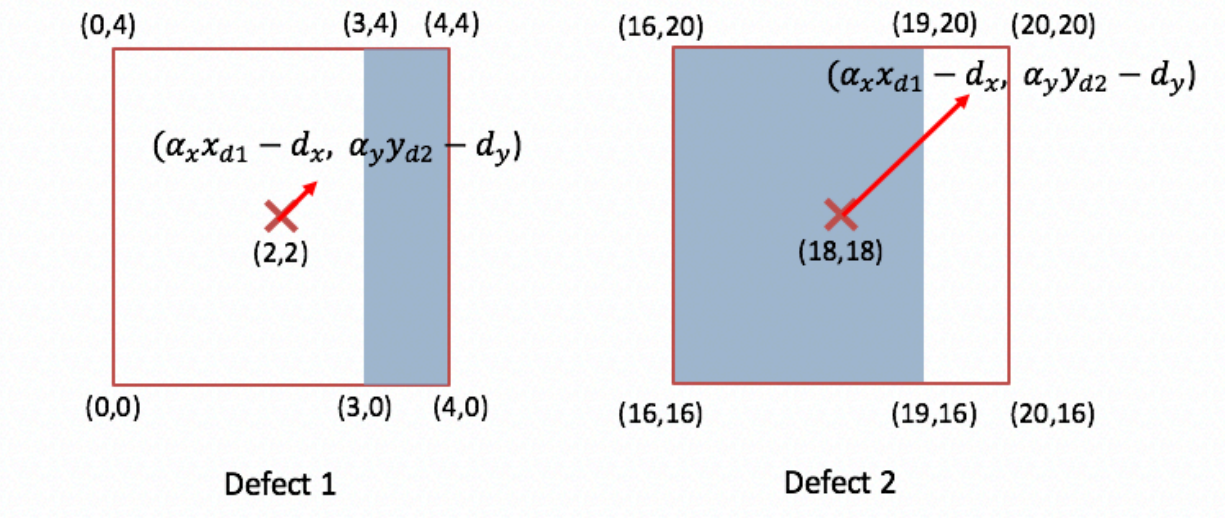

Figure 3.5: Computing new defect location using proposed constraint programming method

Using our proposed constraint programming method, we can model pattern shift and magnification as displacement in defect as shown in Figure 3.5. Then, we can construct our constraint programming model with the following parameters:

Find $\{\alpha_x, \alpha_y, d_x, d_y\}$ (9)

s.t. $\frac{1}{mag_{max}} \leq a_{x,y} \leq \frac{1}{mag_{min}}$ (10)

$shift_{min} \leq d_{x,y} \leq shift_{max}$ (11)

$x_{min,1} \leq \alpha_x x_{d1} - d_x \leq x_{max,1}$ & $y_{min,1} \leq \alpha_y y_{d1} - d_y \leq y_{max,1} = 0$ (12)

$x_{min,2} \leq \alpha_x x_{d2} - d_x \leq x_{max,2}$ & $y_{min,2} \leq \alpha_y y_{d2} - d_y \leq y_{max,2} = 0$ (13)

Objective (9) defines the parameters to fine. Constraint (10) and (11) defines the allowed degree of freedom, and constraint (12) and (13) defines the illegal solution space for the parameters. When values are substituted, the constraints look as following:

Find $\{\alpha_x, \alpha_y, d_x, d_y\}$ (14)

s.t. $-2 \leq d_{x,y} \leq 2$ (13)

$\frac{1}{1.10} \leq a_{x,y} \leq \frac{1}{0.90}$ (14)

$3 \leq \alpha_x 2 - d_x \leq 4$ & $16 \leq \alpha_y 2 - d_y \leq 19 = 0$ (15)

$16 \leq \alpha_x 18 - d_x \leq 19$ & $16 \leq \alpha_y 18 - d_y \leq 20 = 0$ (16)

Through our framework, maximum number of mitigated defect is 2 in this example and provides corresponding degrees of freedom. An example of possible solution is $a_x = 1.075$, $a_y = 1.075$ $d_x = 0$, $d_y = 0$. We can verify that this is a valid solution by applying the magnification values to the pattern and combining the solution space. As shown in Figure 3.6., we can verify magnification of 0.93 (-7% magnification) is a valid value for a successful defect avoidance in this example.

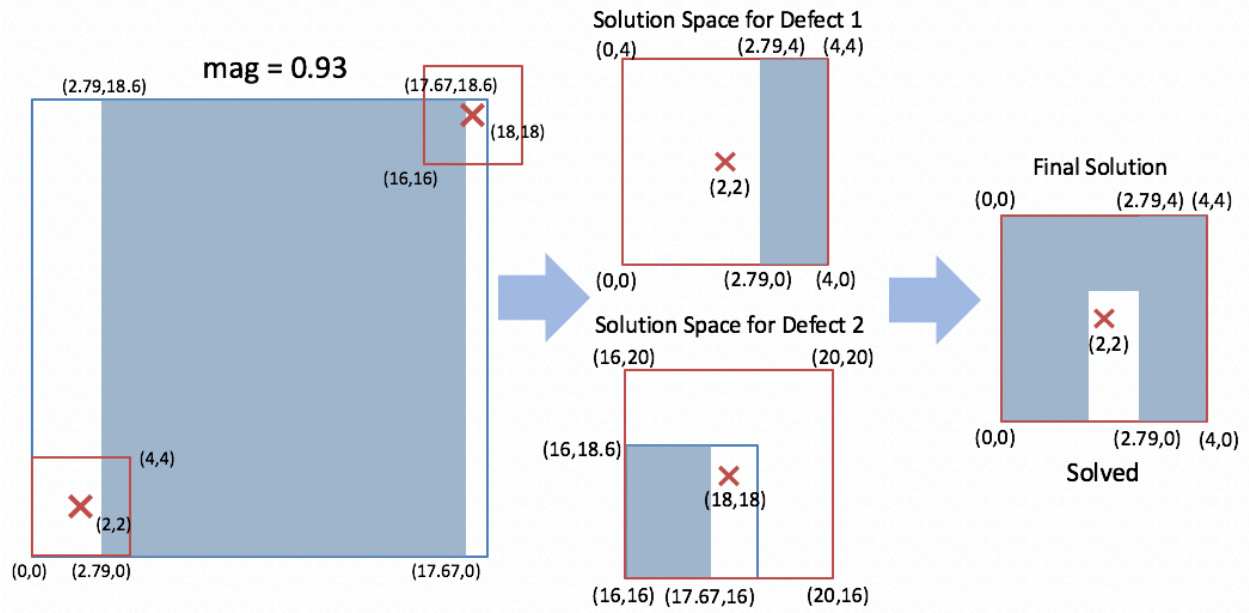

Figure 3.6: Example of defect avoidance using pattern shift and magnification

3.3 Experimental Setup

Our proposed constraint programming based EUV mask defect avoidance method has been implemented in Python using Decision Optimization CPLEX API developed by IBM [21]. We chose to use constraint programming as our method of choice because it is efficient in handling logical constraints and it allows us to explore all solution spaces (unlike other mathematical programming methods where object function is needed). Our solutions from constraint programming method were validated using prohibited region to ensure the assumptions made in our methods were valid. To do so, we implemented prohibited region method in C++ using OpenAccess and Boost Polygon API. OpenAccess was used to read and deform the layout shapes, then Boost Polygon API was used to perform polygon Boolean operations.

We used ARM Cortex M0 processor layout and a 7nm technology node inspired test design provided by our industry partner Rik Jonckheere from imec (referred to as imec_n7). ARM Cortex M0 was synthesized, placed and routed using Cadence Encounter with 32 nm Synopsys Standard Cell Library [22]. The layout was then scaled to an 8nm technology node for our experiment. ARM Cortex M0 layout is 162 × 159 μm^2 and imec_n7 layout is 152 × 152 μm^2. Note that these die sizes are much smaller than the full-field size of masks. The defect density reported in our results may

not represent the realistic values in production. Nonetheless, the analysis is sufficient to evaluate the effectiveness of our proposed method.

On the ARM Cortex M0 design, Monte Carlo analysis over 100 random defect map was performed to determine the effectiveness of our method. 100 random spatial defect maps were generated to test our method and it was assumed that the defects were distributed uniformly across the mask. Each map consisted of 50 defects and our constraint programming method returned the maximum number of defects that could be avoided. Mask yield shown in the results are percentage of defect maps that are made usable (no impact on chip yield) through defect avoidance. On imec_n7 design, we used a defect map of 57 defect count provided by our industry partner. Number of mitigated defects are listed as result of our methodology for this design.

In creating the prohibited rectangles, we set the "safety margin" to be 20nm for all our designs. Safety margin refers to the distance the defect must be placed to not affect the printing on the wafer (noted as d_{in} and d_{out} in Figure 1.5). It accounts for the half-pitch of the defect diameter as well as location uncertainties of the defects. We allow a maximum pattern shift of 20μm, a small-angle rotation of 3° and magnification of 0.1%. Maximum second-order deformation term β is 10 ppb for our designs, as the deformed pattern displacement due to $\beta_x y_{dn}^2$ term should not exceed certain limit.

3.4 Experimental Results

Table 2: Summary of mask yield of ARM Cortex M0 layers using 20μm pattern shift

Defect Count	POLY	M1	ACT	CO
10	100%	100%	100%	100%
20	100%	100%	100%	100%
30	44%	100%	100%	100%
40	5%	100%	100%	100%
50	0%	86%	100%	100%

Table 2 shows mask yield using only pattern shift for four critical layers for EUV. As shown, 20μm pattern shift is a sufficient degree of freedom for defect avoidance for metal 1, active and contact layers. However, 20μm pattern shift is not a sufficient degree of freedom for polysilicon layers which has unidirectional and equally spaced parallel shapes. Thus, the further degree of freedom is necessary for polysilicon layer and is the subject of our study. The following results for ARM Cortex M0 design are for polysilicon layer.

Table 3: Summary of mask yield of ARM Cortex M0 polysilicon layer after using our defect avoidance method

Defect Count	Shift	Shift + rotation	Shift + magnification	Shift + magnification + 2nd order deformation	Shift + rotation +magnification
10	100%	100%	100%	100%	100%
20	100%	100%	100%	100%	100%
30	44%	100%	100%	100%	100%
40	5%	29%	53%	100%	98%
50	0%	0%	9%	51%	26%

Table 3 shows the summary of our mask yield for polysilicon layer on ARM Cortex M0 design. We see a major improvement for yield in 30, 40, 50 defect count maps. While shift can only mitigate 44% of 30 defect count maps, adding another degree of freedom such as rotation and/or magnification allows the yield to become 100%. For 50 defect count maps, combination of magnification and second order deformation was able to achieve 51% compared at 0% yield solely using pattern shift.

This results show us that non-linear degrees of freedom when combined with pattern shift benefit defect avoidance as expected from Chapter 2. This is because defect avoidance by linear degree of freedom, such as pattern shift, is limited by regular and unidirectional polysilicon layer.

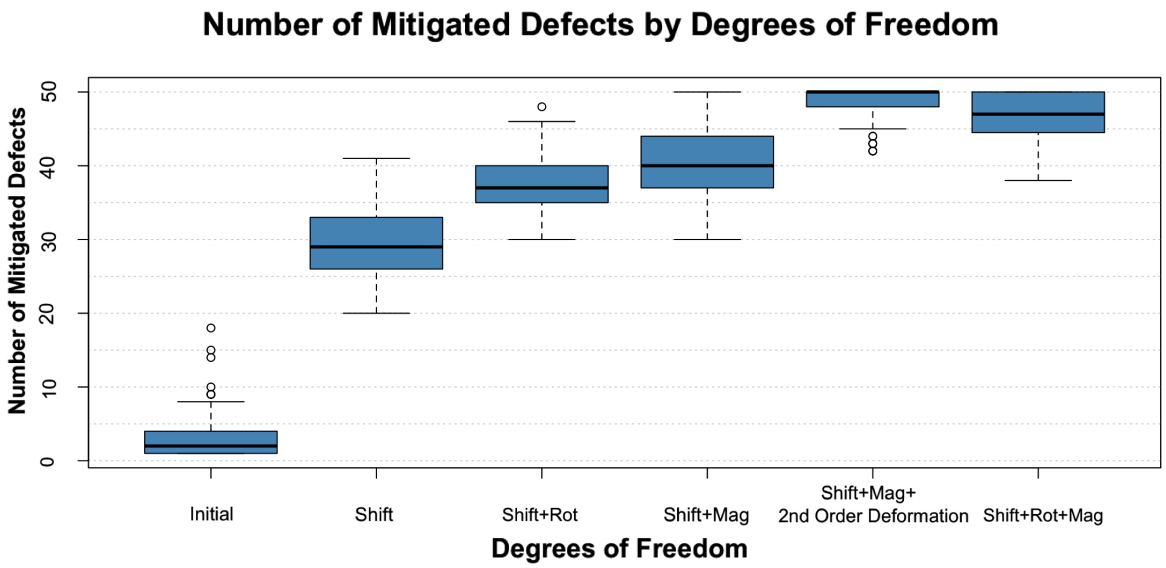

Figure 3.8: Boxplot of number of defects mitigated in polysilicon layer by degrees of freedom

Our constraint programming method returns the maximum number of defects mitigated. Figure 3.8 shows a boxplot of number of mitigated defects in polysilicon layer by degrees of freedom. The results show that combination of shift, magnification and second order deformation is the most effective degree of freedom for the polysilicon layer. It yields the highest number of mitigated defects with the average of 48.4 and median of 50 defects as shown in Table 4. This specific results pertain to the ARM Cortex M0 polysilicon layer and different combinations of degree of freedom may be more suitable for different designs.

Table 4: Average and median number of defects mitigated in polysilicon layer by degrees of freedom

	Initial	Shift	Shift + rotation	Shift + magnification	Shift + magnification + 2nd order deformation	Shift + rotation + magnification
Average	3.3	29.4	37.5	40.5	48.4	46.5
Median	2	29	37	40	50	47

We tested the combination of degrees of freedom on two layers of imec_n7 design – via 1 layer (M20-V1) and metal 2 layer (M30-M2). Table 5 shows the number of mitigated defects from the provided defect map. In via 1 layer, combination of shift, magnification and second order deformation can avoid up to 17 more defects compared to only pattern shift. In metal 2 layer, combination of shift, magnification and rotation gives the best the improvement of 5 more mitigated defects than pattern shift.

Table 5: Number of mitigated defects on imec_n7 design using different degrees of freedom

Degrees of Freedom	M20 – V1	M30 – M2
20u shift	36	10
20u shift + 0.1% mag	44	13
20u shift + 3° rotation	42	13
20u shift + 0.1% mag + 3° rotation	49	15
20u shift + 0.1% mag + 10ppb beta	50	13
20u shift + 0.1% mag + 20ppb beta	53	13

The difference in success for defect avoidance in via 1 and metal 2 comes from the pattern density of the layers. As pattern density increases, absorber area to cover the defect decreases making it harder to find concurrent solution space. Figure 3.9 illustrates the difficulties of defect coverage depending on the pattern densities. As illustrated, metal 2 has a very high pattern density, which even with additional degree of freedom it is difficult to mitigate large number of defects.

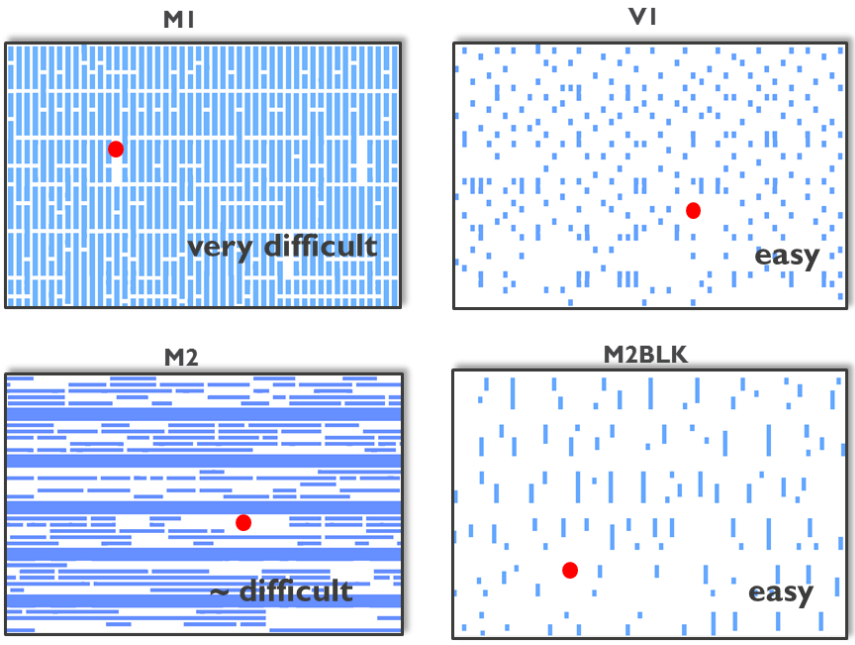

Figure 3.9: Illustration of defect coverage dependency on pattern density. Clear area (reflective ML) is shown in blue, and the white background represents absorber. A red dot represents a ML-defect, that is attempted to be covered by absorber [18].

Chapter 4
Conclusion and Future Work

In this thesis, we proposed an EUV mask defect avoidance method that can explore pattern shift, rotation, and pattern deformation as degrees of freedom. We modeled the degrees of freedom as displacement in relative location of defects and used constraint programming to simultaneously solve for optimal solution. Our methodology is general and additional degrees of freedom may be added to explore a further benefits of defect avoidance.

Using our proposed methodology, we explored the benefits of pattern deformation as an additional degree of freedom to prior studies. Our analysis shows that pattern deformation (magnification and second order deformation) can provide a significant benefit to defect avoidance under right circumstances. For the polysilicon layer of an ARM Cortex M0 layout, pattern deformation combined with pattern shift was able to improve mask yield by more than 90%-point compared to pattern shift alone for a 40-defect mask.

Applicability of the defect avoidance method depends largely upon the ability of lithography tools to handle degrees of freedom. Pattern deformation is especially dependent since scanner operation must be modulated to not reproduce pattern deformation on the wafer. Defect location uncertainty is another major bottleneck to defect avoidance. In this thesis, we assume the defect half-pitch and locational uncertainty is combined to be 20nm which is referred to as safety margin from absorber edges. However, if the locational uncertainty is larger, the expected mask yield may be lower.

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