Design Impacts of Back-End-Of-Line Line Edge Roughness

Eugene Chu, Yandong Luo, and Puneet Gupta

***Abstract*—One of the main issues of EUV lithography is Line Edge Roughness (LER) on photo-resists, which significantly impacts yield at sub-30 nm pitches. In this work, an analytical model of LER is presented and analyzed for yield loss induced by open/short failures, cut mask defects, enhanced time dependent dielectrics breakdown (TDDB) failures for metal wires with different geometries, electro-migration (EM) impacts from the presence of LER on SRAM bitlines, and finally, LER impacts on functional errors. The model will be evaluated on single and double patterned designs with metal pitches of 24 and 28 nanometers. We show experimental results and give specific criteria in which LER thresholds can be relaxed without negatively impacting yield and path delay. This is a critical issue as higher LER tolerance allows exponential increase in throughput and thus reduces cost of fabrication.**

***Index Terms*—EUV, line edge roughness, yield estimation, cut mask, TDDB, electro-migration, chip area penalty**

I. Introduction

LIGHT source power has long been a critical issue in extreme ultraviolet (EUV) lithography, and requires photo-resists (PR) with high sensitivity to meet the demands for adequate throughput. Higher sensitivity in PR commonly leads to higher line edge roughness (LER), which stems from the random distribution of soluble and insoluble chemicals at the boundary of patterned features, caused by the stochastic nature of the polymer deprotection process [1]. Past research [2] has shown several other features of EUV lithography that may also contribute to increases in LER: 1) Photons with higher energy excite secondary electrons during exposure. 2) Reduced light source power leads to limited exposures, which add to the stochastic behavior of photons. 3) LER transferred from EUV Mask roughness. This currently constrains the throughput of EUV processes, as the limited light intensity requires prolonged exposure time to mitigate LER, as shown in Fig. 1 [3].

Currently, industrial processes manufacture metal layers with multiple patterning technology in 193 nm-immersion lithography. The Taiwan Semiconductor Manufacturing Company (TSMC) has announced the volume production of 7 nm nodes with EUV within the year, which feature less exposure steps and fewer restrictions in layout design compared to previous 193 nm design processes. Fig. 2(a) and Fig. 2(b) show that for future EUV lithography, single patterning and litho-etch litho-etch (LELE) patterning are two potential candidates

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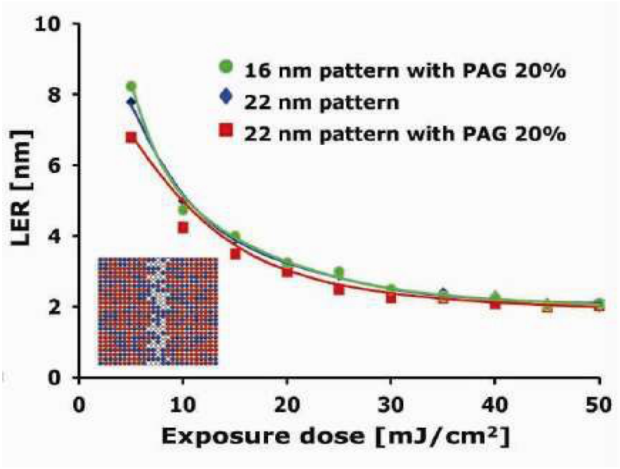

Fig. 1. Trade-off between LER magnitude and exposure dose. Source: Adapted from [3]

[3]. As resolution limits for EUV originates from stochastic effects such as LER, LELE for EUV may be required for 20 nm line-widths due to larger defectivity at such pitches.

As LER does not scale down accordingly with along interconnect pitch, designs with sub-30 nm pitches can be observed having undesirable protrusions or indentations at wire edges that may cause catastrophic yield loss and interconnect performance and lifetime variability. Fig. 2(c) shows two possible failures due to LER: 1) protrusions at two neighboring wire edges can connect and cause short circuits, which can be exacerbated by the overlay shift in LELE patterning. 2) LER at the two edges of an interconnect segment may also cutoff the interconnect and cause open circuit, resulting in errors. All of these issues can lead to catastrophic chip malfunction and increase yield loss. Furthermore, issues such as time dependent dielectric breakdown (TDDB) of interconnects and electro-migration (EM) failures heavily impact chip lifetime, which can also be further aggravated due to LER and overlay. In this paper, we first utilize an analytical based model for estimation of LER, which is then applied for simulation of induced metal wire shorts/opens failures for different process parameters, TDDB and EM lifetime variability.

Critical area based analyses have been widely used to calculate yield loss induced by photo-lithographic defects [4], where defects are typically modeled as circular areas with various sizes. However, in this paper, yield is modeled based on statistical characteristics of LER. We also model critical path delay variability due to LER with Elmore's delay model

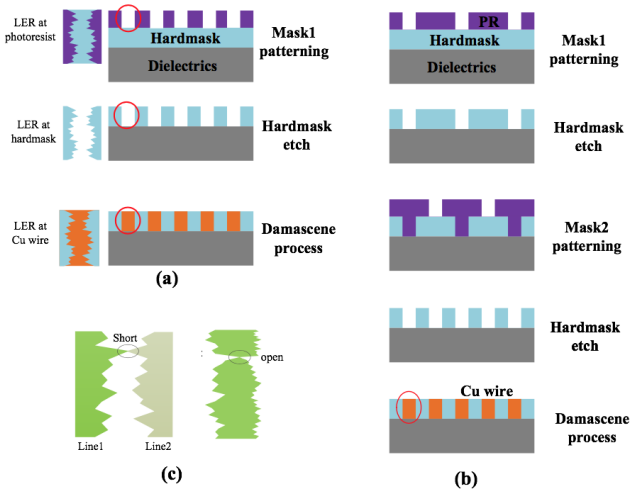

Fig. 2. (a) single patterning by EUV. (b) litho-etch litho-etch patterning by EUV. (c) An illustration of LER induced wire shorts and opens.

[5] on single patterning designs. In this paper, both area and path delay of EUV metal wire patterning at 24 nm and 28 nm pitch are calculated, and the possibility of relaxing LER requirements while maintaining high yield with low path delay variability is explored.

II. Modeling of LER Induced Failures

In this section, we determine a stochastic model that represents the correlated variation of both magnitude and direction of LER. The model is then utilized to simulate problems that may be exacerbated by LER, including several process parameters, reliability issues, and chip-level metrics.

A common way to generate wire geometry with LER is to conduct inverse Fourier transform from its power spectral density (PSD) with random phases, which is typically described by a Gaussian or exponential auto-correlation function [6]. However, this method leads to heavy computational burdens for chip level estimations. In this section, a simple analytical approach is proposed, which can be applied to calculate the yield of a metal layer.

Fig. 3 shows LER along a wire with sample intervals of 1 nm [6]. LER1 = $(x_{11}, x_{12}, ..., x_{1i}, ..., x_{1N})$, and LER2 = $(x_{21}, x_{22}, ..., x_{2i}, ..., x_{2N})$ indicate the LER variation along the two wire edges, which are defined as the deviation of the actual wire edge from its baseline position (shown as the dashed line). Each segment along the wire is modeled as a spatially correlated Gaussian random variable with $N(0, \sigma_{LER})$ and co-variance shown in (1). λ denotes the correlation length, which is typically 10-50 nm [7]. The metal wire is assumed to inherit the exact LER geometry from the photo-resist without variations from effects such as blurring or shadowing. Wire tapering in the vertical direction and wire thickness variation is not considered.

$$cov(x_{ki}, x_{kj}) = \sigma_{LER}^2 e^{\frac{-[(i-j)]^2}{\lambda^2}}, \quad (1)$$

where $k \in \{1, 2\}$, and $1 \leq i, j \leq N$.

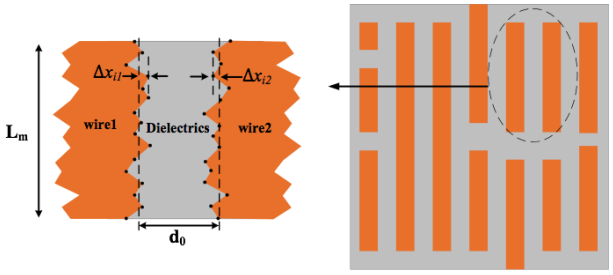

Fig. 3. An illustration of the LER model in this study.

The local wire space at point i can be expressed as $d_i = d_0 - X_i$, where $X_i = x_{1i} + x_{2i}$ is of normal distribution $N(0, \sqrt{2}\sigma_{LER})$ and d_0 is the nominal wire space without LER. The spatial correlation of X can be expressed as (2). As the metal edges on opposite sides of the spacing are not spatially correlated, we can calculate the LER of the two sides separately.

$$\begin{aligned} cov(X_i, X_j) &= cov(x_{1i} + x_{2i}, x_{1j} + x_{2j}) \\ &= cov(x_{1i}, x_{2i}) + cov(x_{1j} + x_{2j}) \\ &= (\sqrt{2}\sigma_{LER})^2 e^{\frac{-[(i-j)]^2}{\lambda^2}}, \end{aligned} \quad (2)$$

Equation (3) shows the probability density function of $x = [X_1, X_2, X_3, ..., X_N]^T$, which is a Nth-dimension Gaussian distribution. $u = [u_1, u_2, u_3, ..., u_n]^T$ denotes the vector of mean values of shift due to overlay. Σ is a $N \times N$ positive definite co-variance matrix with $\Sigma_{ij} = cov(X_i, X_j)$. We calculate the cumulative probability distribution of x with the mvtnorm package in the statistics software language R [8] to model the probability of open/short failures due to LER. In this study, the dimensionality of the random variables longer than 1 µm is reduced by segmentation of wires into sections that are serially connected.

$$f(x) = \frac{e^{-\frac{1}{2}(x-u)^T \Sigma^{-1}(x-u)}}{\sqrt{(2\pi)^N det(\Sigma)}}, \quad (3)$$

A. Open/Short catastrophic failures

The design will short circuit if at any point k, the LER protrusions exceed the spacing between wires, i.e. $X_k > d_0$. Equation (4) expresses the short probability for metal wires with length L_N.

$$P(short, L_N) = 1 - P(X_1 < d_0, ..., X_N < d_0), \quad (4)$$

Similarly, the probability that a wire of length L_N gets open circuited can thus be expressed as (5). w_0 is the nominal wire width without LER. $Y_i = y_{1i} + y_{2i}$, where y_{1i}, y_{2i} are the LER magnitudes at the two edges of a wire.

$$P(open, L_N) = 1 - P(Y_1 < w_0, ..., Y_N < w_0), \quad (5)$$

In LELE patterning, overlay errors shift wires by u_i and the vector of means $u = [u_i, u_i, ..., u_i]^T$. Therefore, the short

probability is expressed as (6), where the short probability under each overlay shift u_i is evaluated. u_i is assumed to obey normal distribution $N(0, \sigma_{overlay})$, where $\sigma_{overlay}$ is the standard deviation of the overlay shift. The open probability is not affected by overlay error.

$$P(short, L_N) = 1 - \sum_{i=1}^{m} P(X_1 < d_0, ..., X_N < d_0 | u = u_i) P(u = u_i), \quad (6)$$

The short probability for a metal layer is calculated by considering metal wires of all the possible lengths in the layer, as shown in (7). N_{wire} denotes the total number of wires in a metal layer. The open probability in a metal layer can be calculated in a similar way.

$$P(short) = 1 - \prod_{m=1}^{N_{wire}} (1 - P(short, L_m)), \quad (7)$$

B. Time Dependent Dielectrics Breakdown

LER in wires potentially affect the reliability of the dielectric materials by locally enhancing the electric field generated by a voltage difference between adjacent wires. Ideally, two adjacent interconnect wires have parallel sidewall surfaces, which define a constant spacing and therefore constant electrical field along the entire wire length. With LER, notches and protrusions cause spatially correlated variations within the electric field, which increases the chance of conductive paths forming in the dielectrics between interconnects [9]–[15]. However, limited work has been conducted on TDDB due to LER impacts in local line-to-line spacing variations [10]. In this section, a LER-aware TDDB model is proposed and studied.

The probability for TDDB occurring before time t in low-k dielectrics is assumed that the time-to-breakdown t_{BD} obeys the Weibull distribution [12], [13]. However, past research [7], [16], [17] models TDDB without considering effects such as non-homogeneous electrical fields and spatially non-uniform charge percolation. These complex effects induce non-linear changes in critical weibull parameters such as t63, the weibull shape factor β, and the field acceleration factor γ. In our paper, we consider a Root-E (RE) model for the underlying acceleration model with respect to the electrical field, as well as a percolation model for β that assumes that the required critical defect density for TDDB decreases with separation. The models are presented in (8) and (9), where $A_{RE} = 7.06 \times 10^{19}$, $\gamma_{RE} = 45.96 (nm/V)^{0.5}$, E is the electric field calculated assuming uniform distance for each segment, and d_i denotes the segment spacing in nm.

$$t63 = A_{RE} e^{-\gamma_{RE}\sqrt{E}}, \quad (8)$$

$$\beta = \frac{d_i - 5.803}{10.24}, \quad (9)$$

Fig. 4 shows that in the presence of LER, the electric field intensity is not constant along the metal wire due to variations in geometry. With segmentation, the probability that an segment i, fails in time interval $(t, t+\Delta t)$ is given by (10), which is derived from the elemental weibull distribution. The chip TDDB failure probability before a certain time t can then be estimated by (11), where it is assumed that the dielectric fails as long as breakdown is observed in one segment. N is the total number of the dielectric segments in a metal layer that are electrically stressed, and T is set to 5 years. Furthermore, we reduce the pessimism of TDDB lifetime estimation with a signal-aware TDDB model, where we assume a duty cycle α defined as the fraction of the time when a pair of interconnects have opposite logic signals [18]–[20].

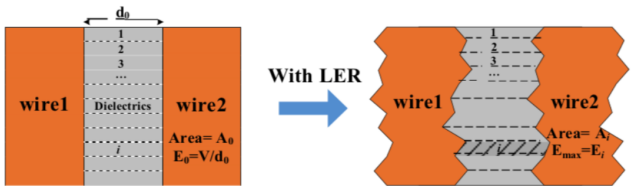

Fig. 4. The model for calculating TDDB failure with segmentation.

$$h_i(t)\Delta t = \frac{\beta_i}{t} \left(\frac{\alpha t}{t63_i}\right)^{\beta_i} \Delta t \quad (10)$$

$$F(t) = 1 - \prod_{i=1}^{N} \left(1 - \int_0^T h_i(t) dt\right), \quad (11)$$

C. Electro-Migration failures in SRAM

Electro-migration (EM) induced interconnect degradation is gaining importance in power semiconductor devices and memory arrays as the technology node shrinks down. As the current density within copper wires increases along with metal pitch, increased LER in EUV lithography induces both functional failures from path delay and EM failures from void stress. Past research [21], [22] shows that process variation in sub-30 nm technology nodes results in less than 3% delay variation, while predicted lifetime is drastically decreased due to EM failures, and the reduction of pitch size further diminishes the lifetime of the circuit. As such, we model SRAM bitlines for 7 nm technology nodes as multi-segment interconnects with voltage input/output and current source ports represented by inter-layer vias and contacts. We use a physics-based analytical model to calculate the mean-time-to-failure (MTTF) of bitlines due to stress distribution within the confined metal line caused by the current [23].

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \frac{D_a B \Omega}{k_B T} \left(\frac{eZ\rho j}{\Omega} + \frac{\partial \sigma}{\partial x}\right), \quad (12)$$

Equation (12) is the well-known Korhonen's equation for stress evolution due to applied current [23]. A solution for void nucleation time can be approximated by the method of separation of variables into (13), where L is the segment length, k_B is the boltzmann constant, T is the temperature, D_a is the atomic diffusivity, B is the bulk elasticity modulus, Ω is the atomic volume, eZ is the effective charge, j is the current

density, ρ is the wire resistivity, and σ_T is the preexisting stress [18].

$$t_{nuc} \approx \frac{L^2 k_B T}{2 D_a B \Omega} ln\left\{\frac{\frac{eZ\rho jL}{2\Omega}}{\sigma_T + \frac{eZ\rho jL}{2\Omega} - \sigma_{crit}}\right\}, \quad (13)$$

After void nucleation, the void growth stage involving atom migration begins line resistance degradation [24]. We designate the time required for full void saturation, where current is forced to flow through the high resistivity side barriers, as the time-to-failure for bitlines. The TTF equation is shown in (14).

$$t_{VS} = t_{nuc} + \frac{k_B T L^2}{2B\Omega D_a} \cdot \left(1 + \frac{2\sigma_T \Omega}{eZ\rho j_0 L}\right), \quad (14)$$

D. LER induced critical path delay variability

LER within manufacturing processes induces variation in interconnect geometry, which may lead to larger delay by both changes in resistance and capacitance [25], [26]. As process variations do not proportionally shrink along with feature size, LER has far graver impacts on sub-7 nm nodes compared to previous works on 22 nm nodes [21], [22]. The deviation of both clock path and signal path delays from its designed value may lead to timing errors, thus causing functional errors and lowering yield [27].

We use Elmore's delay model to model critical path delay, where an interconnect wire delay is dependent on resistors and capacitors. The capacitance can be calculated with (15) [28]. As Cu resistivity increases with higher impact of grain boundary and surface scattering in narrow trenches, we model the impacts of stochastic process variations on mean free path with a semi-empirical model which considers effects including mobility reduction, grain size, boundary scattering, and surface scattering (16). We can then derive the local cross-section resistivity by the integral of (16). $\rho_b = 32.05$, $\rho_q = 82$, and $\lambda = 3.75$ are the three model fitting parameters [29], L is the length of the wire segment set to 1 nm, W is the wire width accounting for LER, T is the thickness of the wire, which is constant across a technology node. H is the vertical distance between ground and the wire segment, and S is the distance between two parallel wires accounting for LER variations. The tapering angle for wires is not considered. The signal delay of a certain path can then be modelled as $D = RC$, and we model path resistance and capacitance via segmentation: the total R, C values of a path is the equivalent of multiple wire segments of length 1 nm in series. Each wire path is extracted and modelled for its R, C values by calculating the worst case scenario where both resistance and capacitance are chosen separately for a certain $3\sigma_{LER}$. We then back-annotate the Standard Parasitic Exchange Format (SPEF) files and run static timing analysis on designs to calculate slack, where the cutoff for acceptable delay threshold is chosen at zero.

$$\frac{C}{E_{ox}} = 1.15\left(\frac{W}{H}\right) + 2.80\left(\frac{T}{H}\right)^{0.222} + 2\left[0.03\left(\frac{W}{H}\right) + 0.83\left(\frac{T}{H}\right) - 0.07\left(\frac{W}{H}\right)^{0.222}\right]\left(\frac{W}{H}\right)^{-1.34}, \quad (15)$$

$$\rho[y,z] = \rho_b + \rho_q\left(\frac{Cosh[\frac{y}{\lambda_q}]}{Cosh[\frac{W}{2\lambda_q}]} + \frac{Cosh[\frac{z}{\lambda_q}]}{Cosh[\frac{T}{2\lambda_q}]}\right), \quad (16)$$

III. Experimental results

In this section, we quantify the models in the previous section and present several possible design rule relaxations for LER that may increase throughput. We also show the impacts of LER on time-dependent functional issues such as TDDB and EM for sub-30 nm interconnect pitches, and look into chip level metrics including critical path delay for varying LER values and chip area penalty analysis on differing LER for trade-off between area and yield. We use 24 nm as default metal pitch for designs.

A. Effect of design on LER yield tolerance

An 1D metal pattern on a 1 cm^2 chip is used as baseline comparison for two open-core designs for yield estimation with respect to LER: an Advanced Encryption Standard cipher chip (AES), and a low power, small area Arm processor (CORTEXM0DS), which are both enlarged for fair comparison. The designs are as shown in Fig. 5(a), Fig. 5(b), and Fig. 5(c). We determine the process tolerance of LER as the $3\sigma_{LER}$ value that reduces chip yield to below 99%. Fig. 6(a) shows the yield of 24 nm pitch wires patterned as parallel wires. It can be seen that for 1D parallel metal patterning with minimum 24 nm pitch, the yield becomes intolerable around $3\sigma_{LER}$ = 3.4 nm, with a sharp transition down to 0% yield at $3\sigma_{LER}$ = 3.8 nm. This indicates that the design is very sensitive to $3\sigma_{LER}$ after the yield threshold. It is also recognized that the sharp transition is slightly delayed when choosing a longer correlation length λ in the model. However, as the defined yield tolerance threshold is not noticeably changed by λ, we accept λ = 20 nm for the rest of the paper.

Fig. 6(b) and Fig. 6(c) present the yield of two designs under different overlays of $3\sigma_{LER}$. It is shown that yield estimation with 1D metal patterning can be overly pessimistic as actual designs show higher LER tolerance with yield thresholds around $3\sigma_{LER}$ = 4 nm. Realistic designs therefore give at least 0.2 nm extra LER tolerance compared to our baseline. This can be attributed to 1D patterning being limited by constant minimum spacing across the entire chip, while physical designs lack such stringent rules in the final layout. Wider spacing thus allows greater LER resilience, and consequently, higher yield. It is also seen that higher metal layers allow larger $3\sigma_{LER}$ values before dropping under the threshold, as the wire density decrease in upper layers effectively increases the pitch size. As such, the total chip yield is constrained by the lower metal layers, and design-dependent optimization may be considered to increase throughput.

B. Impacts of LER on different pitches

In this section, the trade-off between $3\sigma_{LER}$ and pitch size is determined. We choose 24 nm and 28 nm as possible metal pitch sizes for 5 nm technology nodes, and the yield estimates for lower metal layers are shown in Fig. 7(a) and Fig. 7(b). Higher metal layers are ignored as chip yield is typically restrained by lower metal layers. Results show that lowering the pitch decreases LER tolerance, which can be explained due to less width and spacing of wires. It is also evident that if photo-resist manufacturing can be improved with around 0.2 nm reduction in $3\sigma_{LER}$, a 16% decrease in wire pitch is allowed while maintaining yield. Conversely, increasing the tolerance of LER for designs results in an exponential decrease in exposure dose, which translates to an exponential increase in throughput.

C. Impacts of LER on utilization rate

In this section, the effects of different utilization rates during placement on yield are considered. The yield loss for the lowest horizontal metal layer, MINT1, due to LER for three different utilization rates: 70%, 80%, and 90% are observed in Fig. 8. It is shown that lowering utilization rate by 10% gives around 0.2 nm extra tolerance in $3\sigma_{LER}$. The results correspond with increasing the pitch size, as lower utilization rates allow more spacious placement for cells, which in turn gives greater effective spacing for interconnects. However, as the benefits for reducing utilization result in an increase in chip core area, it may not be desirable to adjust utilization during place and route for smaller LER values.

D. Impacts of LER on trim/cut masks

As the technology node scales down to sub-7 nm, small feature resolution is often challenging for optical lithography. Techniques such as self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP) are utilized for line-end cut processes to generate fine metal interconnect patterns from 1D metal layers [30]. Cut masks are then employed to create the desired interconnect patterns. Two main cut mask methodologies exist: 1) End cuts: Cut masks are used to split regular line patterns into multiple wire segments, with some segments used as actual routing and others as dummy wires that serve no function on the final design. The masks in question are produced similar to contact/via masks as they create discrete slits along the 1D metal pattern, as shown in Fig. 9(a). Optimization is performed by shifting and merging neighboring cuts to reduce and normalize the total number of cut shapes on the mask [30]. 2) Block cuts: Cut masks allow convex or concave polygonal cuts across several metal wires, as seen in Fig. 9(b), thus decreasing the amount of dummy wires on the final design. Further optimization can be achieved via minimizing irregularities, whether by lengthening the wires at the expense of performance or running optimizations during the routing stage [31].

However, current cut processes use conventional 193 nm optical lithography, thus suffering from the same resolution limits as the mandrel process. For sub-7 nm nodes, EUV light sources will be necessary to achieve the required resolution. However, LER variations may cause incomplete(shorts) or undesirable(opens) cuts that impact yield. Open/short failures due to LER are therefore a critical issue when fabrication cut processes start to migrate from traditional optical lithography to EUV.

In this section, LER effects are modeled on 1D metal layers subject to SADP, with cut masks set between dummy fill and wires. The layout CORTEXM0-GS is used from Kwangsoo

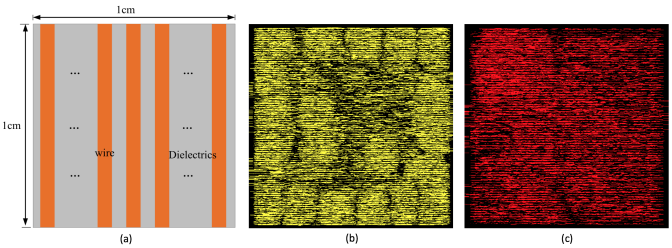

Fig. 5. (a) 1D metal pattern. (b) MINT1 layout for AES. (c) MINT1 layout for CORTEXM0DS.

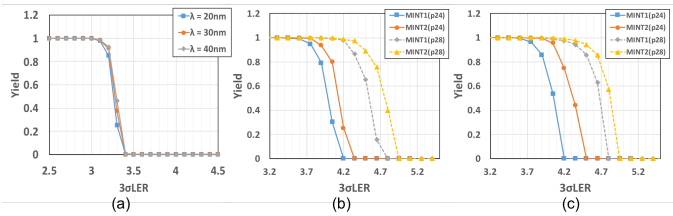

Fig. 6. (a) Yield of 24 nm pitch of 1D wires. (b) Yield of 24 nm pitch of AES. (c) Yield of 24 nm pitch for CORTEXM0DS.

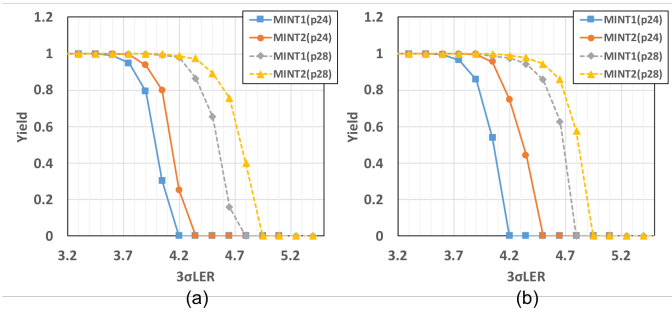

Fig. 7. (a) MINT1, MINT2 yield for AES. (b) MINT1, MINT2 yield for CORTEXM0DS.

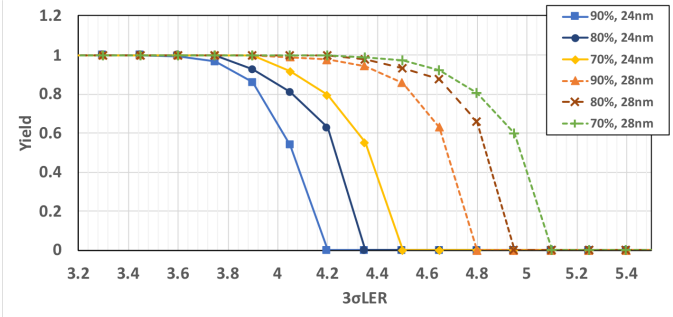

Fig. 8. Yield of CORTEXM0DS MINT1 with differing utilization rates.

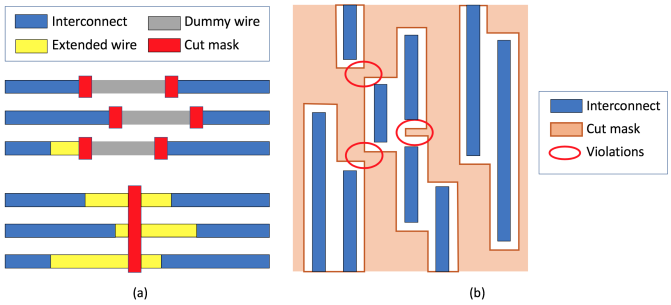

Fig. 9. (a) End cut illustration and optimizations. (b) Block cut illustration and optimizations.

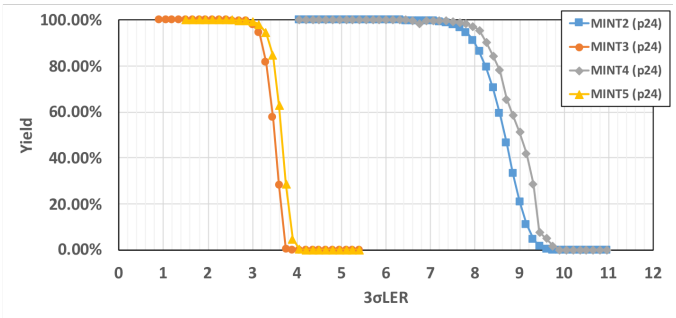

Fig. 10. Yield versus $3\sigma_{LER}$ for 24 nm and 28 nm pitch trim mask design.

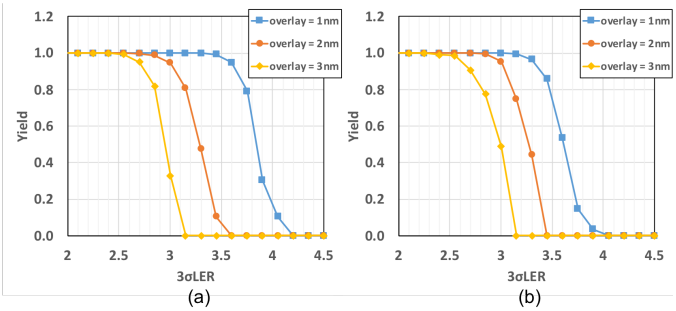

Fig. 11. Yield of (a) AES and (b) CORTEXM0DS MINT1 versus $3\sigma_{LER}$ for varying overlay mismatch

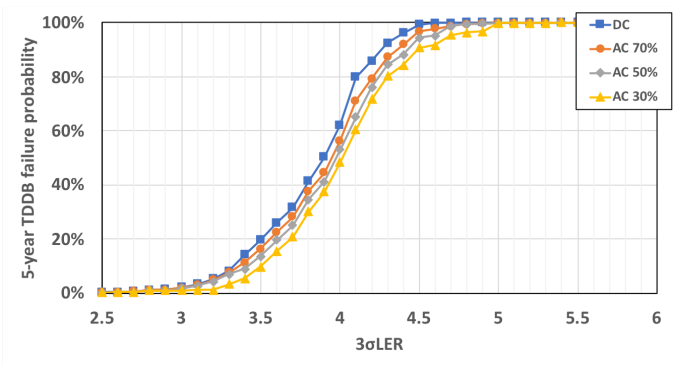

Fig. 12. 5-TDDB failure probability for 24 nm AES MINT1.

Han, et al, UCSD [32], scaled to 24 nm and 28 nm metal pitches. The horizontal metal layers MINT3 and MINT5 are measured to have minimum cut sizes of 7 nm, while the vertical layers MINT2 and MINT4 have minimum cuts sizes of 19 nm. The results in Fig. 10, show noticeably harsher requirements compared to interconnect pitching. One possible method for mitigating LER impact with little increase in chip area is to increase the cut size placed between dummy fills and interconnects, as seen in Fig. 9. From the results, increasing the minimum cut size from 9 nm to 10 nm effectively shifts the yield curve to have comparable yield to the MINT1 open/short yield as seen in Fig. 7, with little increase in chip area. However, designers must take note of overhang margins during this relaxation, as further expansion of cut size may result in DRC violations.

E. Impacts of LER on double patterning

In this section, we model the effects of overlay error for LELE patterning with LER. As the technology node shrinks to sub-7 nm processes, typical overlay budgets are often set to be around 20% to 25% of half pitch [33], thus we model the yield of LELE patterning with overlay variations within the range of 1-3 nm, along with the presence of LER. We model overlay error in double patterning by dividing the layout file into two different masks via alternating tracks, then shift one mask to simulate the effects of overlay mismatch. Fig. 11 presents the modeling results for 24 nm pitch designs with differing overlay values. It is noticed that yield is reduced significantly as the overlay variation increases, which can be attributed to the wire spacing reduction by overlay shift. As a 3 nm shift in overlay drastically reduces LER tolerance by around 1.2 nm, shrinking of the design rules require tight overlay control due to its impact on yield sensitivity. Since EUV suffers from large process variation compared to traditional 193 nm lithography processes, precise overlay management and mitigation is required for further reduction in pitch size.

F. Impacts of LER on TDDB

The 5-year TDDB loss for AES MINT1 is plotted in Fig. 12, where it is observed that there exists a positive correlation between TDDB loss and $3\sigma_{LER}$. It can be seen that despite [19], [20] showing twice the lifetime estimates for 50% duty cycle compared to DC stress, full chip analysis shows similar failure probability for equivalent LER values. This can be explained by the percolation effects on critical defect density, which affects the slope parameter as seen in (9).

As critical defect density for TDDB decreases with separation, segment pairs which have minimal spacing result correspond to a shorter estimated lifetime, which is represented by a small slope factor β. This reduces the duty cycle dependence on the failure probability, and gives smaller changes in TDDB loss than naive estimates. It is also seen that LER drastically worsens the 5-year failure probability, as the chip reaches unacceptable failure estimates at $3\sigma_{LER} > 2.5$ nm. As past research [34] measures EUV $3\sigma_{LER}$ values at 2.58 nm, further relaxation of design spacing or improvement of manufacturing process may be required for acceptable lifetime.

Furthermore, we also look into the effects on TDDB failure probability due to LELE overlay mismatch. We choose the nominal duty cycle of 50% as our baseline. Fig. 13 shows the

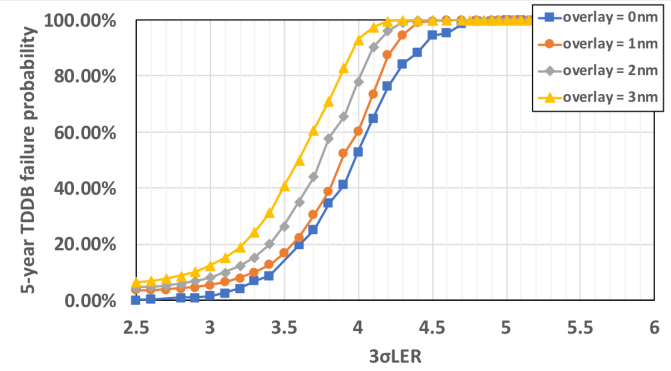

Fig. 13. 5-TDDB failure probability for 24 nm AES MINT1 with overlay.

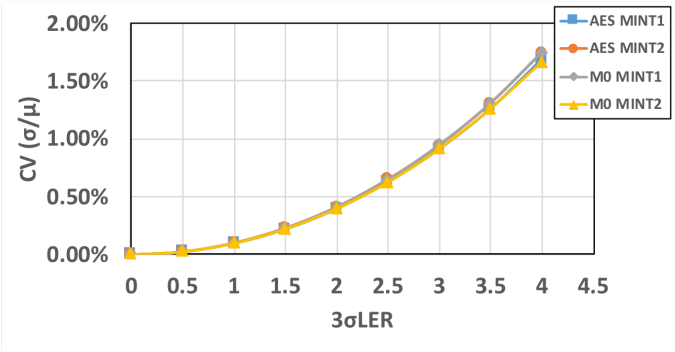

Fig. 14. Normalized variation of resistivity in AES and CORTEXM0DS for $3\sigma_{LER}$ = 3.5 nm.

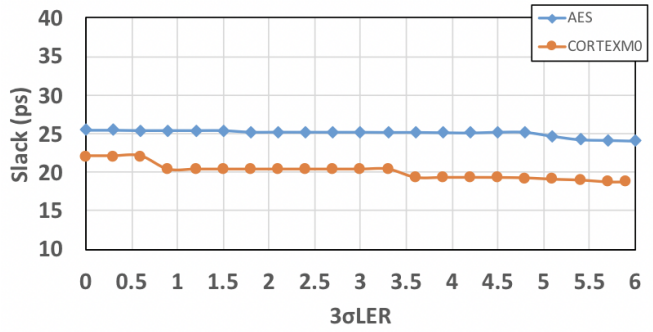

Fig. 15. Design slack against $3\sigma_{LER}$.

lifetime reduction with typical overlay values of 1-3 nm. It can be seen that with an overlay value of 3 nm, the failure probability at $3\sigma_{LER}$ = 2.5 nm reflects an unacceptable failure rate within 5 years. This is consistent with both past research [35] and our model, as overlay errors further reduce wire spacing at critical segments, and drastically reduce MTTF for TDDB. As double patterning may be required for EUV at sub-5 nm technology nodes, this presents a critical roadblock for further reduction in feature size.

G. Impacts of LER on EM failures in SRAM arrays

In this study, the MTTF of SRAM array sizes 64KB and 60MB, indicative of L1 and L3 caches [36], [37], are used to quantify the trade-off between higher activity factor and a greater number of bitlines. The dimension of a single cell array is also considered, as while wordline lengths are often constant within a process technology, vendors may resize bitline lengths for faster read/write or for uniform area. For our 64KB L1 cache, the activity factors are set to be 25% [38] for memory intensive applications and worst case 100% for artificial read-write programs. For the 60MB L3 cache, we set the activity factor to 1% and 25%. Bitlines of both 128 cells/bitline and 512 cells/bitline are considered. The current can then be estimated with the root-mean-square of leakage current and active current with respect to the activity factor [33], [39], [40]. We consider chip failure when the cache has 1% cumulative probability of bitlines entering the void saturation phase, as on-chip caches are optimized for speed and do not have advanced memory techniques such as page retirement.

Table I and Table II give the results of MTTF in years for EM failure. It can be seen that for L1 caches, failures due to EM do not occur within ten years despite the overly pessimistic 100% activity factor, regardless of the pitch size. For L3 cache, the unrealistic 25% activity factor also gives MTTF greater than ten years. Both simulations show that for $3\sigma_{LER} \leq 4$ nm, electro-migration does not cause significant concern as most processors are retired or updated within a decade. $3\sigma_{LER}$ values greater than 4 nm will degrade the lifetime even further, however the lifetime difficulties caused by TDDB failures in interconnects will be a much more significant issue. This is consistent with the Blech Effect [41] and the latest predictions of 7 nm nodes [42], as despite having smaller wire dimensions with non-scalable process variations, the near threshold supply voltage for 7 nm SRAMs results in a significant decrease in active current. The resulting product of current density and wire length proves insufficient to cause EM failure within a reasonable time frame.

IV. LER Impacts on Chip Level Metrics

As the technology node advances to sub-30 nm pitch and below, the performance of the chip becomes more and more dependent upon interconnect performance [4]. However, the interconnect performance is further impacted at smaller wire dimensions due to vulnerability to process variation, which influence delay, power consumption, and cross-talk between interconnect levels. In this section, the impact of LER on chip level metrics is evaluated with critical path delay via static timing analysis. We also extract and model the chip area penalty required in order to maintain chip bandwidth.

A. LER induced critical path delay variability

In this section, the variations in resistance and critical path delay is modeled with static timing analysis to evaluate LER impacts on chip timing performance. Wire geometry is extracted from the designs AES and CORTEXM0DS, while LER is modeled with the discussed model on wire pitches of 24 nm and 28 nm. We then back-annotate the SPEF files with scaled RC values for each net as a result of LER. The results

TABLE I
MTTF FOR EM FAILURE OF 24 NM PITCH (CACHE SIZE/CELL PER BITLINE/ACTIVITY FACTOR)

	64KB/128/25	64KB/128/100	64KB/512/25	64KB/512/100	60MB/128/1	60MB/128/25	60MB/512/1	60MB/512/25
$3\sigma_{LER}$ = 0 nm	60	32	60	32	285	60	285	60
$3\sigma_{LER}$ = 2.8 nm	32	17	32	19	112	27	111	27
$3\sigma_{LER}$ = 3.2 nm	27	15	29	17	91	23	97	22
$3\sigma_{LER}$ = 3.6 nm	25	14	26	15	75	18	84	19
$3\sigma_{LER}$ = 4.0 nm	22	14	23	14	62	14	71	16

TABLE II
MTTF FOR EM FAILURE OF 28 NM PITCH (CACHE SIZE/CELL PER BITLINE/ACTIVITY FACTOR)

	64KB/128/25	64KB/128/100	64KB/512/25	64KB/512/100	60MB/128/1	60MB/128/25	60MB/512/1	60MB/512/25
$3\sigma_{LER}$ = 0 nm	80	42	80	42	387	80	387	80
$3\sigma_{LER}$ = 2.8 nm	47	24	48	25	180	39	182	40
$3\sigma_{LER}$ = 3.2 nm	43	23	42	24	140	35	177	37
$3\sigma_{LER}$ = 3.6 nm	35	20	39	22	139	28	136	33
$3\sigma_{LER}$ = 4.0 nm	34	18	39	20	114	25	122	26

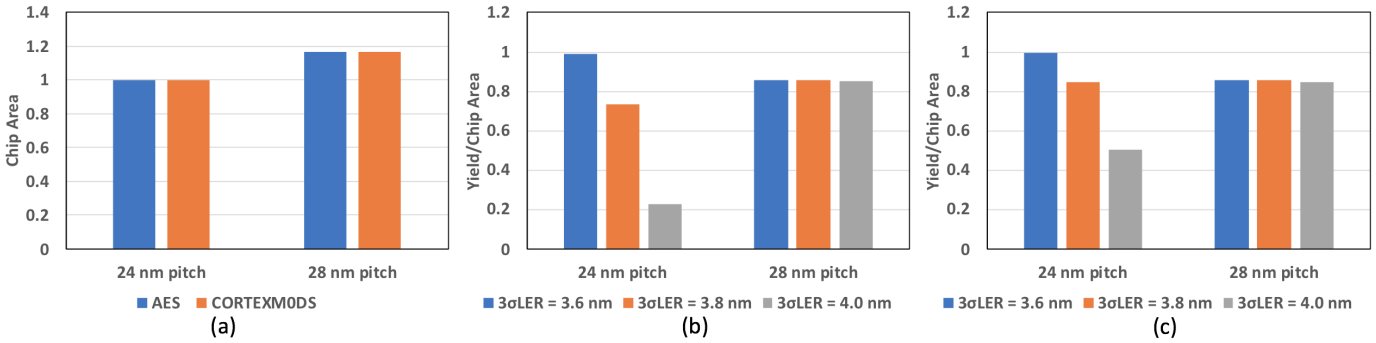

Fig. 16. (a) The estimated chip area when using different wire pitches. (b) Yield/chip area for AES. (c) Yield/chip area for CORTEXM0DS.

are modeled in Innovus with the resized NanGate FreePDK15 Open Cell Library [43].

Fig. 14 gives the results for the coefficient of variation of resistivity on differing test-benches, accounting for $3\sigma_{LER}$. It is shown that while variability increase is proportional to $3\sigma_{LER}$, the changes are design independent. Furthermore, the magnitude of variation is insignificant. This can be explained by averaging effects on the interconnects, where LER impacts 'average out' over sufficiently long wires.

Fig. 15 shows the results for minimum slack in AES and CORTEXM0DS for various $3\sigma_{LER}$, where $3\sigma_{LER}$ = 0 nm is the nominal slack value for no LER variation during manufacturing. It is observed that there is little decrement in slack values within the acceptable yield tolerance region for $3\sigma_{LER}$, which can be estimated as $3\sigma_{LER} \leq 3.5$ nm. This result indicates that an increase in LER has limited impact on chip delay.

Past research [44] concludes similar results, as electrical performance showed that the roughness creates an increase in the effective width of the wire and a decrease in the resistivity. However, despite larger LER values and limitations in mean free path (MFP), The impurities in the trenches yields a smaller scattering contribution of the sidewall, which results in smaller resistivity changes due to the LER. As such, LER mainly results in variations of the local line-width, and the effect on the resistivity is reduced.

B. Chip area penalty

As previous sections have shown, yield loss in dominated by short/open failures in interconnects. Therefore, interconnects with larger pitches can be applied to local metal layers to conserve yield at the cost of chip area in order to maintain chip bandwidth. In this section, we investigate the trade-off between area and bandwidth. Past research [45] shows that bandwidth can be evaluated depending on the delay and number of wires in each metal layer. Chip area can also be estimated via the wire density in each metal layer [46]. In this model, we use the 7-layer interconnect hierarchy [47], with 24 nm pitch wire applied to M1-M3, 36 nm in M4-M5, and 48 nm in M6-M7. Fig. 16(a) estimates the chip area of both designs normalized by chip area with 24 nm metal pitch. It can be observed that about 16% area penalty occurs when substituting 24 nm metal pitch for 28 nm.

We take chip area into account by normalizing yield as plotted in Fig. 16(b) and Fig. 16(c). It is observed that for small $3\sigma_{LER}$ values ($3\sigma_{LER}$ = 3.6 nm), 24 nm metal pitches can achieve high yield without invoking chip area penalties; yet for larger values of LER ($3\sigma_{LER}$ = 4.0 nm), interconnect layers with 28 nm pitch gives significantly greater yield despite incurring penalties. As LER variations for EUV are greater than traditional optical lithography, technology nodes that use EUVL for 24 nm metal pitches may choose to incur area penalties in order to maintain high yield, while designs with

28 nm metal pitches can preserve chip size without significant yield loss.

V. Conclusion

In this work, the possibility of patterning sub-30 nm copper interconnect wires with EUV under different LER and overlay variations is studied. An analytical and simulation-based yield model is proposed to assess test-benches for open/short failures, cut mask failures during SADP, LER enhanced TDDB failure, and EM failures for SRAM caches. Yield analysis results indicate that the yield threshold is dependent on the effective wire density; therefore larger pitches, lower utilization rates, and higher metal layers are more tolerant to LER variations. It is shown that EM failures are constrained as it results in negligible yield loss compared to open/short failures with similar LER process variations, while TDDB further limits tolerable LER margins in order to achieve acceptable lifetime. Furthermore, we give modelling results that indicate overlay errors as a critical issue in LELE patterning, as the uncertainty causes significant yield and lifetime degradation, with worst case estimates unfeasible with the current LER process technologies. It is also observed that at higher $3\sigma_{LER}$ values, yield loss can be recovered by penalizing chip area by 16% with small impacts on delay, while critical path delays are not significantly impacted by LER. In our future work, we plan to explore fault-tolerant designs with relaxed LER requirements and routing optimizations to reduce unacceptable yield and lifetime issues.

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