Leveraging NMOS Negative Differential Resistance for Low Power, High Reliability Magnetic Memory

Shaodi Wang, *Student Member, IEEE,* Andrew Pan, *Member, IEEE,* Cecile Grezes, *Member, IEEE,* Pedram Khalili Amiri, *Member, IEEE,* Kang L. Wang, *Fellow, IEEE,* Chi On Chui, *Senior Member, IEEE,* and Puneet Gupta, *Senior Member, IEEE*

***Abstract*—We propose, demonstrate, and assess a non-tunneling based NMOS voltage-controlled negative differential resistance (V-NDR) concept for overcoming the intrinsic efficiency and reliability shortcomings of magnetic random access memory memories (MRAM). Using NMOS V-NDR circuits in series with MRAM tunnel junctions, we experimentally observe 40X reduction in current during switching, enabling write termination and read margin amplification. Large scale Monte Carlo simulations also show 5X improvement in write energy savings and demonstrate the robustness of the scheme against device variability.**

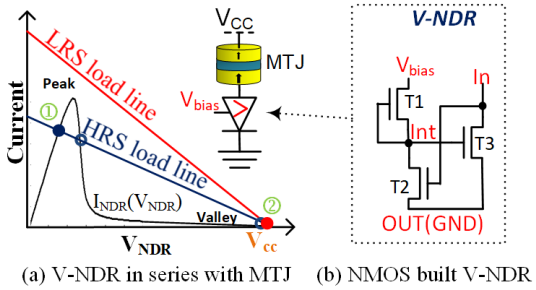
***Index Terms*—MRAM, negative differential resistance, readout circuits, resistive memory, write termination, read margin, read disturbance, reliability.**

I. Introduction

Magnetic random-access memories (MRAM) [1] using magnetic tunnel junctions (MTJ) are promising because of their non-volatility, speed, and high density, but have been hindered in practical usage by power consumption and reliability concerns. These issues are due to 1) the current-driven switching mechanism [2, 3] which requires long write times to minimize programming errors [4] and 2) practical constraints on the tunnel magnetoresistance ratio TMR = $(R_H - R_L)/R_L$ (where R_H and R_L are the high and low resistances) which limit the read voltage margin [5, 6]. To overcome these problems, we previously proposed [7, 8] incorporating voltage-controlled negative differential resistance devices (V-NDR) such as tunnel diodes (TDs) or tunnel FETs (TFETs) in MRAM read and write circuitry. Simulations showed that the peak and valley regions of the V-NDR device can be used to "amplify" the current difference between the MTJ states, allowing an unified low-overhead approach to reduce dissipation and improve reliability. However, because most V-NDR semiconductor devices like TDs or TFETs are either CMOS-incompatible or not yet technologically mature, their use in commercial memory applications may be problematic.

As the first technologically practical solution, therefore, in this paper, we propose and experimentally demonstrate a non-tunneling based V-NDR implemented using three-transistor (3T) NMOS circuits for MRAM read and write functions. This new approach has the following significant advantages: 1) it uses only conventional silicon MOSFETs, reducing cost while eliminating the compatibility issues associated with devices like TDs or TFETs, 2) it provides tunable V-NDR characteristics which can be matched to MRAM design specifications, and 3) it allows process variations to be reduced using mature CMOS processes and variation reduction techniques. In Section II we discuss the uses of V-NDR in MRAM, introduce our 3T NMOS design, and validate a simple NMOS V-NDR analytical model to ease design of circuit characteristics. In Section III we present experimental results which show how using NMOS V-NDR with 50nm voltage-controlled MTJs (VC-MTJ) [9] can improve read and write outputs and perform large scale simulations of the variability resilience of our design. We conclude in Section IV.

The authors are with the Department of Electrical Engineering, UCLA, Los Angeles, CA, 90095, (e-mails: shaodiwang@g.ucla.edu, pandrew@ucla.edu, grezes.cecile@gmail.com, pedramk@gmail.com, wang@ee.ucla.edu, chui@ee.ucla.edu and puneet@ee.ucla.edu).



(a) V-NDR in series with MTJ (b) NMOS built V-NDR

Fig. 1. (a) Load line for V-NDR-MTJ series circuit (illustrated in inset). Blue line corresponds to the MTJ HRS and red line to the MTJ LRS. The stable operating points when the MTJ is in HRS and LRS are indicated by ① and ②, respectively. (b) Diagram of proposed 3T NMOS circuit for generating V-NDR between IN and OUT terminals.

II. V-NDR Usage and Implementation

A. V-NDR Applications in MRAM

We first briefly review the key benefits of V-NDR usage in MRAM. The identifying features of V-NDR are the existence of a large peak current (I_{peak}) at low voltage and a small valley current (I_{valley}) at higher voltage, as illustrated in the generic I-V curve (black line) of Fig. 1 (a). We analyze the behavior of a series-connected V-NDR element and MTJ (shown in the inset of Fig. 1 (a)) by analyzing the load line of their respective I-V curves. When the externally applied voltage across the circuit increases from 0 to V_{dd}, if the MTJ is in its anti-parallel (AP) high resistance state (HRS), the current and voltage drop across the V-NDR stays in the peak region at point ① in Fig. 1 (a). Likewise, if the MTJ is in the parallel (P) low resistance state (LRS), the circuit will stabilize at ② in the V-NDR valley region. This indicates that current flows freely when the MTJ is in the AP state but is blocked when

the MTJ is in the P state. If the MTJ switches from AP to P, the current through the circuit drops from ① to ②. This operating scheme differs from that in previous proposals for V-NDR in memory [10–12] and offers significant advantages.

The current ratio between the AP and P states in conventional MRAM is limited by the TMR of the MTJ in each cell, which is typically of order 1-4X. Using V-NDR, the current ratio can be boosted up to the V-NDR peak-to-valley ratio $PVR = I_{peak}/I_{valley}$, which can be made very large (from 10-1,000X). MRAM switching is stochastic, and write pulse is over 3X average switching time to minimize possible write errors. The high PVR enables early write termination, reducing energy dissipation when writing from AP to P since the write current turns off automatically once switching occurs. (Though V-NDR does not offer any advantage when writing from P to AP, that switching direction does not waste as much power as AP to P, since in switching of P to AP, the post-switching state dissipates less power owing to the higher AP resistance.) The much larger current ratio using V-NDR also amplifies the read voltage margin, improving reliability. Finally, the small LRS current minimizes accidental switching of the memory state during read operations, i.e., read disturbance. These features are more thoroughly discussed in [7].

It is important to note that these advantages accrue without a significant change in area overhead because the V-NDR element can be implemented at the bit-line level rather than the 1T1M cell level, akin to sense amplifiers in conventional memories. All the cells in each bit-line (e.g., 1024 in a typical MRAM array) can share a single read or write V-NDR, as illustrated in Fig. 2 (a). Furthermore, conventional MRAM requires cascaded sense amplifiers to distinguish the small MTJ resistance ratio. Placing V-NDR in the read circuitry amplifies the resistance ratio, allowing a single-level sense amplifier to be used as shown in Fig. 2 (b); this saves two transistors from the read circuitry per bit-line, further lowering the area cost as well as associated leakage currents for the sense amplifier. In addition, the PVR does not need to be very high for substantial benefits to be realized. We find that a PVR of around 10 suffices for most applications.

B. 3T NMOS Circuit for V-NDR Generation

For integration into commercial memory technology, silicon MOSFETs are preferable to III-V tunnel devices [7]. We therefore propose generating V-NDR using three NMOS transistors in the circuit depicted in Fig. 1 (b). This circuit has three terminals (IN, OUT, and BIAS); T1 and T2 are used to control the gate bias of T3, and the V-NDR current is mainly driven by T3. The gate of T1 is connected to its drain to maintain low leakage, enabling low valley currents and hence write termination for MRAM. For small V_{in} applied between IN and OUT, the current increases due to the increased voltage drop across T3. However, V_{int} decreases with higher V_{in}, such that when V_{in} reaches a certain value V_{peak} (the peak voltage), the output current attains I_{peak} and the T2 transistor turns on and shuts off T3, leading to reduced output current with further increase in V_{in} (the "valley region"). The peak current and PVR can be selected by tuning the V_{bias} applied to T1

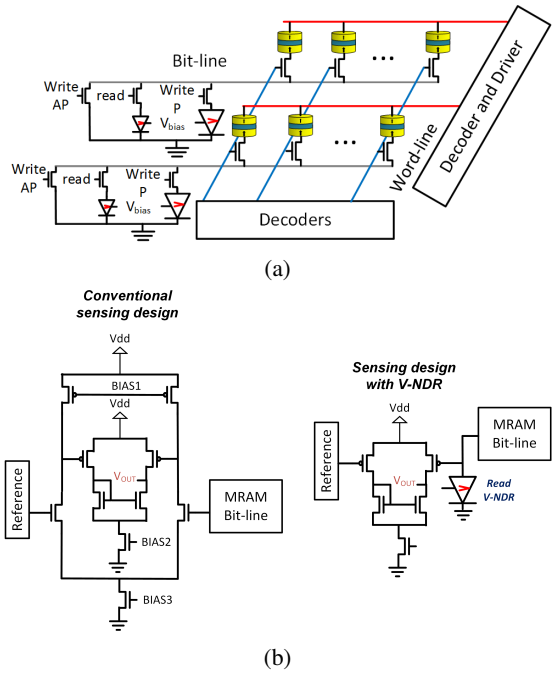


Fig. 2. (a) Schematic array level integration of write V-NDR and read V-NDR elements; note each element can be shared by an entire bit-line, leading to near-zero area overhead for large arrays. (b) Comparison of conventional MRAM cascaded sense amp design versus the more compact single-level design using V-NDR to improve read margin.

to change the T3 operation region. This circuit is therefore capable of low V_{peak} and highly tunable I_{peak} and PVR.

We have demonstrated this structure experimentally by wire bonding NMOS transistors on a single die. As shown in Fig. 3, the peak current can be tuned from the nA to μA range by changing bias voltage (V_{bias}) between 0.8 and 1.3 V while maintaining a peak voltage of 0.25 V and achieving PVR up to 1,000 and greater. Note that the sensitivity of peak current to V_{bias} is determined by the sizes and threshold voltages of the constituent transistors. In our experiment, the sensitivity is relatively high because we used a preexisting die whose transistor characteristics had not been specifically optimized. In real implementation, the devices can be designed to limit the V_{bias} tunability and hence reduce possible variability effects.

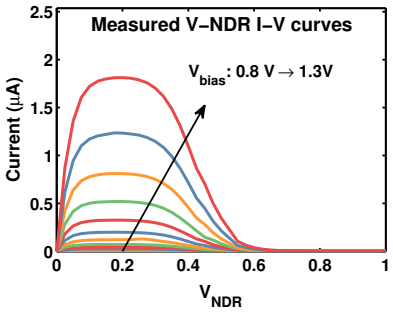


Fig. 3. Experimental I-V curves for NMOS V-NDR circuit; current is measured at IN terminal as a function of voltage drop V_{NDR} across the IN and OUT terminals. Different curves correspond to application of V_{bias} between 0.8 and 1.3V. The circuit is constructed using preexisting long channel NMOS devices with gate lengths of 10 μm, W/L ratios from 4 to 10, and off-currents around 0.1-1 nA and on-currents ranging between 10-100 μA.

C. Analytical Model of NMOS V-NDR Behavior

The characteristics of MRAM depend on technology and application, so to ease V-NDR design for any particular application, we derive a compact model of its current behavior. The essential design task for MRAM usage is to select the appropriate peak current and voltage to lie between the MTJ HRS and LRS load lines as shown in Fig. 1 (a). Typical peak voltages are around 50 to 200 mV (V_{peak}), indicating that transistors T1 and T2 (see Fig. 1) are in the subthreshold region. By contrast, T3 operates in the linear region with its gate bias over 400 mV (V_{int} in Fig. 1) when V-NDR is in peak region. The subthreshold current [13] I_{sub} for T1 and T2 can be modeled using

$$I_{sub} = \frac{WI_0}{L} e^{\frac{V_{GS}-V_{th}-\lambda V_S+\eta V_{DS}}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \quad (1)$$

where W and L are the transistor width and length, I_0 is a constant parameter, V_{th} is the threshold voltage, V_T is the thermal voltage, and n, λ, and η are the subthreshold swing, body effect, and drain-induced barrier lowering (DIBL) coefficients, respectively [13]. In typical operation, both T1 and T2 are in subthreshold and the same current flows through both devices, which is given using (1) for the respective biases and geometries of each device. By equating $I_{sub,T1} = I_{sub,T2}$ and solving for the voltage V_{int}, we find V_{int}, which is equivalent to the gate bias of T3, as a function of the T1 and T2 widths W_1 and W_2 and threshold voltage mismatch ($\Delta V_{th} = V_{th2} - V_{th1}$):

$$V_{\text{int}} = \left(\ln\left(\frac{W_1}{W_2}\right) nV_T + \Delta V_{th} + \eta V_{bias} - V_{in}\right) / (\lambda + 2\eta). \quad (2)$$

The current mostly flows through T3, which is in the linear region [14] around the V-NDR peak. The current of T3 as a function of V_{in} is

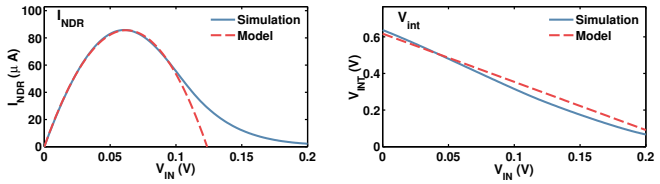
$$I_{T3}(V_{in}) = \mu C_{OX} \frac{W_3}{L_3} \left[\left(V_{\text{int}}(V_{in}) - V_{T3}\right) V_{in} - \frac{V_{in}^2}{2}\right]. \quad (3)$$

By maximizing I_{T3} as a function of V_{in}, we can obtain the V-NDR peak voltage and current by:

$$V_{peak} = \frac{\ln\left(\frac{W_1}{W_2}\right) nV_T + \Delta V_{th} - (\lambda + 2\eta) V_{th3} + \eta V_{bias}}{2 + \lambda + 2\eta} \quad (4)$$

$$I_{peak} = \frac{W_3}{L} \mu C_{ox} \times \frac{\left(\ln\left(\frac{W_1}{W_2}\right) nV_T + \Delta V_{th} - (\lambda + 2\eta) V_{th3} + \eta V_{bias}\right)^2}{2(2 + \lambda + 2\eta)(\lambda + 2\eta)}. \quad (5)$$

The V-NDR circuit enters the valley region when V_{in} pulls V_{int} to zero and turns off T3, in which case the current is limited by the leakage currents of T1 and T3. Equations (2)-(4) show the V-NDR characteristics can be designed by adjusting the T1 and T2 size and V_{th} mismatches as well as the terminal voltage V_{bias}.



(a) (b)

Fig. 4. Model and SPICE comparison of 3T V-NDR circuit using 45 nm commercial CMOS library for (a) I versus V_{in} and (b) V_{int} versus V_{in}.

D. Model validation

This model describes qualitative features of the V-NDR circuit as the comparison with SPICE simulations shows in Fig. 4. Good agreement is found for V_{int} and I_{NDR} with $V_{in} < 0.1$ V. The current mismatch for high V_{in} in Fig. 4 (a) is due to the oversimplified current equation for T3, which only works in linear region and is targeted to predict peak current and voltage.

TABLE I
NDR AND MRAM PARAMETERS FOR THREE DIFFERENT MRAM READ OR WRITE DESIGN.

MRAM				NDR		
MRAM	Operation	R_P	TMR	V_{dd}	W_3	V_{bias}
STT-MRAM	Write	5 kΩ	150%	0.8 V	1200 nm	0.85 V
STT-MRAM	Read	5 kΩ	150%	0.4 V	550 nm	0.8 V
MeRAM	Write/Read	50 kΩ	150%	1 V	210 nm	0.6 V

To validate the model functionality, we use it to guide NMOS V-NDR designs for representative MRAM read and write applications using either spin transfer torque (STT-MRAM) or magnetoelectric memory (MeRAM) technologies. The parameters of MRAM and corresponding V-NDR are specified in Table I. Since data on MTJ resistance of commercial MRAMs is not widely available, we choose illustrative values of 5 kΩ for STT-MRAM P resistance and 50 kΩ for MeRAM, which fall within the reported range for these technologies [9, 15, 16]. Higher TMR gives rise to larger design margin, so we use 150% as a baseline, noting that TMR up to 180% has been demonstrated in commercial STT-MRAM [17]. With these parameters, we design the V-NDR to allocate its peak current point between the R_{AP} and R_P load lines (see Fig. 1 (a)). We also use HSPICE to simulate the peak current point and its margin (the current difference from peak current point to R_{AP} and R_P load lines), which are plotted in Fig. 5. All predicted V-NDR peak current points lie close to the center of the simulated design margin, supporting the model.

III. Experimental and Numerical Validation

In this section, we validate the proposed applications of NMOS V-NDR in MRAM through experiment and simulation. In III-A, we measure the response of a V-NDR circuit in series with a voltage-controlled MTJ (VC-MTJ) as a function of time and applied magnetic field to illustrate how write termination and read margin amplification can occur for a single memory cell. This helps validate the concept and advantages of our approach at the device level (for reading/writing a single cell).

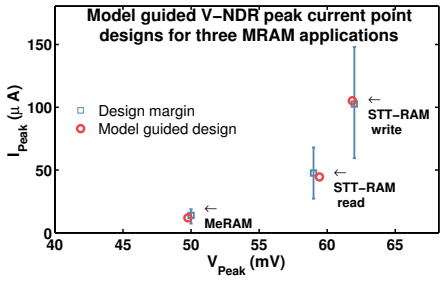


Fig. 5. Simulated peak current points of V-NDR designs guided by model and their margins for three MRAM applications. The error bars illustrate allowed design margins.

The switching of VC-MTJ is mostly controlled by voltage dropped across the device. Hence VC-MTJ usually has a high resistance to lower switching current and energy. Though VC-MTJ is used in the experiment, the demonstrated concept can be extended to other resistive memory devices, like STT-MTJ. However, device and circuit variability play an important role in the actual performance of real MRAM arrays. To prove that the demonstrated cell-level improvements can survive these effects, in section III-B we use Monte Carlo circuit simulations to show the robustness of the energy savings and accuracy improvements accounting for circuit variation.

A. V-NDR MTJ Experiments

As discussed above, we build a NMOS V-NDR circuit by wiring pre-fabricated MOSFETs on a single die, with the resulting characteristics shown in Fig. 3. We connect this circuit in series with a 50 nm diameter voltage-controlled MTJ [9]. The stack structure of the MTJ consists of bottom electrode/$Co_{20}Fe_{60}B_{20}$(1.1)/MgO(1.4)/$Co_{20}Fe_{60}B_{20}$(1.4)/Ta(0.25)/$[Co/Pd]_{10}$/top electrode (numbers in parentheses are thicknesses in nm).

The experimental MTJ can be switched between the AP and P states by either tuning the applied voltage (of order 0.4-0.7 V, corresponding to current of 1-2 μA) or an externally applied out-of-plane magnetic field. A sample MTJ $R-H$ curve is shown in Fig. 6. The MTJ is bistable for external fields between -1400 G to -1200 G, where stochastic switching between the P and AP states occurs due to thermal activation; outside the bistable range, the MTJ state can be deterministically controlled. The AP- and P-state resistances are around 320 kΩ and 240 kΩ under a voltage bias of 0.1 V.

The external wiring and transistor size limitations make the response time of our V-NDR circuits ($\sim$ 1 ms) much slower than the internal switching time of our MTJs ($\sim$ 1 ns), so that at present we cannot observe the switching on the internal time scale of the MTJs. Therefore, in these experiments, rather than relying directly on current-driven switching, we first use the external magnetic field to control the MTJ and avoid MTJ thermal activated switching during the V-NDR response time, as shown in Fig. 7. This is not a fundamental constraint since on-chip V-NDR circuits using nanoscale transistors can easily operate at higher speeds (on the order of ps) than MTJ switching times. By sweeping the external field magnitude, we could switch the MTJ from its AP to P state and back and observe the current response of the combined circuit. As seen in Fig. 7, a steep decline in current occurs when the MTJ switches from AP to P, pushing the V-NDR from the peak region ① (see Fig. 1 (a)) into the valley region ②; the low current is maintained even after the junction switches back to AP because the valley point ② is a stable state.

To better demonstrate write termination, we next initialize the MTJ in the AP state and then situate it in the bistable region by adjusting the external magnetic field to -1.34 kG. We then measure the current through the circuit (equivalent to the write current) as a function of time. In this regime, the MTJ can switch states due to voltage controlled magnetic anisotropy (VCMA) or spontaneous thermal activation [18]. The resulting measurement of current versus time is shown in Fig. 8. We observe around the 7.5 ms mark that the write current drops dramatically by a factor of 40 (from 1.2 μA to 25 nA), owing to the switching of the MTJ from the AP to P state at that time. Once this switching occurs, the V-NDR reaches its new stable point in the valley region and the current reaches and stays at a very low level. This mimics how write termination can occur in a real MRAM application when writing from AP to P states. As before, the application of an external magnetic field in this experiment is simply to bias the MTJ in bistable regime and thus lengthen the time scale of the switching so it becomes visible with our instrumentation and circuits. In a practical MRAM array, no external magnetic field is present and the time scale of switching will be far faster, as noted, but the effect of the V-NDR circuit remains the same.

We note that the intrinsic resistance ratio of the MTJ used in this experiment is only 1.33X as shown from the high and low resistance in Fig. 6 (=320 kΩ/240 kΩ at 0.1 V). This ratio should further reduce if a higher bias is applied to the device [17]. The effective TMR of 33% is smaller than that reported for other experimental MTJs in the literature, so our device is not fully optimized; nonetheless, the difference in current

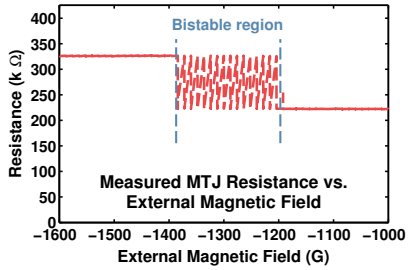


Fig. 6. Experimental MTJ resistance (R_H = 320 kΩ, R_L = 240 kΩ) as a function of external magnetic field.

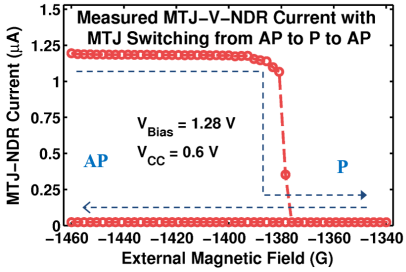


Fig. 7. Current through series-connected V-NDR and MTJ as external field is cycled to switch the MTJ from AP to P and back.

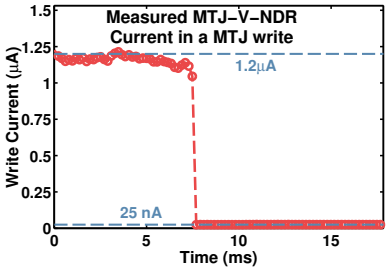


Fig. 8. Time-dependent measurement of MTJ-V-NDR current for MTJ initially in AP state and with external magnetic field of -1.34 kG biasing the device in the bistable region. $V_{CC} = 0.6$ V for this measurement. Note the drastic reduction in current through the circuit around 7.5 ms from 1.2 μA to 25 nA due to switching of the MTJ from the AP to P state.

between the two states once the V-NDR is introduced is far greater and amplified to in excess of 40X (=1.2 μA/25 nA in Fig. 8 and likewise in Fig. 7). This shows how read margin between the AP and P states can be drastically improved by 30X (=40X/1.33X) by using V-NDR during the read process. The improvement in current ratio may actually even more greater than 30X because the effective voltage drop across the MTJ is estimated to be around 0.3-0.4 V in the series connection, and the device TMR is likely to be lower than 33% (measured at 0.1V voltage bias) at high MTJ bias. As this demonstration was performed using preexisting MTJs and NMOS devices whose characteristics were not optimized for usage in V-NDR applications, we expect that even greater quantitative improvements will be possible for a pre-designed and integrated implementation in MRAM.

B. Array-level Variability Study

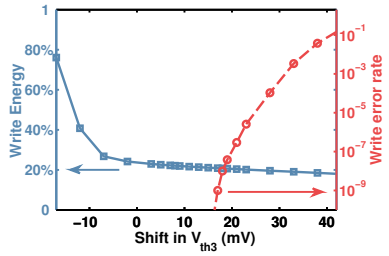


Fig. 9. Simulated write energy (normalized to conventional write scheme) and WER (right axis) vs. threshold voltage shift of T3 for 25 fF bit-line load (256 1T-1M cells per bit-line). The WER is extracted from 10 billion Monte-Carlo numerical simulations for V-NDR assisted STT-MRAM write. MTJ device parameters can be found in Table II.

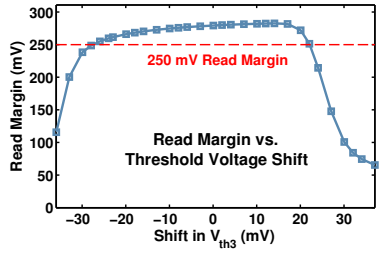


Fig. 10. Simulated STT-MRAM read margin vs. T3 threshold voltage shift. MTJ device parameters can be found in Table II.

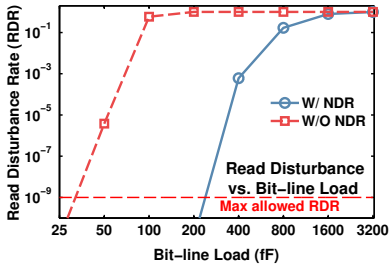


Fig. 11. Simulated read disturbance rate vs. bit-line size (load) for read design with and without V-NDR. Larger load leads to more pre-charging/discharging current and more read disturbance. The 256-bit line has a capacitive load of 25 fF.

The write termination and increased read margin characteristics that are experimentally observed can significantly improve the power consumption and reliability of MRAM [7]. At the array level, process variation and write error rate [19] are also main concerns due to the low TMR and stochastic switching behaviour of MTJs. We have proposed that V-NDR can also improve MRAM performance by reducing read disturbance. To quantify these improvements and evaluate their robustness in the presence of device fluctuations, we perform Monte-Carlo simulations of STT-MRAM read and write operations including NMOS V-NDR circuitry and considering both transistor and MTJ process variations [18] except for Fig. 10, where 3-σ-corner resistance are used for simulating read margin. The MTJ parameters used in our simulations can be found in Table II [18].

The dominant source of variability in the V-NDR circuit is the threshold voltage V_{th3} of the T3 transistor in Fig. 1 (a), which affects I_{peak} and PVR. In Fig. 9, we observe how the write energy improvement and write error rate (WER) for V-NDR-assisted operation vary with shifts in V_{th3}. As V_{th3} increases, I_{peak} reduces according to (4); this causes write termination to occur earlier during switching and reduces write energy but increases WER. For typical system requirements of WER $< 10^{-9}$ [7, 20], V_{th3} can vary over 35 mV while maintaining write energy savings from 20% to 80%. Please note that the MTJ variation has been included in the WER and read disturbance rate (RDR) simulation, which is shown in details in Table II. Similarly, we examine the impact on read margin in Fig. 10 and find that large voltage read margins (source-line voltage difference for reading AP and P) in excess of 250 mV can be sustained over a 60 mV window in V_{th3}. In practice, NMOS V-NDR circuits can be designed with large diffusion areas to minimize V_{th3} shifts to nearly zero, providing more than sufficient design margin.

We also simulated RDR for bit-line size from 25 fF to 400 fF. In STT-MRAM's precharge-and-sense read [21], the precharging/discharging current flowing through STT-MTJ

TABLE II
VARIATION PARAMETERS FOR STT-MTJS IN THE SIMULATIONS OF WRITE ERROR RATE AND READ DISTURBANCE RATE.

Parameters	Mean	Variation
Diameter	50nm	σ=1nm
MgO thickness	0.9nm	σ=0.003nm
T_{FL}	1.18nm	σ=0.003nm
Resistance	2KΩ / 5KΩ	Depending on MgO and Diameter

may falsely switch its state. In a V-NDR assisted read, the circuitry is designed such that the precharging/discharging current tries to switch MTJ to AP, and V-NDR is designed to allow peak and valley current for AP and P states respectively. This minimizes the disturbance current (i.e., P-to-AP switching). In the read, larger bit-line load leads to more precharging/discharging current and more read disturbance. The read disturbance rates of design with and without V-NDR are shown in Fig. 11 as a function of load size. V-NDR shows 10^9 X read disturbance reduction for bit-line load below 200 fF. With 10^{-9} error rate as a requirement, V-NDR improves the maximum bit-line load size from 30 fF in conventional read to 250 fF.

IV. Conclusion

We propose, model, and experimentally demonstrate a NMOS V-NDR circuit to improve MRAM write efficiency and read reliability. Experiments with MTJs demonstrate write termination and read margin improvement and show amplification of current ratio to 40X upon switching, even with unoptimized V-NDR and MTJ devices. Large scale Monte Carlo simulations similarly demonstrate large power and reliability improvements in the presence of device variability. Though our experiments are obtained using VC-MTJs and STT-MTJs, the same design can be applied to improve read/write circuitry for a wide array of magnetic and nonmagnetic resistive memories.

References

[1] S. Tehrani, J. M. Slaughter, E. Chen, M. Durlam, J. Shi, and M. DeHerren. "Progress and outlook for MRAM technology". *IEEE Transactions on Magnetics*, vol. 35, no. 5, pp. 2814–2819, Sept. 1999. ISSN: 0018-9464. DOI: 10.1109/20.800991.

[2] C. Heide. "Spin currents in magnetic films". *Physical review letters*, vol. 87, no. 19, p. 197201, 2001. DOI: 10.1103/PhysRevLett.87.197201.

[3] X. Fong, Y. Kim, K. Yogendra, D. Fan, A. Sengupta, A. Raghunathan, and K. Roy. "Spin-Transfer Torque Devices for Logic and Memory: Prospects and Perspectives". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 1, pp. 1–22, Jan. 2016. ISSN: 0278-0070. DOI: 10.1109/TCAD.2015.2481793.

[4] W. Kang, L. Zhang, W. Zhao, J. O. Klein, Y. Zhang, D. Ravelosona, and C. Chappert. "Yield and Reliability Improvement Techniques for Emerging Nonvolatile STT-MRAM". *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 1, pp. 28–39, Mar. 2015. ISSN: 2156-3357. DOI: 10.1109/JETCAS.2014.2374291.

[5] W. Kang, Z. Li, J. O. Klein, Y. Chen, Y. Zhang, D. Ravelosona, C. Chappert, and W. Zhao. "Variation-Tolerant and Disturbance-Free Sensing Circuit for Deep Nanometer STT-MRAM". *IEEE Transactions on Nanotechnology*, vol. 13, no. 6, pp. 1088–1092, Nov. 2014. ISSN: 1536-125X. DOI: 10.1109/TNANO.2014.2357054.

[6] Soheil Salehi, Deliang Fan, and Ronald F. Demara. "Survey of STT-MRAM Cell Design Strategies: Taxonomy and Sense Amplifier Tradeoffs for Resiliency". *J. Emerg. Technol. Comput. Syst.* Vol. 13, no. 3, 48:1–48:16, Apr. 2017. ISSN: 1550-4832. DOI: 10.1145/2997650. URL: http://doi.acm.org/10.1145/2997650.

[7] S. Wang, A. Pan, C. O. Chui, and P. Gupta. "Tunneling Negative Differential Resistance-Assisted STT-RAM for Efficient Read and Write Operations". *IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 121–129, Jan. 2017. ISSN: 0018-9383. DOI: 10.1109/TED.2016.2631544.

[8] S. Wang, S. Pal, T. Li, A. Pan, C. Grezes, P. Khalili-Amiri, K. L. Wang, and P. Gupta. "Hybrid VC-MTJ/CMOS non-volatile stochastic logic for efficient computing". *Design, Automation Test in Europe Conference Exhibition (DATE), 2017*. Mar. 2017, pp. 1438–1443. DOI: 10.23919/DATE.2017.7927218.

[9] C. Grezes, F. Ebrahimi, J. G. Alzate, X. Cai, J. A. Katine, J. Langer, B. Ocker, P. Khalili Amiri, and K. L. Wang. "Ultra-low switching energy and scaling in electric-field-controlled nanoscale magnetic tunnel junctions with high resistance-area product". *Applied Physics Letters*, vol. 108, no. 1, p. 012403, 2016. DOI: 10.1063/1.4939446.

[10] D. Halupka, S. Huda, W. Song, A. Sheikholeslami, K. Tsunoda, C. Yoshida, and M. Aoki. "Negative-resistance read and write schemes for STT-MRAM in 0.13 um CMOS". *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*. Feb. 2010, pp. 256–257. DOI: 10.1109/ISSCC.2010.5433943.

[11] Yohei Umeki, Koji Yanagida, Shusuke Yoshimoto, Shintaro Izumi, Masahiko Yoshimoto, Hiroshi Kawaguchi, Koji Tsunoda, and Toshihiro Sugii. "STT-MRAM Operating at 0.38 V Using Negative-Resistance Sense Amplifier". *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. 97, no. 12, pp. 2411–2417, 2014. ISSN: 1745-1337.

[12] Y. Umeki, K. Yanagida, S. Yoshimoto, S. Izumi, M. Yoshimoto, H. Kawaguchi, K. Tsunoda, and T. Sugii. "A negative-resistance sense amplifier for low-voltage operating STT-MRAM". *The 20th Asia and South Pacific Design Automation Conference*. Jan. 2015, pp. 8–9. DOI: 10.1109/ASPDAC.2015.7058920.

[13] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand. "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits". *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003. ISSN: 0018-9219. DOI: 10.1109/JPROC.2002.808156.

[14] J.R. Brews. "A charge-sheet model of the MOSFET". *Solid-State Electronics*, vol. 21, no. 2, pp. 345–355, 1978. ISSN: 0038-1101. DOI: http://dx.doi.org/10.1016/0038-1101(78)90264-2. URL: http://www.sciencedirect.com/science/article/pii/0038110178902642.

[15] R. Dorrance, F. Ren, Y. Toriyama, A. A. Hafez, C. K. K. Yang, and D. Markovic. "Scalability and Design-Space Analysis of a 1T-1MTJ Memory Cell for STT-RAMs". *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 878–887, Apr. 2012. ISSN: 0018-9383. DOI: 10.1109/TED.2011.2182053.

[16] Suock Chung, K. M. Rho, S. D. Kim, H. J. Suh, D. J. Kim, H. J. Kim, S. H. Lee, J. H. Park, H. M. Hwang, S. M. Hwang, J. Y. Lee, Y. B. An, J. U. Yi, Y. H. Seo, D. H. Jung, M. S. Lee, S. H. Cho, J. N. Kim, G. J. Park, Gyuan Jin, A. Driskill-Smith, V. Nikitin, A. Ong, X. Tang, Yongki Kim, J. S. Rho, S. K. Park, S. W. Chung, J. G. Jeong, and S. J. Hong. "Fully integrated 54nm STT-RAM with the smallest bit cell dimension for high density memory application". *2010 International Electron Devices Meeting*. Dec. 2010, pp. 12.7.1–12.7.4. DOI: 10.1109/IEDM.2010.5703351.

[17] Y. J. Song, J. H. Lee, H. C. Shin, K. H. Lee, K. Suh, J. R. Kang, S. S. Pyo, H. T. Jung, S. H. Hwang, G. H. Koh, S. C. Oh, S. O. Park, J. K. Kim, J. C. Park, J. Kim, K. H. Hwang, G. T. Jeong, K. P. Lee, and E. S. Jung. "Highly functional and reliable 8Mb STT-MRAM embedded in 28nm logic". *2016 IEEE International Electron Devices Meeting (IEDM)*. Dec. 2016, pp. 27.2.1–27.2.4. DOI: 10.1109/IEDM.2016.7838491.

[18] "Comparative Evaluation of Spin-Transfer-Torque and Magnetoelectric Random Access Memory". *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 6, no. 2, pp. 134–145, June 2016. ISSN: 2156-3357. DOI: 10.1109/JETCAS.2016.2547681.

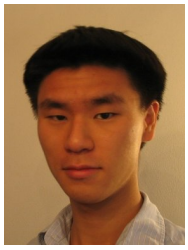
[19] Shaodi Wang, Hochul Lee, Cecile Grezes, Pedram Khalili, Kang L. Wang, and Puneet Gupta. "MTJ Variation Monitor-

assisted Adaptive MRAM Write". *Proceedings of the 53rd Annual Design Automation Conference*. DAC '16. Austin, Texas: ACM, 2016, 169:1–169:6. ISBN: 978-1-4503-4236-0. DOI: 10.1145/2897937.2897979. URL: http://doi.acm.org/10.1145/2897937.2897979.

[20] S. Wang, H. (. Hu, H. Zheng, and P. Gupta. "MEMRES: A Fast Memory System Reliability Simulator". *IEEE Transactions on Reliability*, vol. 65, no. 4, pp. 1783–1797, Dec. 2016. ISSN: 0018-9529. DOI: 10.1109/TR.2016.2608357.

[21] H. Lee, J. G. Alzate, R. Dorrance, X. Q. Cai, D. Marković, P. Khalili Amiri, and K. L. wang. "Design of a Fast and Low-Power Sense Amplifier and Writing Circuit for High-Speed MRAM". *IEEE Transactions on Magnetics*, vol. 51, no. 5, pp. 1–7, May 2015. ISSN: 0018-9464. DOI: 10.1109/TMAG.2014.2367130.

Shaodi Wang (S'12) is currently a researcher in the NanoCAD lab at Department of Electrical Engineering, UCLA. Shaodi received the Ph.D. degree in electrical engineering from UCLA, in 2017, and the B.S. degree from Peking University in 2011.



Andrew Pan (S'12-M'15) is currently in a post-doctoral researcher at the Department of Electrical Engineering, University of California, Los Angeles. His research interests include electronic device modeling, transport phenomena, and solid state physics.

Cecile Grezes (M'15) received the B.Sc. degree in Physics and Mathematics from the Université Joseph Fourier, Grenoble, in 2008, the M.Sc. in Physics from the Ecole Normale Supérieure, Paris, in 2011, and the Ph.D. degree (cum laude) in physics from CEA Saclay/Université Pierre et Marie Curie, Paris in 2014.

Pedram Khalili Amiri (M'05) received the B.Sc. degree from the Sharif University of Technology in 2004 and the Ph.D. degree (cum laude) in electrical engineering from Delft University of Technology in 2008. He is an Assistant Adjunct Professor at the EE Dept. of University of California at Los Angeles since 2009.

Kang L. Wang (F'92) received the B.S. degree from the National Cheng Kung University, Taiwan, and the M.S. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, MA, USA. He is currently a Distinguished Professor and holds the Raytheon Chair Professor in physical science and electronics with the Electrical Engineering Department, University of California at Los Angeles, Los Angeles, CA, USA.

Chi On Chui (S'00–M'04–SM'08) received his Ph.D. degree in electrical engineering from Stanford University. He is currently an Associate Professor with the Department of Electrical Engineering and Bioengieering at UCLA, conducting research on circuit-device interaction and bioelectronics.

Puneet Gupta (M'07-SM'16) is currently a faculty member of the Electri-cal Engineering Department at UCLA. He received the B.Tech degree in Electrical Engineering from Indian Institute of Technology, Delhi in 2000 and Ph.D. in 2007 from University of California, San Diego. He co-founded Blaze DFM Inc. (acquired by Tela Inc.) in 2004 and served as its product architect till 2007.