Spin Electronics

Source Line Sensing in Magneto-Electric Random-Access Memory to Reduce Read Disturbance and Improve Sensing Margin

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Abstract— A source line sensing (SLS) scheme is presented, along with a corresponding memory core circuit architecture, for the sensing operation of magneto-electric random-access memory (MeRAM). Compared to a conventional bit-line sensing (BLS) scheme, the proposed SLS, which exploits the voltage-controlled magnetic anisotropy (VCMA) effect, applies a voltage across the magneto-electric tunnel junction (MEJ) with an opposite polarity. The SLS significantly reduces read disturbance and increases the sensing margin due to the enhanced coercivity of the bit during the read operation. Experimental data demonstrate that the thermal stability of nanoscale MEJs increases up to 2 times during the SLS operation compared with conventional BLS. An MEJ compact model based the SLS simulation shows that read disturbance improves by a factor greater than 10^9 fJ/V·m and the sensing margin increases up to 3 times in the MEJ with the large VCMA coefficient $(>100$ fJ/V·m$)$.

Index Terms—Spin electronics, magneto-electric tunnel junction, magneto-electric random-access memory, voltage-controlled magnetic anisotropy, tunneling magnetoresistance, read disturbance, thermal stability.

I. INTRODUCTION

The magneto-electric tunnel junction (MEJ) is an emerging variant of the magnetic tunnel junction (MTJ) device used in magnetic random-access memory (MRAM), which exploits magneto-electric interface effects to control its free layer magnetization, and tunneling magnetoresistance (TMR) to read its state. These electric-field-controlled nano-magnets are being developed as basic building blocks for the next generation of memory and logic applications, since they have the potential for significant reductions in power dissipation, offer high endurance and density, and can be applied to high-speed operation systems.

The MEJ differs from a conventional magnetic tunnel junction in that an electric field is used to induce switching, in lieu of substantial current flow for utilizing spin transfer torque (STT) in a current-controlled MTJ [Alzate 2012, Huai 2004, Ikeda 2010, Kanai 2012, Katine 2000, 2008, Shiota 2012a, 2012b, Wang 2013, Wang 2012]. Compared to MTJs, MEJs have three noticeable advantages: i) extremely low dynamic switching energy due to significant reduction of Ohmic loss, ii) sub-nanosecond writing speed based on precessional switching (which for STT devices requires very large currents through the device to achieve the same speed), iii) high density in a memory array application due to the use of minimum sized access transistors or diodes in a cell.

Magneto-electric random-access memory (MeRAM) uses MEJ devices in its memory cell array. MeRAM offers the potential to replace conventional SRAM-based caches and DRAM based working memories in the Von Neumann computer architecture since the performance of MeRAM is comparable with that of conventional memories in terms of speed (1 ns or less), density (6 F^2), and endurance $(>10^{15})$ where F is the minimum feature size, and endurance is defined as the number of program cycles. In addition, non-volatility of MeRAM gives rise to zero leakage, achieving dramatic standby power reduction [Khalili Amiri 2015].

However, some challenges currently prevent MeRAM from being implemented in embedded system memory applications. One problem is read failure, which occurs when a sensing circuit cannot distinguish between two states of the memory cell without changing the memory state due to the small sensing margin. This is caused by the low tunneling magnetoresistance (TMR) ratio in typically used material systems in spin-transfer torque magnetic random-access memory (STT-RAM) and MeRAM. As the sensing margin decreases, the memory becomes more susceptible to noise, increasing the read failure and requiring a dedicated circuit to amplify signals. The other issue is the read disturbance, a chance of flipping the MEJ state after applying an electric read pulse (i.e., the probability of a destructive read), which is not affected by TMR but by the thermal stability. The read disturbance happens when reading occurs by charging up bit lines to a certain voltage level (sensing voltage) in MeRAM as well as STT-RAM. To be specific, this bit-line voltage reduces the energy barrier E_b between the two stable states of an MEJ via the voltage-controlled magnetic anisotropy (VCMA) effect. The possibility of the destructive read exponentially therefore increases as the sensing voltage of bit lines increases, since the applied voltage lowers the thermal stability $(\Delta = E_b/kT)$ of the MEJ, where k is the Boltzmann constant and T is temperature.

To increase the sensing margin and reduce the read disturbance, we propose a source line sensing (SLS) scheme for MeRAM, which reversely exploits the VCMA effect to stabilize the bit (MEJ) during sensing. The basic concept of the reverse use of VCMA effect was introduced in our previous work on MeRAM based ternary content

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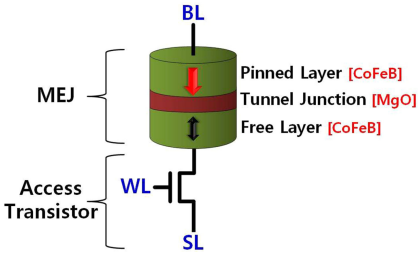

Fig. 1. A 1-transistor/1-MEJ MeRAM cell structure with a transistor as the access device. A bit line (BL) and a source line (SL) are connected to the pinned layer of the MEJ and the source of the access transistor, respectively. Note that the orientation of the MEJ layers may be reversed depending on the sign of the VCMA coefficient. A word line (WL) controls the gate of the transistor.

addressable memory (TCAM) application [Wang 2015]. However, that paper does not provide quantitative assessments based on experimental data and simulation data from a large number of trials.

In this paper, besides providing a corresponding memory core circuit architecture for the SLS, we measured the retention time from nanoscale (60 nm) MEJs by changing the sensing voltage across the MEJ and extracted read disturbance by executing 10^{10} attempts based on MEJ compact model simulation. The experiment data shows that the SLS (applying -0.6 V) lengthens the retention time by up to a million times $(\times 10^6)$ compared to the BLS (applying 0.6 V). Also, the simulation results show that the SLS can significantly reduce read disturbance up to 10^9 times and improves its sensing margin by 3 times.

II. BACKGROUND AND MEJ OPERATION

An MEJ device consists of two ferromagnetic layers divided by a tunneling barrier MgO, as shown in Fig. 1. The magnetic moment of one layer can switch freely by using the electrical and magnetic field, and the magnetic moment of the other layer is fixed. The MEJ has a low resistance (R_P) when the magnetic moments of the free and pinned layers are aligned along the same direction, i.e., in the parallel state (denoted as P). In the anti-parallel state (denoted as AP), the free layer magnetization is aligned in the opposite direction to the pinned layer, resulting in a high resistance (R_{AP}) [Wang 2015].

Switching of MEJs can be executed via precessional (also referred to as resonant) or thermally activated switching depending on the required speed of the reversal. Recent research efforts have demonstrated VCMA-effect-based switching of perpendicularly magnetized MEJs in both precessional and thermally activated regimes [Alzate 2012, Kanai 2012, Shiota 2012]. The schematic illustration of voltage-controlled MEJ precessional switching is shown in Fig. 2 [Khalili Amiri 2015] where K_i is the perpendicular magnetic anisotropy (PMA), ξ is the VCMA coefficient, t_{CoFeB} is the thickness of the free layer, d_{MgO} is the thickness of the MgO, and M_s is the saturation magnetization. Under zero bias condition across the MEJ, the magnetization of the free layer is aligned with the out-of-plane direction, due to the large PMA. The PMA (K_i) is reduced by applying a voltage, given the correct polarity, hence lowering the energy barrier of the free layer. If the PMA decreases sufficiently to remove the barrier (due to an applied voltage of at or above a critical value), switching can occur by a precessional reorientation of the magnetic moment. In

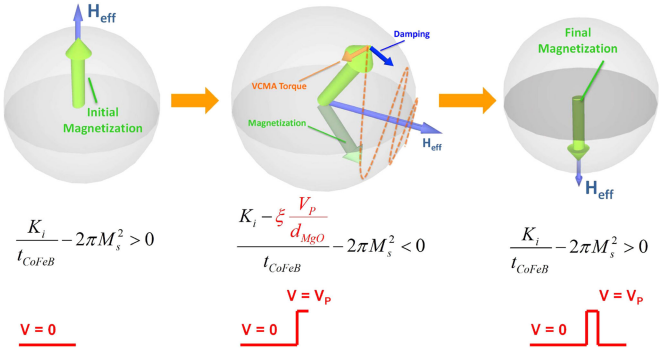

Fig. 2. Schematic illustration of VCMA-induced precessional switching mechanism in the free layer of an MEJ with perpendicular magnetization. At zero bias condition ($V = 0$), the free layer magnetization is aligned with the out-of-plane direction due to the sufficiently large PMA. When a voltage applied across the device reduces the PMA due to the VCMA effect, the magnetic moment starts to precess around the in-plane direction. If the width of the applied pulse is designed to coincide with half the precession period, full 180° switching can be achieved. Note that voltage with opposite polarity will not switch the free layer, provided the dependence of PMA on applied voltage is odd, which is the case in most reported experiments.

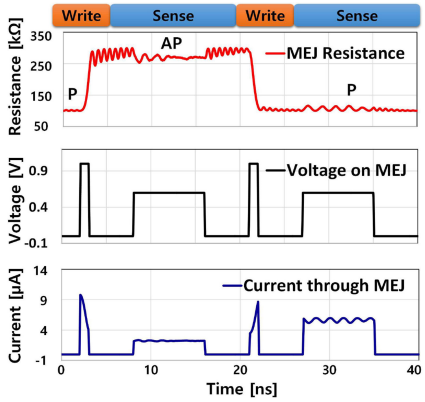

Fig. 3. Conventional write and sense operations of MeRAM. For the write operation, a 1 V write pulse, which has 1 ns duration, is applied to the bit line to switch the MEJ state. A sensing voltage (0.6 V) is applied across the device for reading, which might cause unwanted switching due to the reduced energy barrier of the free layer.

the case where the barrier is not sufficiently reduced, switching still can happen through thermal activation across the barrier. This causes read disturbance in the presence of a small sensing voltage applied to the device, provided it has the same polarity as the write voltage.

There are two basic modes which need to be considered for device design in memory operations, i.e., write mode and read mode. For writing, in the case of MeRAM, a pulse generator circuit applies a write pulse of suitable duration to the bit line (see Fig. 1) to switch the MEJ state. The basic modes are illustrated in Fig. 3, showing simulation results from an MEJ macrospin compact model incorporating VCMA-based switching, taking into account thermal effect and demagnetizing field, and other key physical effects [Lee 2014, Wang 2016]. In the MEJ compact model simulation, a write pulse (1 ns, 1.2 V) can switch the MEJ state from P to AP or from AP to P. This demonstrates the resonant but non-deterministic feature of precessional switching, where the state of the bit is always reversed regardless of its initial state for a given pulse duration. If the control

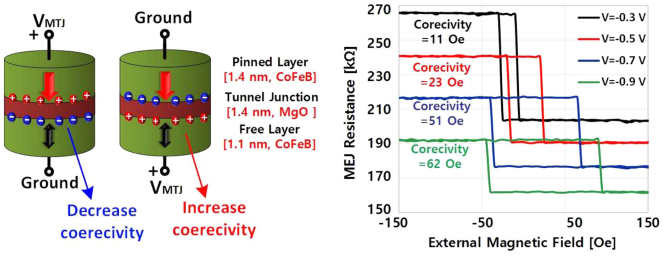

Fig. 4. (a) Voltage dependence of the coercivity. Based on the polarity of the applied voltage, the coercivity of the free layer changes due to the VCMA effect. (b) Measured coercivity with respect to the applied voltage across the device. The ground and V_{MEJ} are connected to the pinned (top) layer and the free (bottom) layer, respectively. In this condition, as the amplitude of the bias increases, the coercivity continues to enhance from 11 Oe (−0.3 V) to 62 Oe (−0.9 V).

circuit uses the conventional BL sensing (BLS) scheme, a moderate sensing voltage (e.g., ∼0.6 V) is applied to the bit lines for reading. Then, sense amplifiers detect the voltage or current of the bit line to read the MEJ state during the read mode.

III. SOURCE LINE SENSING SCHEME

Reading of an MEJ, unlike typical STT devices, is strongly affected by the choice of voltage polarity during the read operation, since the VCMA effect results in a change of PMA in the free layer under voltage application, which in turn leads to a coercivity change. This is illustrated in Fig. 4(a) for the case of MgO|CoFeB|Ta based MEJs, where a negative (positive) voltage across the perpendicularly magnetized MEJ increases (decreases) the coercivity of the bottom free layer. Fig. 4(b) shows the measured corresponding coercivity change of an MEJ (RA product 650 $\Omega \cdot \mu\mathrm{m}^2$, diameter 60 nm, 1.1 nm thick CoFeB free layer, 1.4 nm thick MgO barrier layer) as a function of voltages across the device [Grèzes 2016]. In this case, the MEJ has its free layer at the bottom, and the coercivity is enhanced as the amplitude of negative voltage increases. The change of coercivity, in turn, varies the thermal stability of the free layer. Although the non-vanishing STT effect shifts the offset field due to the electric dc bias (a few seconds), the effect is negligible in an actual read operation (5–50 ns).

As a result of this coercivity dependence, the BLS scheme has a possibility of causing read disturbances in MeRAM cell arrays. This is especially the case for embedded system memory applications, which may only require a relatively short retention time (<1 ms) since they have a relatively low thermal stability ($\Delta \sim 20$–30) compared to storage applications (typically $\Delta > 40$). To reduce the read disturbance during the BLS scheme, the sensing voltage (pre-charge voltage) on the bit line should be limited, which, however, reduces the sensing margin.

The VCMA effect can be used to enable the SLS scheme, resulting in the reduction of read disturbance and the improvement of sensing margin. In this paper, sensing margin can be defined by the potential difference between V_{sen} (the SL node) and V_{ref} (the REF node) as shown in Fig. 5. The key idea of the SLS is to apply a sensing voltage on the source line, hence increasing the coercivity of the MEJs during the read operation, taking advantage of the odd dependence of PMA on voltage in typical MEJ material systems. Although applying a negative read voltage to BL has the same effect as the SLS does, generating

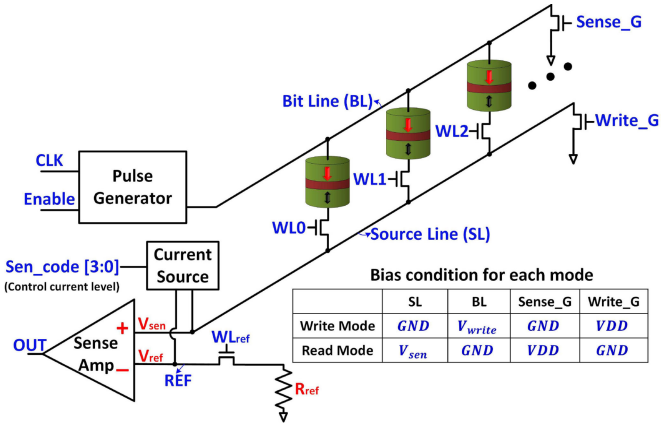

Fig. 5. Proposed core circuit architecture for the SLS. The pulse generator is connected to the BL and provide a write pulse to switch MEJs. The sense amp and the current source circuit are connected to the SL so that they generate a sensing voltage in an opposite polarity of the write pulse, reducing the possibility of read disturbance.

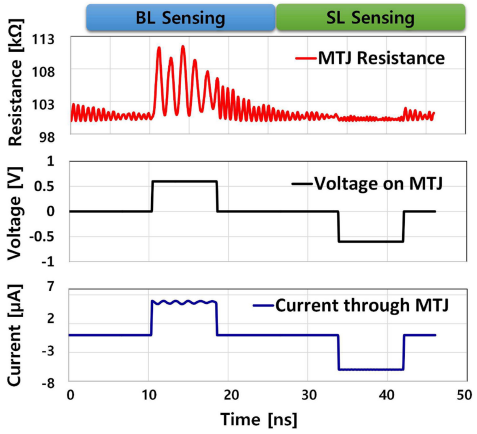

Fig. 6. Simulation results of the BLS and the SLS based on the physical MEJ compact model. A positive voltage across the MEJ causes resistance fluctuations up to 13% due to the reduced PMA. On the contrary, the resistance of MEJ is stable when a negative voltage is applied, achieving reliable sensing and reducing read disturbance.

a negative bias requires more resources (e.g., charge pump circuit) in the chip where it has a positive power supply and common ground. Fig. 5 shows the proposed MEJ cell array and core architecture for the SLS. In this architecture, the sense amplifier (sense amp) and the current source are connected to the source line, and a number of MEJ cells are attached to both the bit line and the source line. The pulse generator is connected to the bit line. To select an MEJ, VDD should be applied to one of word lines (WLs) during the each operation mode.

For the write mode, the pulse generator provides a write pulse to the bit line while the potential of the source line discharges to the ground level by applying VDD on the *Write_G* node. On the other hand, during the read mode, the bit line is grounded by applying VDD on the *Sense_G* node. Then, the current source supplies a certain amount of current to the source line and the *REF* node, which generates V_{sen} and V_{ref} at each node, respectively. The potential difference between V_{sen} and V_{ref} is amplified by the sense amp, generating a digital output "0" (AP) or "1" (P) at the *OUT* node.

Fig. 6 shows a comparison between the BLS and the SLS schemes based on the compact model transient simulation. In the case of the

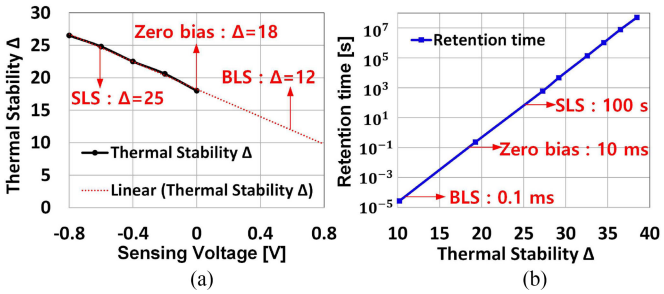

Fig. 7. (a) Measured thermal stability of an MEJ device with respect to voltage across the device. Due to the VCMA effect, the thermal stability is a function of the applied voltage, which has $-16\ \mathrm{V}^{-1}$ slope. (b) Retention time is calculated based on the amplitude of the thermal stability at room temperature. At zero bias condition, retention time is 10 ms. The retention time is modulated by the type of sensing scheme. During the BLS, the retention time is reduced to 0.1 ms, increasing the possibility of read disturbance. However, the retention time is increased to 100 s by using the SLS.

BLS, there is an MEJ resistance fluctuation up to 13%, resulting in an unstable sensing current which may cause the sensing to fail. In addition, as it is being read, the MEJ state can be switched to the opposite state, since the VCMA effect lowers the energy barrier, causing read disturbance. Therefore, the sensing voltage of the BLS needs to be carefully determined within a range where it avoids read disturbance while taking that into account. However, if the sensing voltage is too low, it limits sensing margins. During the SLS, in contrast, the resistance of the MEJ becomes more stable compared to the BLS case, which allows the sense amp to have more reliable sensing results. Furthermore, as the amplitude of the sensing voltage on the source line increases, the MEJ enhances its thermal stability. This implies that the sensing margin is not limited by the sensing voltage, but rather by the voltage dependence of the TMR, hence obtaining a larger sensing margin compared to the BLS.

IV. EVALUATION

For quantitative assessment of the SLS, we measured the thermal stability (retention time) as a function of the amplitude of an applied voltage to the MEJ [Rippard 2011]. In this experiment, the measured MEJ has a 60 nm diameter, and its thermal stability (Δ) is equal to 18 (retention time $\sim$10 ms) at zero bias condition. The thermal stability is modulated at a rate of $-16\ \mathrm{V}^{-1}$ as shown in Fig. 7(a). In the case of the BLS (0.6 V), the thermal stability is below 12 when the sensing voltage is applied. On the other hand, it reaches 25 in the case of the SLS (-0.6 V). These values, in turn, can be converted to the retention time as shown in Fig. 7(b) [Brown 1963]. The retention times of the BLS and the SLS are 100 μs and 100 s, respectively.

The increase in the retention time of the SLS significantly improves the reliability of MeRAM for system memory applications. Although the MEJ compact model has different parameters ($K_i = 1 \times 10^{-3}$ j/m^2, $\Delta = 29.2$ at zero bias, $\xi = 100 \sim 200$ fJ/V·m, diameter $= 60$ nm) compared to the measured data, it is possible to quantitatively evaluate the read disturbances in terms of switching probability. In this simulation, we assume the MEJ has a relatively large VCMA coefficient. Fig. 8(a) shows the simulated read disturbance as a function of the sensing voltage, which has a 50 ns duration. There is a significant read disturbance under the positive sensing voltage (BLS),

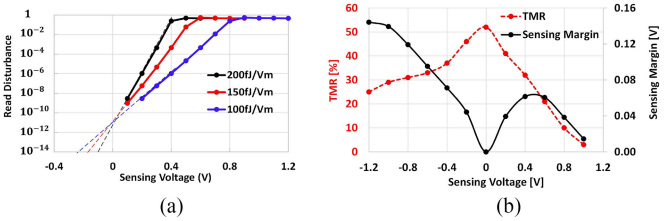

Fig. 8. (a) Read disturbance (switching probability) as a function of sensing voltage, simulated using the MEJ compact model. When the sensing voltage exceeds 0.6 V (BLS), the read disturbance rapidly rises and converges to 50%. However, in the negative bias region (SLS), it achieves the read disturbance below 10^{-12}. (b) Maximum sensing margin as a function of sensing voltage. In the case of SLS, the sensing margin increases with reverse voltage, until it becomes limited by reduction of the TMR due to the applied voltage bias.

resulting in the reliability issue. However, the SLS achieve the read disturbance below 10^{-12}, which is a fairly acceptable value, and it decreases further by increasing the sensing voltage on the source line.

The sensing margin relies on the applied sensing voltage and TMR [Kalitsov 2013]. If TMR is a constant value, the sensing margin can be improved as the applied sensing voltage increases. However, actual TMR is reduced as the sensing voltage rises. Therefore, there is an optimal sensing voltage that gives rise to the maximum sensing margin with an acceptable read disturbance. In this simulation (relatively high VCMA coefficients), we use a voltage sensing scheme, comparing V_{sen} (the SL node) and V_{ref} (the REF node), and assume that TMR (at zero bias 52%) is a function of the applied sensing voltage. As shown in Fig. 8(b), in the BLS approach, the sensing margin is limited by the sensing voltage (0.4 V) which causes significant read disturbance ($>10^{-6}$), obtaining the maximum sensing margin of the BLS (50 mV). However, in the case of the SLS, the sensing margin (150 mV) can be achieved at the sensing voltage (-1.2 V) without causing any read disturbance. Above this sensing voltage ($>|-1.2\ \mathrm{V}|$), the sensing margin starts to diminish since the reduced TMR cancels it out. In short, the sensing margin of the SLS is limited not by the voltage which causes read disturbance but by the voltage that limits TMR, achieving a 3 times higher sensing margin compared to that of the BLS.

V. CONCLUSION

We have presented an SLS scheme that exploits the VCMA effect of alleviating read disturbances and increasing sensing margins in magneto-electric memory circuits. The SLS approach is distinct from BLS in that it raises the thermal stability by applying a sensing voltage in the opposite polarity. Compared to the BLS (0.6 V), the SLS (-0.6 V) lengthens the retention time by up to a million times $(\times 10^6)$, hence reducing unwanted switching during the read operation. In addition, the sensing margin can be improved by increasing the sensing voltage on the source line, enlarging the potential difference between the source line and the reference node.

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