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Comprehensive defect avoidance framework for mitigating extreme ultraviolet mask defects

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Abstract. Defect avoidance methods are likely to play a key role in overcoming the challenge of mask blank defectivity in extreme ultraviolet (EUV) lithography. In this work, we propose an innovative EUV mask defect avoidance method. It is the first approach that allows exploring all the degrees of freedom available for defect avoidance (pattern shift, rotation and mask floorplanning). We model the defect avoidance problem as a global, nonconvex optimization problem and then solve it using a combination of random walk and gradient descent. For a 8-nm polysilicon layer of an ARM Cortex M0 layout, our method achieves a 60% point better mask yield compared to prior art in defect avoidance for a 40-defect mask. We show that pattern shift is the most significant degree of freedom for improving mask yield. Rotation and mask floorplanning can also help improve mask yield to a certain extent. © *2014 Society of Photo-Optical Instrumentation Engineers (SPIE)* [DOI: 10.1117/1.JMM.13.4.043005]

Keywords: extreme ultraviolet; masks; defects; defect mitigation; buried defects; mask yield; optimization; random walk; gradient descent.

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1 Introduction

Extreme ultraviolet (EUV) lithography remains the most promising next-generation lithography solution to replace the current deep ultraviolet lithography.[1] In addition to source power, mask blank defectivity is one of the key challenges facing this technology.[2]

In conventional 193-nm lithography, the photomask containing the circuit pattern (layout) comprises transparent and opaque regions. However, the lack of transparent materials for 13.5-nm light means that EUV masks must be reflective. EUV masks are Bragg reflectors comprising several alternating layers of molybdenum and silicon. The thickness of these materials is chosen to enable the reflected light at each interface to intefere constructively. The circuit pattern is placed on the top of this multilayer reflector in the form of an absorber layer.[3]

During the manufacure of EUV masks, small particles or imperfections in the substrate can manifest themselves as mask defects. Even tiny mask blank defects can significantly alter the pattern printed on the wafer. For example, even a 3.5-nm tall defect can cause a massive critical dimension (CD) change of 20 nm on the wafer.[4] This is illustrated in Fig. 1.

EUV mask manufacturers have recently reported that they can achieve mask blanks with zero defects of a size larger than 100 nm.[5] However, defects smaller than 100 nm are also capable of causing yield loss. More importantly, mask blank inspection tools tend to miss several defects,[6] thus the severity of this problem remains unclear. Because these mask defects are buried under multilayers, repairing them is very challenging.[7]

Due to the defective and hard-to-repair nature of EUV mask blanks, the ability to tolerate some of these defects without any impacts on yield is a very attractive proposition. Defect avoidance-based techniques have emerged as a very effective means to tolerate mask defects. These techniques rely on inspection of mask blanks to first determine defect locations. The position of the design pattern which needs to be written on the mask can then be shifted relative to the mask to avoid the defects. There are three degrees of freedom that can be exploited to avoid mask blank defects:

- "Pattern Shift" requires moving the entire mask field pattern relative to the defective mask blank to avoid defects. Several prior approaches look at methods to exploit a pattern shift to avoid defects.[8–11]
- "Rotation" involves rotating the entire mask pattern about the center of the mask blank. Most approaches consider rotation only in multiples of 90 deg.[8,10,11] However, Zhang et al.[12] propose small-angle rotation as well. Although this additional flexibility can improve the chances of using a defective mask blank, it is unclear whether EUV scanners will be able to support the nonorthogonal rotation of the mask.
- "Mask Floorplanning" avoids defects by independently moving each die copy inside the mask field. Kagalwalla and Gupta,[13] and Du et al.[14] propose methods to perform mask floorplanning together with a pattern shift. There are two key issues that could hinder the use of mask floorplanning as a defect avoidance method. First, it can lead to gaps between die copies (scribe area), which is area wasted on the wafer. However, this wasted scribe area is <1% of the total area of the die copies according to our experimental results in Sec. 4.3. Second, different layers of the same design must be simultaneously moved. Consequently, mask floorplanning can help improve defect avoidance

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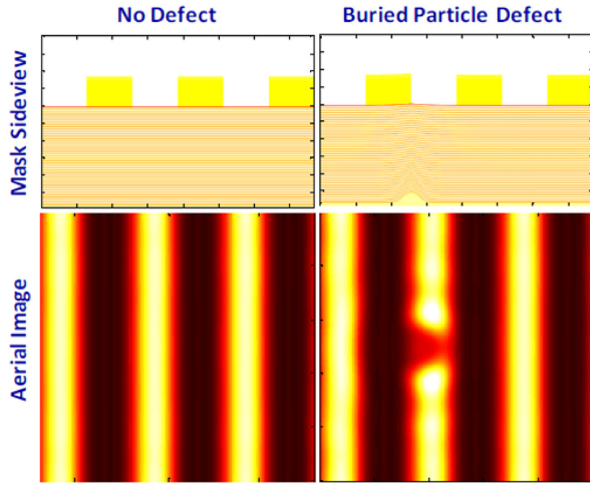

Fig. 1 Illustration of extreme ultraviolet (EUV) mask defect.[4]

only if the number of critical design layers patterned using EUV lithography is small.

Figure 2 summarizes the different degrees of freedom. Elayat et al.[15] and Jeong et al.[16] provide a cost-benefit assessment of different defect avoidance and reticle planning strategies, respectively. The low accuracy of mask blank inspection tools is a serious limitation for defect avoidance-based mitigation. Recent techniques have also looked at methods that can tolerate defect position inaccuracy.[13,17] Alternate approaches for mask defect mitigation that rely on correcting the absorber pattern after mask write have also been proposed,[4,18] but they may be less effective than defect avoidance techniques,[19] especially for large defects or a high defect density.

In this work, we present a global optimization-based defect avoidance method to mitigate EUV mask defects. To the best of our knowledge, this is the first work on EUV mask defect mitigation that allows simultaneous optimization of all the three degrees of freedom offered by defect avoidance: pattern shift, rotation, and floorplanning. We formulate the problem as a nonconvex optimization problem and then solve it using a combination of hit-and-run based random walk and gradient descent. Some other key features of our methodology are as follows:

- Multilayer: When multiple layers of a single design need to be patterned with EUV, the entire mask pattern corresponding to each layer can be independently shifted. The various die copies, however, must have the same relative location to ensure alignment. The floorplanning method proposed by Kagalwalla and Gupta[13] accounts for this by using a two-step heuristic, where the pattern shift of each layer is done first, followed by simultaneous floorplanning. Our formulation enables simultaneous global optimization of the pattern shift and floorplanning, thereby allowing better exploration of the solution space.
- Continuous: Our method explores the continuous solution space, instead of making discrete moves as done in the previous works on defect avoidance floorplanning[13] and small-angle rotation.[12]

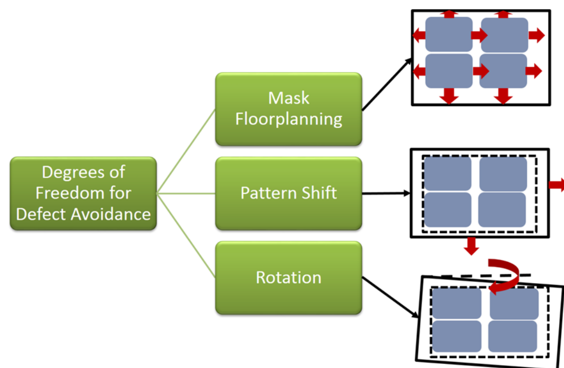

Fig. 2 Summary of three degrees of freedom for avoiding EUV mask defects.

The remainder of this paper is organized as follows. Section 2 describes our problem formulation, which is followed by the details of our solution methodology in Sec. 3. Section 4 then shows some simulation results where we compare our method to prior work. Finally, we conclude this work in Sec. 5. All notation used in this paper is summarized in Table 1.

2 Holistic Defect Avoidance Problem Formulation

In this work, we focus on EUV mask defect avoidance of single-project masks. This is because EUV is likely to be economically viable only for high-volume designs where single-project masks are used. Moreover, we shall assume that the floorplan of the die copies on the mask is gridded. Although this restricts the potential solution space, it guarantees full dicing yield. The number of die copies inside the mask is kept fixed. This contrasts with Du's approach,[14] where the number of die copies on the defective mask is maximized.

Since pattern shift and rotation can be done independently for each layer, we define (Xp_l, Yp_l, Θ_l) as the coordinates of the center of the mask field relative to the center of the mask itself and the rotation of each layer, l. Mask floorplanning, on the other hand, must be done together for all the layers to ensure layer alignment. Hence, we define the relative coordinates of the r'th row of dies relative to the zeroth row as Yf_r $[r \in 1,2\ldots(R-1)]$, and the relative coordinate of the c'th column of dies relative to the zeroth column is Xf_c $(c \in 1,2,\ldots C-1)$. The goal of EUV mask defect avoidance is to determine this set of $3L+R+C-2$ variables such that the impact of the defects is minimized.

In order to ensure that the final mask is manufacturable, certain spatial constraints need to be satisfied by any defect avoidance solution. The various types of constraints are the following:

1. "Reticle boundary constraints" ensure that the entire mask field is inside the usable area of the mask. These spatial constraints must account for rotation and must be applied for each EUV layer of the design. In order to make these constraints linear, we make the small angle assumption ($\sin\Theta \approx \Theta$, $\cos\Theta \approx 1$).

$$\pm Xp_l \pm \tfrac{W_F}{2}\Theta_l \le \tfrac{W_M - W_F}{2} \quad \pm Yp_l \pm \tfrac{H_F}{2}\Theta_l \le \tfrac{H_M - H_F}{2} \quad \text{for } l \in \{1,2,\cdots,L\} \tag{1}$$

2. "Maximum field constraints" ensure that mask floorplanning does not move the die copies too far apart causing the field size to become too large.

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Table 1 Glossary of terminology.

Term	Description
$W_D(H_D)$	Width (height) of die
$W_M(H_M)$	Width (height) of usable area of mask blank
$W_F(H_F)$	Width (height) of mask field size
L	Number of design layers patterned using EUV
l	Particular design layer under consideration
$R(C)$	Number of rows (columns) of die copies in mask field
$r(c)$	Row (column) number under consideration
Xp_l	X co-ordinate of center of mask field relative to mask blank center for layer l
Yp_l	Y co-ordinate of center of mask field relative to mask blank center for layer l
Θ_l	Angle by which the mask field pattern is rotated relative to the mask blank co-ordinates
Xf_r	X co-ordinate of r'th row of dies
Yf_c	Y co-ordinate of c'th column of dies
Nd_l	Number of defects in mask blank assigned to design layer l
$Wd_l(n)$	Full width half maximum of n'th defect in mask blank assigned to design layer l
$Hd_l(n)$	Height of n'th defect in mask blank assigned to design layer l
$X(e)$	X co-ordinate of a vertical absorber edge e relative to die center
$\hat{X}(e)$	X co-ordinate of a vertical absorber edge e relative to mask field center
$Y_{\text{low}}(e)$	Bottom y co-ordinate of a vertical absorber edge e relative to die center
$\hat{Y}_{\text{low}}(e)$	Bottom y co-ordinate of a vertical absorber edge e relative to mask field center
$Y_{\text{high}}(e)$	Top y co-ordinate of a vertical absorber edge e relative to die center
$\hat{Y}_{\text{high}}(e)$	Top y co-ordinate of a vertical absorber edge e relative to mask field center
$r(e,n)$	Distance between absorber edge e and the center of n'th defect
$u(.)$	Unit step function. $u(y)=1$ if $y \geq 0$, $u(y)=0$ otherwise
$\text{Def Height}(e,n)$	Height of n'th defect at location of absorber edge e
$CD_{\text{def}}(e,n)$	Change in critical dimension (CD) of absorber edge e caused by n^{th} defect
CD_{tol}	CD tolerance for mask defects
Cost	Overall CD impact cost function for defect avoidance
N_G	Number of iterations of gradient descent for each starting point
S	Step size of gradient descent

$$Xf_{C-1} + W_D \leq W_F \quad Yf_{R-1} + H_D \leq H_F \tag{2}$$

3. "Die overlap constraints" ensure that the die copies do not overlap.

$$Xf_1 \geq W_D \quad Xf_{c+1} - Xf_c \geq W_D \quad \text{for } c \in \{1,2,\cdots,(C-2)\} \tag{3}$$

$$Yf_1 \geq H_D \quad Yf_{r+1} - Yf_r \geq H_D \quad \text{for } r \in \{1,2,\cdots,(R-2)\} \tag{4}$$

4. "Maximum allowed rotation" restricts the maximum angle by which we can rotate the mask blank.

$$-\Theta_{\max} \leq \Theta_l \leq \Theta_{\max} \quad \text{for } l \in \{1,2,\cdots,L\} \tag{5}$$

This leads to a total of $8L + 2 + (C-1) + (R-1) + 2L$ linear constraints.

A key part of this defect avoidance methodology is to model the CD impact of defects as a function of these pattern shift, rotation, and mask floorplanning variables. Suppose the mask corresponding to the l'th layer contains Nd_l defects and suppose the n'th defect has height $Hd_l(n)$ and a full-width half maximum width (FWHM) $Wd_l(n)$. Suppose the co-ordinate of the center of the defect is $[Xd_l(n), Yd_l(n)]$ relative to the mask center. To account for pattern shift and rotation, the defect co-ordinates can be modified as shown in Eqs. (6) and (7):

$$\hat{X}d_l(n) = Xd_l(n)\cos(\Theta_l) - Yd_l(n)\sin(\Theta_l) - Xp_l \tag{6}$$

$$\hat{Y}d_l(n) = Xd_l(n)\sin(\Theta_l) + Yd_l(n)\cos(\Theta_l) - Yp_l. \tag{7}$$

Next, let us consider one vertical edge of an absorber shape e with x co-ordinate $X(e)$ and y co-ordinates $[Y_{\text{low}}(e), Y_{\text{high}}(e)]$, relative to the die origin. If the absorber edge is a part of a die in the r'th row and c'th column, we can write the co-ordinates of the edge relative to the mask origin as shown in Eq. (8):

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$$\hat{X}(e) = X(e) + Xf_c \quad \hat{Y}_{\text{low}}(e) = Y_{\text{low}}(e) + Yf_r$$
$$\hat{Y}_{\text{high}}(e) = Y_{\text{high}}(e) + Yf_r. \tag{8}$$

We can then compute the distance of the edge from the defect using Eq. (9), where $u(y)$ is the step function that is one if $y \geq 0$, else it is zero. Using this distance, we can then compute the CD impact of the defect on the layout shape using the linear model proposed by Clifford et al.[4] and described by Kagalwalla et al.,[13] as shown in Eq. (11). The values of I_{NoDef}, m_{def}, b_{def}, and ImageSlope are constants whose values are taken from the proposed model.[4] D_A is an additional parameter which is 1 if the defect center lies outside the absorber and 0.5 if it lies inside. The CD impact of defects is scaled up by three to guardband against a defocus of 75 nm:[4]

$$r(e,n)^2 = [\hat{X}d_l(n) - \hat{X}(e)]^2 + [\hat{Y}d_l(n) - \hat{Y}_{\text{low}}(e)]^2 u[\hat{Y}_{\text{low}}(e) - \hat{Y}d_l(n)] + [\hat{Y}d_l(n) - \hat{Y}_{\text{high}}(e)]^2 u[\hat{Y}d_l(n) - \hat{Y}_{\text{high}}(e)] \tag{9}$$

$$\text{Def Height}(e,n) = Hd_l(n)\exp\left\{\frac{-r(e)^2}{[Wd_l(n)/2]^2}\right\} \tag{10}$$

$$CD_{\text{def}}(e,n) = \frac{3D_A \cdot \sqrt{I_{\text{No Def}}} \cdot (m_{\text{def}} \cdot \text{Def Height} + b_{\text{def}})}{\text{Image Slope}}. \tag{11}$$

In order to ensure that the die works, we must ensure that the CD impact of the defect is less than the CD tolerance for every absorber edge. Since the number of mask defects is significantly smaller than the number of absorber edges in the field pattern, we assume that a single absorber edge is not affected by more than one defect. Moreover, a defect only impacts a small set of absorber edges around it, so for any given floorplan solution, we only need to look at the absorber shapes within a certain distance of the defect. In this work, we take this distance as $3 * Wd_l(n)$. This significantly reduces the overhead of checking every defect-absorber edge pair of the mask pattern. The CD tolerance value for any absorber edge could be a single value assigned to all absorber shapes, or be design-aware, as done by Kagalwalla et al.[20]

3 Random Walk + Gradient Descent-Based Solution Method

The objective of EUV mask defect avoidance is to determine a feasible value of $Xp_l, Yp_l, \Theta_l, Xf_c$ and Yf_r such that all the spatial constraints and CD tolerance constraints are obeyed. The spatial constraints are simple linear constraints. However, the CD tolerance constraints are nonconvex as proven below.

Theorem: For any absorber edge defect pair, the constraint $CD_{\text{def}}(e,n) \leq CD_{\text{tol}}$ is nonconvex.

Proof: Consider a left vertical edge of an absorber shape as shown in Fig. 3 below. Let us consider the multivariable function $f(Xp_l, Yp_l, \Theta_l, Xf_c, Yf_r) = CD_{\text{def}}(e,n) - CD_{\text{tol}}$. By analytically computing the partial second derivative with respect to any of the pattern shift (Xp_l, Yp_l), rotation (Θ_l) or floorplanning variables (Xf_c, Yf_r), we find that it is not guaranteed to be positive for all possible defect-absorber edge positions. This proves that all the CD tolerance constraints are nonconvex. Geometrically, we can consider two potential defect locations relative to this edge, as shown in Fig. 3. Both defect locations obey the CD constraint, but the line segment connecting them contains potential defect locations which would cause a CD violation. This implies that the geometric space of feasible defect locations relative to a single-absorber edge is nonconvex.

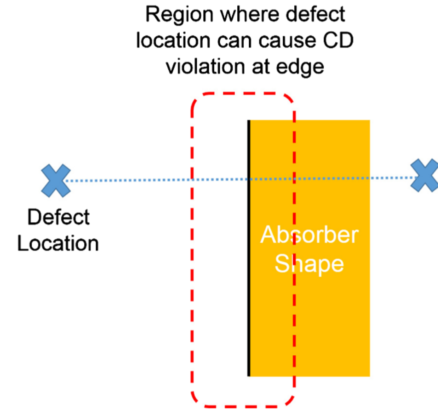

Fig. 3 Illustration of nonconvexity of cirical dimension (CD) constraint showing that two feasible defect locations and the segment connecting them crosses through the prohibited region for an absorber edge.

Since handling nonconvex constraints is very hard in optimization, we relax the CD tolerance constraints by converting it into an objective function that we then minimize. We use the sigmoid penalty function to relax every CD constraint $(\text{sigmoid}(x) = 1/1 + e^{-\alpha x},\ \alpha = 4.0$ for this work). As a result, the cost function for our optimization problem is the sum of sigmoids for all the relevant defect-absorber edge pairs, as shown in Eq. (12). Hence, our overall optimization problem is to find the pattern shift, rotation, and mask floorplanning variables to minimize this sigmoid cost function while obeying the linear spatial constraints of Eqs. (1) to (5).

$$\text{Cost} = \sum_{\text{All Defects}} \sum_{\text{Absorber Edges}} \text{sigmoid}(CD_{\text{def}} - CD_{\text{tol}}). \tag{12}$$

To solve the nonconvex optimization problem for EUV mask defect avoidance, we use a combination of random walk and gradient descent. Random walk is used to perform a coarse grained search over the multidimensional linear polytope formed by the spatial constraints. For each of the sample points generated by random walk, we use gradient descent for a local search in the vicinity of the sample. The overall method is summarized in Fig. 4.

We use a hit-and-run based Markov chain random walk, which is known to mix fast.[21] Starting from an initial point inside the linear polytope, hit-and-run finds new points inside the linear polytope using the following steps:

1. Draw a line in a randomly chosen direction passing through the given point.

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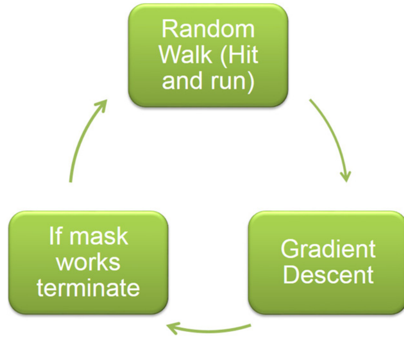

Fig. 4 Illustration of the method used to solve the EUV mask defect avoidance problem.

2. Find the two points where this line intersects the linear polytope.
3. Pick a random point on the line segment connecting the two points above.
4. Go back to Step 1 with this new random point.

In order to apply gradient descent to each sample point generated by random walk, we need to analytically compute the gradient of the cost function of Eq. (12). The analytical expression for the gradient of one defect and vertical absorber edge pair is shown in Eq. (13). The intermediate variables Z_1, Z_2 and U_Y are shown in Eqs. (14) to (16), respectively. Note that the discontinuity of the cost function at $\hat{Y}_{\text{low}}(e)$ and $\hat{Y}_{\text{high}}(e)$ is handled by function U_Y in Eq. (16) by assuming that only one of the three conditions will hold during a round of gradient descent. Since gradient descent moves in small steps, this assumption is reasonable.

$$\begin{aligned}
\frac{\partial \text{Cost}}{\partial (Xp_l)} &= \frac{\partial \text{Cost}}{\partial CD_{\text{def}}} \frac{\partial CD_{\text{def}}}{\partial [r(e)^2]} \frac{\partial [r(e)^2]}{\partial (Xp_l)} \\
&= -2Z_1Z_2 \cdot [\hat{X}d_l(n) - Xf(e)] \\
\frac{\partial \text{Cost}}{\partial (Yp_l)} &= \frac{\partial \text{Cost}}{\partial CD_{\text{def}}} \frac{\partial CD_{\text{def}}}{\partial [r(e)^2]} \frac{\partial [r(e)^2]}{\partial (Yp_l)} = -2Z_1Z_2 \cdot U_Y \\
\frac{\partial \text{Cost}}{\partial (\Theta_l)} &= \frac{\partial \text{Cost}}{\partial CD_{\text{def}}} \frac{\partial CD_{\text{def}}}{\partial [r(e)^2]} \frac{\partial [r(e)^2]}{\partial (\Theta_l)} \\
&= -2Z_1Z_2 \cdot [Xd_l(n) \sin \Theta_l + Xd_l(n) \cos \Theta_l] \\
\frac{\partial \text{Cost}}{\partial (Xf_c)} &= \frac{\partial \text{Cost}}{\partial CD_{\text{def}}} \frac{\partial CD_{\text{def}}}{\partial [r(e)^2]} \frac{\partial [r(e)^2]}{\partial (Xf_c)} \\
&= -2Z_1Z_2 \cdot [\hat{X}d_l(n) - Xf(e)] \\
\frac{\partial \text{Cost}}{\partial (Yf_r)} &= \frac{\partial \text{Cost}}{\partial CD_{\text{def}}} \frac{\partial CD_{\text{def}}}{\partial [r(e)^2]} \frac{\partial [r(e)^2]}{\partial (Yf_r)} = -2Z_1Z_2 \cdot U_Y
\end{aligned} \tag{13}$$

$$Z_1 = \frac{\partial \text{Cost}}{\partial CD_{\text{def}}} = \alpha \cdot \text{sig}(CD_{\text{def}} - CD_{\text{tol}}) \cdot [1 - \text{sig}(CD_{\text{def}} - CD_{\text{tol}})] \tag{14}$$

$$Z_2 = \frac{\partial CD_{\text{def}}}{\partial [r(e)^2]} = \frac{3D_A \cdot \sqrt{I_{\text{No Def}} m_{\text{def}}}}{\text{Image Slope}} \cdot \text{Def Height} \cdot \frac{-1}{[Wd_l(n)/2]^2} \tag{15}$$

$$U_Y = \begin{cases} [\hat{Y}d_l(n) - \hat{Y}_{\text{low}}(e)], & \text{if } \hat{Y}d_l(n) \le \hat{Y}_{\text{low}}(e) \\ 0, & \text{if } \hat{Y}_{\text{low}}(e) \le \hat{Y}d_l(n) \le \hat{Y}_{\text{high}}(e) \\ \hat{Y}d_l(n) - \hat{Y}_{\text{high}}(e), & \text{if } \hat{Y}d_l(n) \ge \hat{Y}_{\text{high}}(e) \end{cases} \tag{16}$$

For computing the gradient of the cost function, we need to find all the interacting defect-absorber edge pairs, calculate the analytical expressions of Eq. (13) for each such pair and then add them. Since the number of defects are typically much smaller than the number of absorber shapes on the mask, we do this by iterating over all the defects and finding all the absorber shapes within a certain distance $[3\times Wd_l(n)]$ of each defect. We then compute the gradient for each absorber edge within this radius of influence of the defect. Finding all absorber shapes within a certain radius of a defect can be done efficiently by storing the entire mask layout in a two-dimensional region query tree data-structure.[22]

The running time for computing the gradient during the iterations of local search is dominated by the process of repeatedly querying the large layout. Since only small moves are made during the local search, we can avoid this overhead by upfront storing of all the absorber shapes that could be affected by any defect when we make small local moves. For examples, if we set the maximum number of gradient descent iterations for each random starting solution as N_G and the gradient step size is S, we can upfront store all the absorber shapes that are within a radius of $2{\cdot}N_G \cdot S + 3 \cdot Wd_l(n)$ of a particular defect. At the start of the gradient descent iterations, we store all such shapes for each defect. As a result, we do not need to query the large layout every time the gradient needs to be computed.

4 Results and Discussion

Our proposed EUV mask defect avoidance method has been implemented in C++. OpenAccess API has been used to read and access layout shapes.[23] The Eigen Matrix library is used to handle vectors and matrix operations.[24] All our results are shown for an ARM Cortex M0 processor layout which was synthesized, placed, and routed using Cadence Encounter with a 32 nm Synopsys Standard Cell Library. The layout is then scaled to an 8-nm technology node to show our results. We apply defect avoidance to the polysilicon layer unless otherwise stated. Although we set the CD tolerance of every shape to 10% of the technology node ($CD_{\text{tol}} = 0.8$ nm), it is also possible to make the CD tolerance assignment design aware.[13]

We assume single size for all the defects, with peak height $Hd_l = 2$ nm and FWHM $Wd_l = 50$ nm except in Sec. 4.4. Due to the lack of any real data on the spatial distribution of buried defects, we assume that defects are uniformly distributed accross the entire usable area of the mask. The 100 randomly generated spatial defect maps are considered. The main quality metric for evaluating the efficacy of defect avoidance is "mask yield," which we define as the percentage of random defect maps that are made usable (i.e., there is no impact on chip yield) by defect avoidance. We show mask yield for the different number of defects on the mask to highlight acceptable defect density levels.

We set the number of gradient descent iterations for each random point obtained from hit-and-run to 50 and the step

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size to 1 nm. We fix the number of random walk iterations as the ratio of volume of the linear spatial polytope and the volume of the multidimensional ($3L + R + C - 2$ dimensions) ball that is covered by gradient descent. The rationale behind this choice is to ensure equivalent coverage of the available space when we compare different scenarios. The volume of the linear polytope was computed using the tool VINCI,[25] and the volume of the gradient ball can be computed using a simple analytical expression.[26]

We chose the mask field size such that four rows and three columns of die copies of the Cortex M0 ARM processor can be placed inside the mask field. We allow a maximum pattern shift of 20 μm, a small-angle rotation of 6 deg and maximum allowed scribe area of 1% of the mask field size. "Scribe area" is defined as the difference in area between the total area of all the die copies inside the field pattern and the total field size ($W_F \times H_F$). Since the size of one ARM Cortex M0 layout is $162 \times 159\ \mu\text{m}^2$, the total field size becomes $486 \times 636\ \mu\text{m}^2$ and the usable area of the mask is $511 \times 662\ \mu\text{m}^2$. Note that although this is much smaller than the full-field size of $132 \times 104\ \text{mm}^2$, we have analyzed smaller layouts in order to get reasonable runtimes, especially since we perform Monte Carlo analysis over 100 random defect maps. Because our analysis is done for a small mask size, the mask yield values we report for different defect density levels in this section may not correspond to realistic values in production. Nevertheless, the analysis in this section is sufficient to evaluate the efficacy of our proposed mask defect avoidance method and compare it with prior work.

4.1 *Comparison with Other Defect Avoidance Methods*

Mask yield after defect avoidance using two prior methods is shown in Table 2. Prohibited region-based defect avoidance methods[9,12] allow continuous pattern shift and small-angle rotation but cannot handle mask floorplanning. Simulated annealing-based defect avoidance method[13] allows pattern shift and mask floorplanning, but small-angle rotation is not possible. With our implementations of both these methods, the prohibited region method performs significantly better than the simulated annealing method because the prohibited region method allows a continuous pattern shift instead of making discrete jumps. As a result, the solution space is explored more efficiently.

Table 3 shows the mask yield using our defect avoidance method, using the different degrees of freedom. Notice that even if defect avoidance is limited to pattern shift, our method performs better than both the prohibited region and simulated annealing methods. Our method performs significantly better than the prohibited region method because prohibited rectangle construction is inherently pessimistic at corners of absorber shapes, as illustrated in Fig. 5 (CD impact of defect depends to Euclidean distance from absorber edge). When pattern shift and rotation are allowed but mask floorplanning is not, our method is slightly worse than the prohibited region method because of the number of random walk iterations that we set. Given enough iterations, our method can always reach the best possible solution. More importantly, by allowing mask makers to exploit all three degrees of freedom for defect avoidance, our method allows significantly better mask yield compared to these earlier approaches. For a 40-defect mask, the mask yield of prohibited region based defect avoidance with rotation is just 11%. Our method is able to improve the mask yield to 74% in this case.

If the total number of edges in all the layout shapes is L_e, the running time complexity of all the defect avoidance

Table 2 Summary of mask yield after defect avoidance using prior methods.

Defect count	Prohibited region: Pattern shift[9]	Prohibited region: Pattern shift + rotation[12]	Simulated annealing[13]: Pattern shift	Simulated annealing[13]: Pattern shift + Mask floorplanning
10	100%	100%	100%	100%
20	81%	100%	100%	100%
30	8%	97%	0%	6%
40	1%	11%	0%	0%
50	0%	0%	0%	0%

Table 3 Summary of mask yield after our defect avoidance method with different degrees of freedom.

Defect count	Pattern shift	Pattern shift + rotation	Pattern shift+ Mask floorplanning	Pattern shift+ rotation + Mask floorplanning
10	100%	100%	100%	100%
20	100%	100%	100%	100%
30	35%	91%	55%	100%
40	3%	10%	9%	74%
50	0%	1%	2%	13%

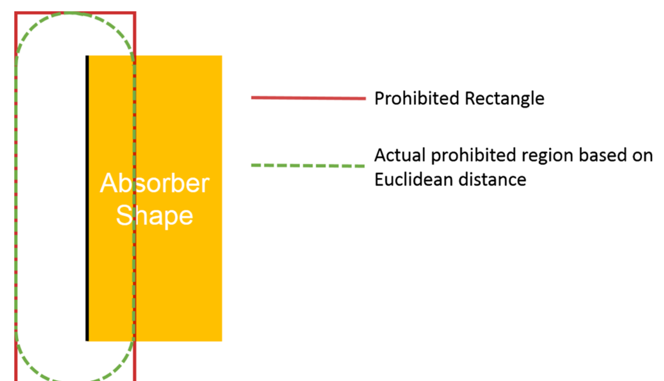

Fig. 5 Pessimism of prohibited rectangle construction compared to true prohibited region based on Euclidean distance for one absorber edge.

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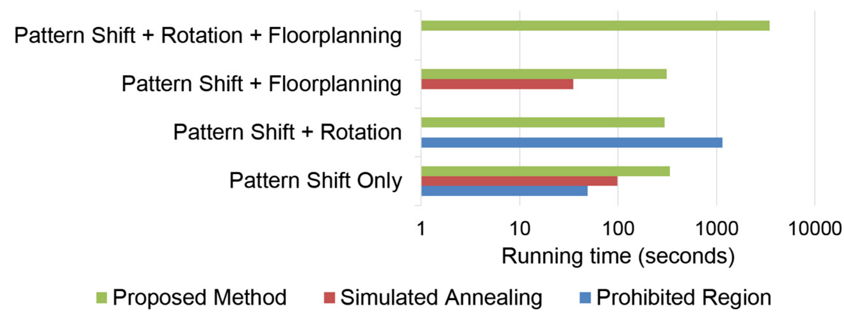

Fig. 6 Average running time of the three defect avoidance methods with different degrees of freedom for a 40-defect mask. Note that the mask yield of the different methods reported in Tables 2 and 3. Our proposed method has the largest mask yield followed by the prohibited region and simulated annealing methods, respectively.

methods we described in this section is $O[L_e \log(L_e)]$, since the running time depends on the the region query operation to obtain all the layout shapes within a rectangular box. Note that the number of queries depends on the number of defects for all the defect avoidance methods. It also depends on the number of random iterations for the simulated annealing method and our global optimization method. The average running time across all the 100 random defect maps with 40 defects that we analyzed is shown in Fig. 6. These results show that the performance of the different methods depends on the degree of freedom. If pattern shift and rotation are the two degrees of freedom that are allowed, our method is faster than the prohibited region method. However, for most other scenarios, our method does require additional computation time to achieve a better mask yield. Note that since we consider a smaller field size in this work, the reported running time is much less than the time it would take for a real full-field chip.

Although Fig. 6 may suggest that defect avoidance methods will require considerable running time for a full-field mask, there are several simple techniques that could significantly improve the running time. Our global optimization method can be easily parallelized because the gradient descent for each random starting point can be done independently. Hence, the critical region query operation can be performed in parallel which would enable signficant performance improvement. Moreover, by using a hierarchical layout, each query operation can be made significantly faster.

4.2 *Analysis for Multiple Layer Defect Avoidance*

Our earlier analysis focused on just the polysilicon layer, which is typically the most critical layer. If more layers need to be patterned using EUV lithography, defect avoidance needs to be applied for each of the corresponding masks. Although pattern shift and rotation can be done independently for each of these layers, mask floorplanning must be done together to ensure alignment.

As described in Sec. 2, our method can handle multiple layer defect avoidance as well. However, the number of variables increases by three every time an additional layer is patterned using EUV. If we were to set the number of random walk iterations based on volume of the linear polytope and gradient ball as done earlier, then the number of random walk iteration would be around 10^{10}. Since this would require considerable running time, we decided to fix the number of random walk iterations as 10^7 for all cases in this subsection. This makes the exploration of the solution space less efficient for multilayer cases.

We have summarized the results for single layer (polysilicon only), two layer (polysilicon and active) and four layer (polysilicon, active, contact and metal 1) scenarios in Fig. 7. Note that mask yield here is defined as the percentage of cases where all the layers work. Consequently, the mask yield is lower for multilayer defect avoidance. The mask yield is close to 100% for all cases when the number of defects is 30 or less. Then the mask yield for multiple layer cases reduces as we add more layers.

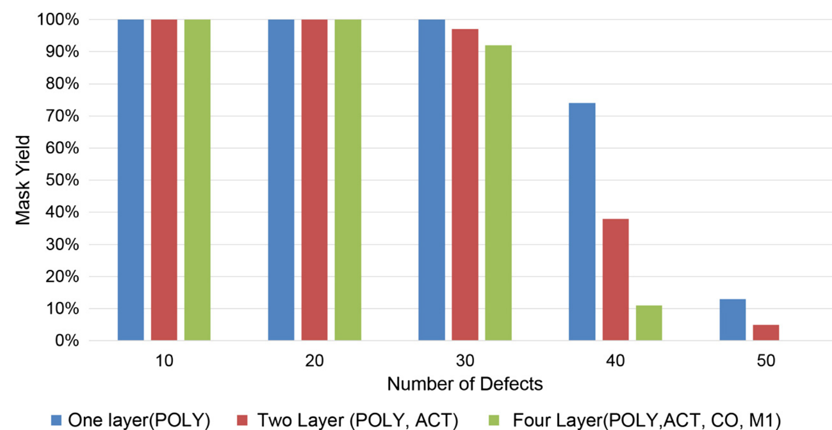

Fig. 7 Comparison of mask yield after defect avoidance when multiple layers of a design are patterned using EUV lithography.

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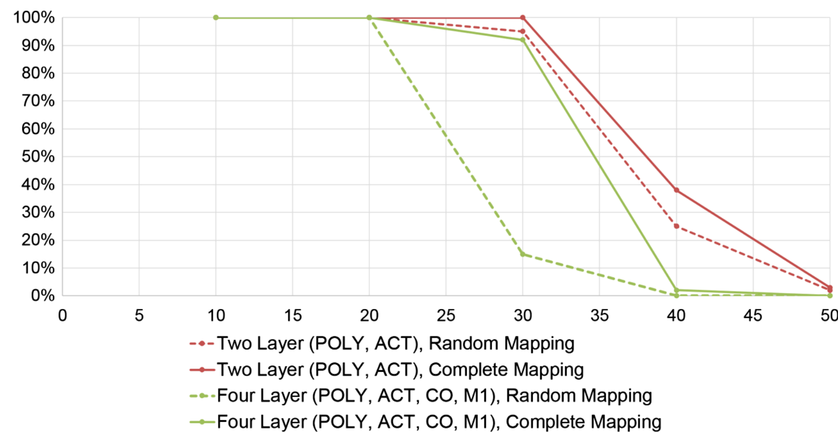

Fig. 8 Comparison of mask yield for multiple layer defect avoidance with complete blank mapping and random blank mapping.

An important concern for multilayer defect avoidance is "mask blank assignment," i.e., determining the mask blank on which each design layer should be patterned. More precisely, given L design layer and L mask blanks with known defect maps, the goal of mask blank assignment is to map each layer to one of the L mask blanks so that the best mask yield can be achieved. For the results shown in Fig. 7, we use the simple strategy of applying defect avoidance to each possible blank mapping solution and picking the mapping that works, which we refer to as "complete mapping."

Complete mapping, which is similar to the blank assignment problem explored by Du et al.,[27] requires applying defect avoidance $L!$ times, making it slow. However, it gives the best possible mask yield. Figure 8 compares complete mapping to "random mapping," where each layer is randomly assigned to a mask blank and defect avoidance is applied just once.

As confirmed by Fig. 8, blank mapping can have a huge impact on mask yield. For the four-layer defect avoidance with 30-defect mask blanks, the difference in mask yield between complete and random mapping is >70%. This is because the mask yield is limited by the regular and unidirectional polysilicon layer.[28] Complete mapping allows the critical polysilicon layer to pick one of four mask blanks, which leads to a significantly better mask yield.

4.3 *Impact of Spatial Constraints on Defect Avoidance*

There are three key manufacturing constraints (corresponding to each of the three degrees of freedom) that strongly affect the potential benefit of defect avoidance:

1. "Maximum pattern shift" is the difference between the size of usable area of mask and the size of pattern field $[(W_M - W_F) \times (H_M - H_F)$ in Eq. (1)].
2. "Maximum rotation angle" is the largest angle by which the mask blank can be rotated relative to the field pattern. It is the value of Θ_{max} in Eq. (5).
3. "Maximum scribe area" is the difference in area between the total area of all the die copies inside the field pattern and the total field size $(W_F \times H_F)$, expressed as a percentage of the total field area.

These three manufacturing constraints limit the solution space available for avoiding defects and hence can strongly affect the mask yield. We shall analyze the impact of each of these constraints in this subsection. For the sake of brevity, we shall only analyze the single layer scenario (polysilicon layer), and we will report the mask yield for 40-defect masks.

The impact of a maximum pattern shift is shown in Fig. 9. Note that all our prior analysis was done assuming a maximum pattern shift of 20 μm. Here, we look at values ranging from 10 to 100 μm. For the layout we chose to analyze, the mask yield for a 40-defect mask was 100% for pattern shift values larger than 50 μm. We also computed the volume of the linear polytope formed by all the spatial constraints of the defect avoidance optimization problem because this volume is a good indicator of the potential mask yield benefit due to the change in the size of the solution space.

Similarly, the benefit of rotation is highlighted in Fig. 10. Both the mask yield for a 40-defect mask and linear polytope volume are plotted for maximum rotation angle (Θ_{max}) ranging from 0 to 10 deg. The interesting thing to note here is that the mask yield saturates at around 80%. The reason for this is that the overall solution space does not grow due to reticle boundary constraints, which is confirmed by the polytope volume in Fig. 10.

Last, the impact of scribe area is shown in Fig. 11. Mask yield can improve up to 100% with a scribe area of 5%. However, this improvement comes at the expense of wasted space on the wafer.

4.4 *Impact of Defect Size Distribution*

We have assumed that every defect is the same size with FWHM = 50 nm and height $H = 2$ nm so far. However, in real masks, different defects will have different sizes. In this subsection, we shall assume that both the FWHM and height of every defect are independent random variables with a probability density function (PDF) as described in Eq. (17). Although there is little experimental data available on EUV mask defect size distribution, we chose this distribution since it is frequently used to model wafer defect sizes.[29]

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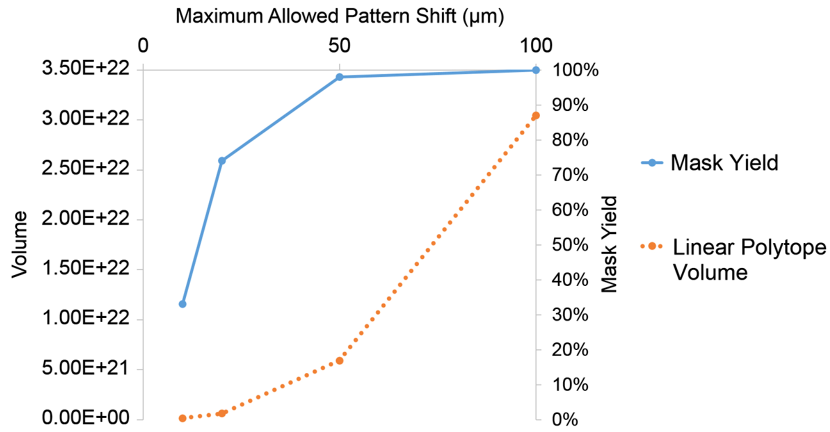

Fig. 9 Volume of linear polytope and mask yield for 40-defect mask with respect to maximum allowed pattern shift.

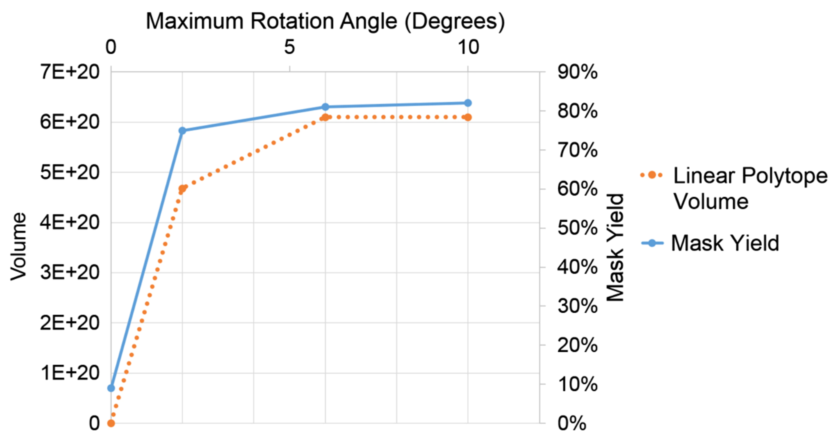

Fig. 10 Volume of linear polytope and mask yield for 40-defect mask with respect to maximum allowed rotation.

$$P(r) = \begin{cases} \frac{r}{r_0^2}, & 0 \le r \le r_0 \\ \frac{r_0^2}{r^3}, & r_0 \le r \le \infty \end{cases} \tag{17}$$

Here, r_0 is a fitted parameter based on distribution statistics, and r is a random variable that corresponds to either the height or FWHM of a defect.

Figure 12 compares the mask yield for the following three scenarios:

1. All defects have constant size with height of 2 nm and FWHM of 50 nm.
2. Height and FWHM of each defect is derived from the PDF of Eq. (17), with modes [value with maximum

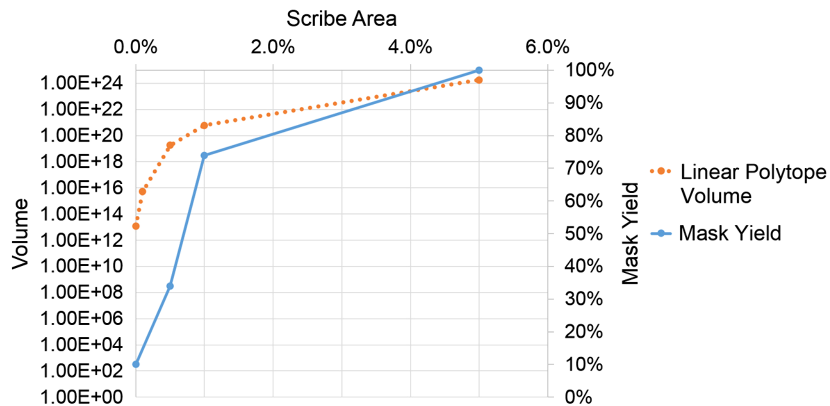

Fig. 11 Volume of linear polytope and mask yield for 40-defect mask with respect to maximum allowed scribe area.

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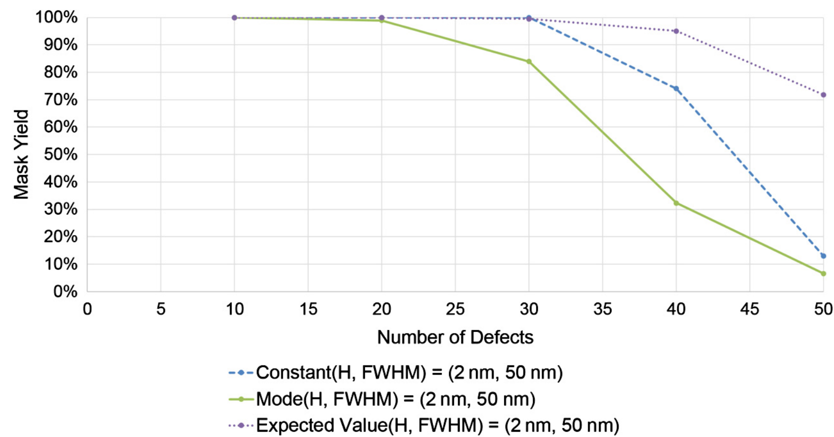

Fig. 12 Comparison of mask yield for different defect size distributions.

probability, in this case r_0] equal to 2 and 50 nm, respectively.

3. Height and FWHM of each defect is derived from the PDF of Eq. (17), withan expected value (in this case $(4/3)r_0$) equal to 2 and 50 nm, respectively.

These results show that mask yield is the lowest when the modes of the defect height and FWHM are 2 and 50 nm, respectively (Scenario 2). This is because the expected values of the defect height and FWHM are 2.67 nm and 66.7 nm, respectively, which are larger than the other two scenarios. Comparing the two cases with the same expected value of defect height and FWHM (scenarios 1 and 3), mask yield is better when the defect size is not constant. Since defect size follows the probability distribution specified in Eq. (17), most defects are smaller than the expected value and only a few are larger than the expected value. Defect avoidance is able to handle this better than constant sized defects by placing the smaller number of large defects in sparse regions of the mask field pattern.

5 Conclusion

In this work, we proposed an EUV mask defect avoidance method that can explore all the available degrees to freedom: pattern shift, rotation, and mask floorplanning. Our method can handle multiple layers of a design and explore the continuous solution space instead of discretizing it.

We modeled EUV mask defect avoidance as a global optimization problem with nonconvex objective and linear constraints. We then solved the problem using a combination of hit-and-run based random walk and gradient descent. Compared to previously proposed methods for defect avoidance, our method can significantly improve the probability of using a defective mask blank without any yield impact (mask yield), and hence our methods allow a tolerance to a larger number/size of defects than is possible with previous methods. For the polysilicon layer of a 8 nm ARM Cortex M0 layout, our defect avoidance method was able to improve mask yield by more than 60%-point compared to prior approaches for a 40-defect mask.

Using our method, we have also compared the potential mask yield benefit of each degree of freedom. Our analysis shows that pattern shift has the most impact on mask yield since increasing the maximum allowed pattern shift always improves mask yield. Rotation and mask floorplanning also help in improving mask yield, but their benefit is not as significant as pattern shift because increasing the maximum allowed rotation angle or scribe area improves the mask yield only up to a certain limit.

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