Evaluation of Digital Circuit-Level Variability in Inversion-Mode and Junctionless FinFET Technologies

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***Abstract*— In this paper, we develop an evaluation framework to assess variability in nanoscale inversion-mode (IM) and junctionless (JL) fin field-effect transistors (FinFETs) due to line edge roughness (LER) and random dopant fluctuation (RDF) for both six transistor (6T) static random access memory (SRAM) design and large-scale digital circuits. From a device-level perspective, JL FinFETs are severely impacted by process variations: up to 40% and 60% fluctuation in threshold voltage is observed from LER RDF. Conversely, results show that variability-induced shifts and broadening of timing and power in large-scale digital circuits are not significant and can be accommodated in the design budget. However, we find that LER has a large impact on static noise margin analysis of 6T SRAMs. Required V_{ccmin} values for SRAMs using JL devices reach up to 2× those implemented in conventional IM technologies. The yield for JL SRAM is completely compromised in the presence of realistic levels of LER and RDF. Fortunately, the impact of variability is somewhat reduced with scaling for JL designs; both LER and RDF induce less variation for the 15-nm node compared with the 32-nm node. The observed reduction in V_{ccmin} with technology scaling suggests that digital circuits implemented with JL FinFETs may eventually offer the same level of operability as those based on IM FinFETs, especially in the presence of circuit-level SRAM robustness optimizations.**

***Index Terms*— Circuit-level variability, fin field-effect transistor (FinFET), junctionless transistor (JL FET), line edge roughness (LER), random dopant fluctuation (RDF).**

I. Introduction

As CMOS technology devices scale ever deeper into the nanometer regime, new transistor designs are being explored to solve the fundamental issues which impede scaling. One innovation, already entering usage, is the inversion-mode (IM) fin field-effect transistor (FinFET), which addresses short channel effects (SCEs) and random dopant fluctuations (RDFs) in conventional CMOS. However, all the IM devices still require abrupt and reproducible source/drain junctions, which increase process complexity and face manufacturing limits in the nanometer scale. In response, the junctionless (JL) FET [1], [2] is proposed as a substitute for IM devices; by uniformly doping the entire device and controlling the channel potential purely electrostatically, the JL FET removes these complications of IM FET.

However, all these technologies still face the bane of process variations, which become more important with shrinking feature size, rendering device, and circuit performance increasingly unpredictable. It is well known that FinFET performance suffers from variations due to line edge or line width roughness (LER/LWR). The effect of LER on IM FinFET-based circuits is analyzed [3] with the primary impact being an increase in mean leakage power. However, JL FinFETs are inherently more sensitive to variability, with device-level simulations revealing threshold voltage standard deviations over six times those of IM FinFETs [4], [5]. In contrast to the robustness of IM devices [6], JL FinFETs are highly sensitive to RDF [4], which also impacts their drive and leakage current, and drain-induced barrier lowering (DIBL). Finally, because of reduction of gate control over the body-centered channel, JL FinFETs show worse SCE compared with IM FinFETs [7]. Therefore, it is crucial to evaluate JL variability at the circuit level to decide if JL transistors are a viable alternative to IM CMOS.

In this paper, we present the first variability-aware circuit studies of JL FinFETs in multiple technology nodes (32, 21, and 15 nm) and compare the results with IM FinFET circuits, introducing calibrated LER and RDF effects in our simulations. Both large-scale digital circuits (e.g., microprocessors) and six transistor (6T) static random access memory (SRAM) cells are evaluated using an original evaluation framework. Our results indicate that the bottleneck for JL FinFET-based circuits rests in SRAM designs needing much higher V_{ccmin} compared with IM FinFET-based circuits, whereas large-scale microprocessors are robust against stochastic variation regardless of the specific FET implementation.

II. Variability and Device Modeling

A. Overview of Evaluation Framework

The framework of our circuit-level variability evaluation is overviewed in Fig. 1. Transistor I–V characteristics and variability data from device-level technology computer-aided design (TCAD) simulations are used as the starting input for subsequent compact modeling. To create a baseline model, we fit a BSIM model based on the predictive technology model (PTM) [8] to match the TCAD I_D–V_G and I_D–V_D data. Using the method in [3] to capture the effect of LER/RDF in our compact model, model samples were generated such that

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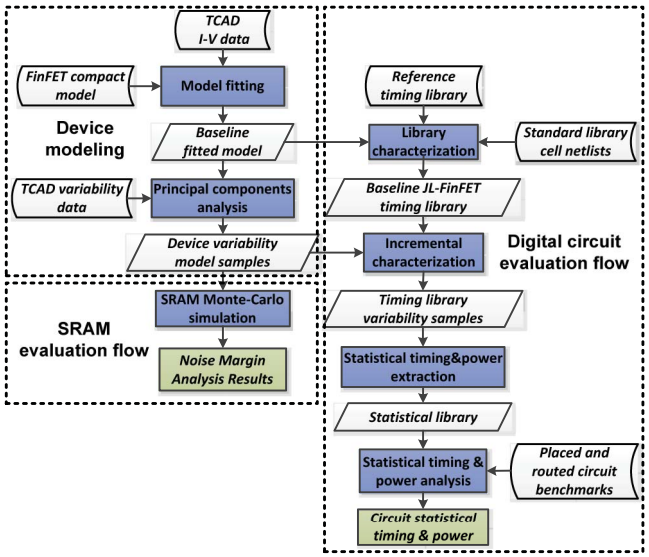

Fig. 1. Overview of the variability evaluation framework used in this paper. The evaluation of (left) 6T SRAM cells and (right) microprocessor circuits are divided into two vertical branches as illustrated.

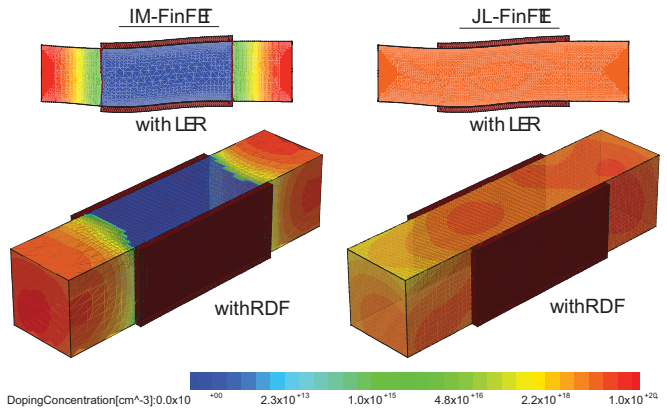

Fig. 2. Simulated 32-nm IM and junctionless FinFETs with LER and RDF. $H_{\mathrm{fin}} = 10$ nm and $\sigma_{\mathrm{LER}} = 1$ nm are used in the above structures.

their predicted behavior matches the original TCAD simulation results. 6T SRAM cell Monte Carlo simulations are performed by generating individual model samples for each of the six transistors, after which the static noise margins extracted. For logic circuit timing and power analysis, we first create and characterize a baseline timing library from a baseline model and template library. Then, through incremental characterization based on model samples, library samples are generated such that the resulting circuit behavior should correctly reflect the performance impact from LER/RDF. Statistical timing and power information is extracted from these library samples, which are then fed as inputs to a computationally efficient statistical timing and power analyses tool based on [9], [10] to evaluate the overall impact of LER/RDF on large-scale digital circuit delay and power consumption. The following sections explain the individual stages of our framework in more detail.

B. LER and RDF Modeling

To introduce the effect of LER in our FETs, we first generate 200 random LER patterns with root-mean-square roughness amplitude σ_{LER} up to 0.6 nm and correlation length $\lambda = 15$ nm using the method of Fourier synthesis [11] with a Gaussian autocorrelation function. These values represent typical LER values which may be required by industry heading beyond 32-nm technology, based on the 2011 ITRS [12] forecast and experimental data [11]. We fixed the correlation length $\lambda = 15$ nm as previous studies [13], [14] have shown that the effect of λ diminishes as $\lambda >$ 15–20 nm, and some experimental data has shown that current values of λ are estimated between 20–30 nm [11] and generally reduces with technology, suggesting $\lambda = 15$ nm as a reasonable estimate for sub-32-nm lithography.

The LER patterns are then used as templates to augment the fin sidewalls in our double-gate FinFET structures as shown in Fig. 2, thus yielding random performance for individual devices. Here, each FinFET technology was designed according to the ITRS forecast for 32, 21, and 15-nm high-performance logic nodes with specific details provided in [5]. Only fin LER along the channel transport direction was considered in this paper for reasons described in [3] and [5]. In addition, we assume all line edges to be uncorrelated within individual devices as well as between devices hence the LWR amplitude $\sigma_{\mathrm{LWR}} = 2^{1/2}\sigma_{\mathrm{LER}}$; this represents the situation of standard resist patterning. The effects of spacer patterning are not explicitly dealt here with the understanding that the device- and circuit-level LER impact will likely be minimal [3], even for JL FinFETs.

The impact of RDF was captured using the same approach in [4] which randomizes the placement and concentration of ionized dopants based on a Poisson distribution. The locally varying doping concentration is calculated from the long-range part of the Coulomb potential with an appropriate screening length [15]. Because of the high doping concentration and small device volumes in our JL FinFETs, the variability impact of RDF is significant from a device-level perspective. This contrasts with the situation for IM FinFETs where the channel is typically undoped and RDF only exists in the source and drain extensions Fig. 2. For JL FinFETs, a nominal doping level of $N_D = 2 \times 10^{19}$ cm^{-3} yields optimal performance in terms of I_{ON} for a given I_{OFF} (≤ 100 nA/μm) while satisfying ITRS design specifications. We found that higher doping levels (e.g., $N_D = 3 \times 10^{19}$ cm^{-3}) result in slightly worse nominal performance as well as heightened variability, while lower doping levels (e.g., $N_D = 5 \times 10^{18}$ cm^{-3}) result in even higher I_{ON} penalties (20%–40%), but reduced variability. We also find that any channel doping lower (higher) than roughly 1×10^{19} cm^{-3} results in accumulation-mode (depletion-mode) behavior for the device geometries considered. With this in mind, the performance versus variability tradeoff for JL technologies may be a critical factor for the optimal design of such devices, and further work will be needed to identify the best strategy for JL FET design (beyond current ITRS guidelines). Unfortunately, such an investigation is beyond the scope of this paper and the remainder of our study will employ FinFETs designs [5] which best match the nominal scaling guideline published by the ITRS.

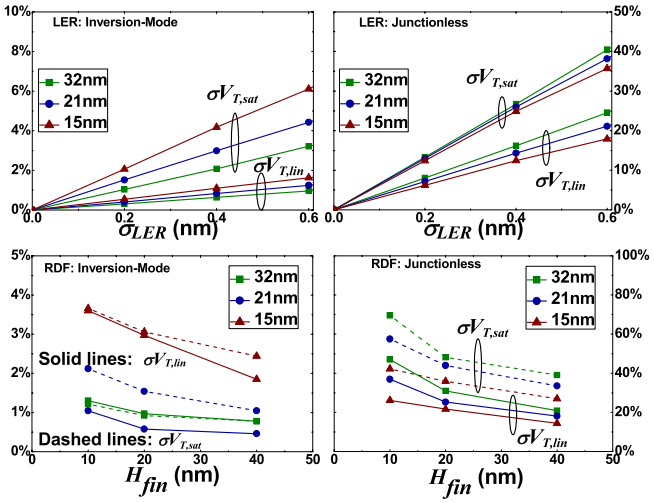

Fig. 3. Threshold voltage variation of IM and junctionless FinFETs due to LER (upper row) or RDF (bottom row). Only one source of variability (LER or RDF) is active at a time. Note the scale for JL FinFETs is larger than that for IM FinFETs.

C. Device-Level Variability

We previously quantified the variability impact of LER and RDF for sub-32-nm IM and JL FinFET technologies in [3]–[5] using 2-D and 3-D TCAD simulations for LER and RDF, respectively. In those simulations, quantum corrections are modeled using the density gradient approxima-tion, high-field transport with a calibrated hydrodynamic model [3], [16], and carrier mobility with doping dependent, surface scattering, and high-field terms. A small subset of our results is shown in Fig. 3, comparing the threshold voltage variability of IM and JL FinFETs due to LER and RDF. JL devices (with $N_D = 2 \times 10^{19}$ cm^{-3}) exhibit significantly higher variability com-pared with similarly designed IM devices. In fact, some JL devices within a $\pm 3\sigma$ spread may have a negative V_T (peak $3\sigma V_{T,\mathrm{sat}} > 100\%$) and be permanently on even at zero gate voltage, constituting switching failure; this may occur due to a surplus of dopants inside the channel from RDF or an unusually wide fin from LER. This revelation is due to the different methods by which LER and RDF affect the intrinsic operation of IM versus depletion-mode FETs [5]. Similar conclusions are obtained for other performance metrics including σI_{ON}, σI_{OFF}, σSS, and σDIBL; data is available in the listed references. With these device-level variability figures, we determine the resulting circuit-level impact in Sections III and IV.

As mentioned in the previous section, we found that JL-FinFETs with lower (higher) doping resulted in less (more) overall variability from LER and RDF. For 32-nm JL-FinFETs with $N_D = 5 \times 10^{18}$ (3×10^{19}) cm^{-3}, LER-induced $\sigma V_{T,\mathrm{sat}}$ drops (rises) to 12% (60%) at $\sigma_{\mathrm{LER}} = 0.6$ nm. Similar changes in JL variability from LER are witnessed for other technology nodes and performance figures as well, suggesting the viability of JL technology will depend on the design strategy employed. A full set of results for RDF-induced variability is not available at this time, but preliminary findings suggest similar trends when the baseline doping is changed.

TABLE I
ALLOWED TUNING RANGE OF FITTED COMPACT MODEL PARAMETERS

Param.	Range	Param.	Range	Param.	Range
nch	0.1–10x	len	0.7–1.6x	tox	0.7–1.6x
tsi	0.5–2x	tbox	0.5–2x	vth0(f)[1]	±0.25 V
vth0(b)[1]	±0.25 V	esi[1]	0.8–1.4x	eox[1]	0.8–1.4x
Lambda	0.5–2x	N1	0.9–1.1x	Vt[1]	±0.25 V
voff1[1]	±0.1 V	u0	0.7–1.6x	eta0	±0.1
dsub	±0.1 V	rdsw	0.7–1.6x		

[1]Parameters in PTM model.

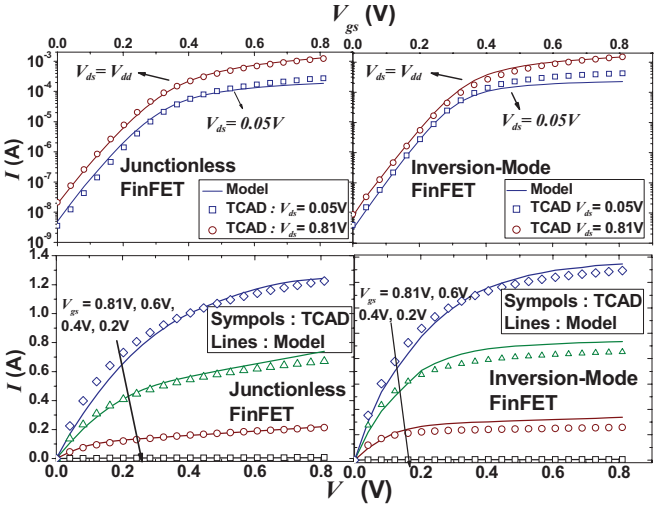

Fig. 4. Matching of baseline FinFET (a) transfer and (b) output curves between TCAD simulation and compact modeling.

D. Device and Variability Model Fitting

PTM FinFET models [8] are fitted to the TCAD-simulated transfer and output characteristics. To match the currents from the 2-D TCAD simulations (in units of A/μm) to the 3-D device model, we linearly scale the currents to match single fin transistor characteristics, where we assume H_{fin} to be equal to the feature size in each technology node (e.g., $H_{\mathrm{fin}} = 32$ nm for 32-nm FinFETs). Seventeen parameters of the PTM model are chosen as fitting variables according to the PTM and BSIM parameter extraction guide [8], [17], with tuning ranges for each chosen parameter listed in Table I. Our error metric for the fitting procedure is the weighted least square difference between the simulated and model I_D–V_{GS} and I_D–V_{DS} curves, with random starts and gradient descent methods being applied. Good matching between the compact models against TCAD simulations are obtained, as shown in Fig. 4.

With the baseline compact model established, the base-line cell library is characterized using Nangate Open Cell Library [18] as the template, similar to [3]. Extraction of device-level variability is based on principle component analy-sis [3], [19], [20]. The model samples are generated [3] hence the resulting device performance variation matches the data from TCAD simulations. The statistical matching results are shown in Fig. 5. Standard deviations of I_{ON} and $V_{T,\mathrm{sat}}$ are calculated from 400 model samples. The maximum error is

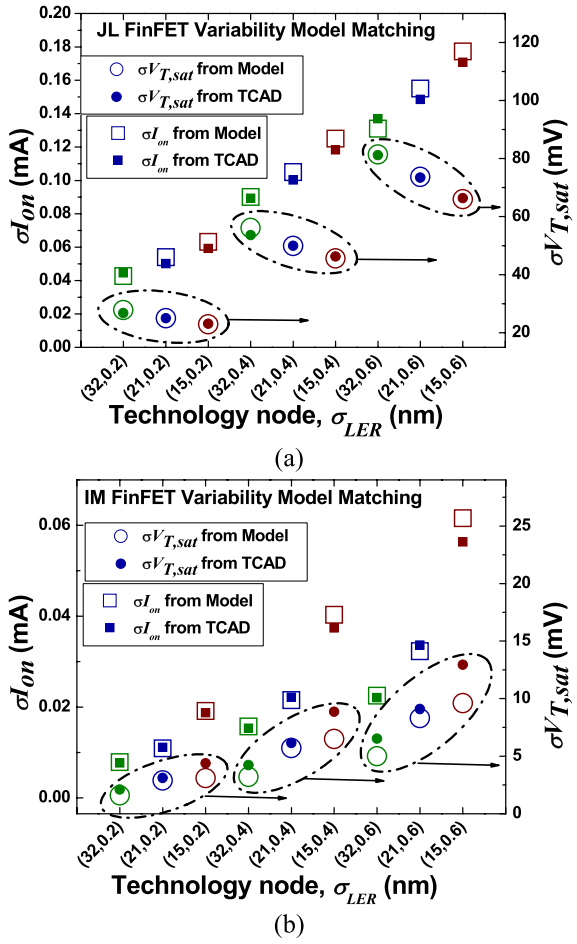

Fig. 5. Comparison of σI_{ON} and $\sigma V_{T,\mathrm{sat}}$ extracted from 200 samples between TCAD simulations and fitted variability models for (a) JL FinFETs and (b) IM FinFETs show a good fit.

only 8.2% in σI_{ON} for JL FinFETs, validating our JL FinFET circuit model. Unfortunately, when matching $\sigma V_{T,\mathrm{sat}}$ for 15-nm IM FinFETs, a maximum error of 25.8% is observed for $\sigma_{\mathrm{LER}} = 0.6$ nm; however, since variation has very limited impact on IM FinFETs, we find that this relatively large matching error does not change our conclusions. For both IM and JL FinFETs, σI_{ON} increases with technology scaling whereas $\sigma V_{T,\mathrm{sat}}$ increases (decreases) in IM (JL) FinFETs. This unexpected trend for $\sigma V_{T,\mathrm{sat}}$ was also reported in [4] and [6], and can be explained by noting that smaller nodes with thinner bodies helps suppress the effects of LER/RDF due to the closer gate-to-channel proximity in JL devices with buried channels [1]. For IM devices with surface channels, the gate-to-channel proximity is relatively insensitive to the body thickness and, therefore, the effects of LER/RDF are not suppressed at smaller technologies (they are only degraded from SCE).

III. Variability Impact on 6T SRAM Memory

A. Baseline Nominal Static Noise Margin

As CMOS technology continues to scale down, SRAM design becomes progressively more complicated. To guarantee proper operation, the cell design must meet noise margin

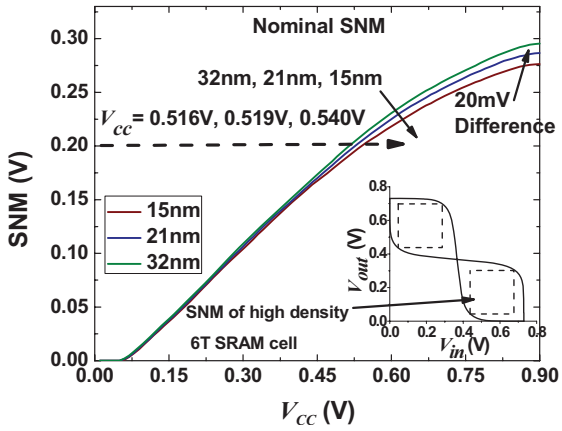

Fig. 6. Nominal SNM as a function of working V_{cc} for high density design JL FinFET 6T SRAM cells. Note that for successive technology nodes, SNM and $V_{cc,min}$ decrease when the other is held fixed.

requirements that are budgeted for all fluctuation sources, including supply, process, and temperature variations. Increasing variability therefore, strongly degrades performance. For instance, static noise margin (SNM), one of the important metrics for SRAM cell stability, decreases with successive technology generations [21]. Fig. 6 shows how nominal SNM changes with supply V_{cc} from 32 to 15 nm for JL FinFET 6T SRAM. With increasing V_{cc}, the SNM diverges for different technologies with differences of up to 20 mV at $V_{cc} = 0.9$ V.

In addition to these generic challenges, FinFETs face an additional disadvantage because of their digitized fin structures. Traditionally, device widths are sized to achieve high stability; for example, symmetric (SYM) designs might continuously scale PMOS widths to be larger size than NMOS to equalize the drive current. Realizing this with FinFETs requires parallelizing fins at the cost of cell area, for instance matching three PMOS with two NMOS fins; instead, typical designs now use one fin for each gate to maximize density [22], [23]. In the following discussion, all SRAM results are generated based on this high density (HD) layout unless otherwise specified.

B. Minimum Working V_{cc} (V_{ccmin})

As cell density increases, power consumption becomes a crucial consideration requiring reduction of V_{cc} to conserve both dynamic and leakage power. The minimum working supply voltage V_{ccmin} is thus an important metric for judging the viability of a cell design. In general, for a fixed SNM, V_{ccmin} increases with scaling. Fig. 6 shows for instance how enforcing SNM of 0.2 V causes V_{ccmin} to increase from 0.516 V at the 32-nm node to 0.540 V at 15 nm. In addition to SNM, static/dynamic read and write noise margins also affect V_{ccmin}; however, considering all such metrics would raise many more design issues outside the scope of this paper. Therefore, we will only consider the effect of SNM on V_{ccmin}.

We use Monte Carlo simulations to search for V_{ccmin} underspecified yield and SNM constraints. HSPICE is used for dc simulations of 6T SRAM cells where each individual device is independent and uses a randomly selected device model, as explained in Section II-D. The SNM is measured as

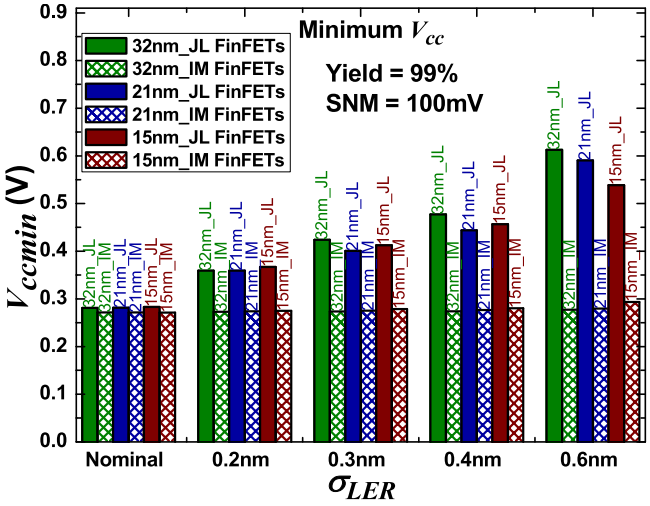

Fig. 7. V_{ccmin} as a function of technology node and LER amplitude for JL and IM FinFET 6T SRAM. The SNM constraint is 100 mV, and yield is 99%.

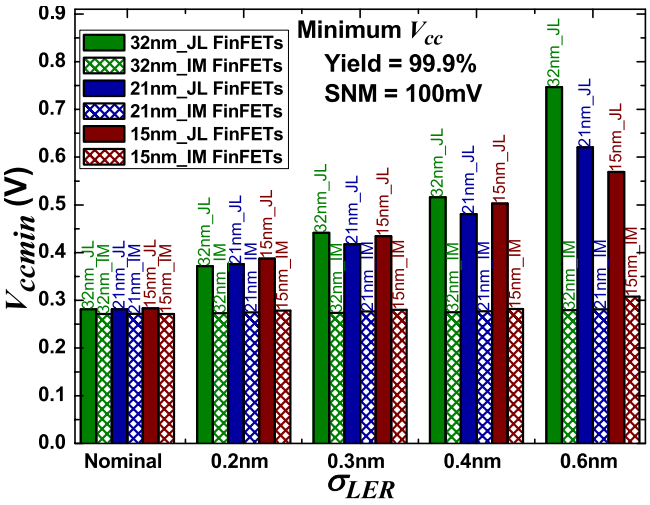

Fig. 8. V_{ccmin} as a function of technology node and LER amplitude for JL and IM FinFET 6T SRAM. The SNM constraint is 50 mV, and yield is 99.9%.

the length of the largest square in the butterfly curve, as shown in the inset Dof Fig. 6. A simulated cell with SNM below the given constraint counts as a failed cell. A given supply voltage is said to work for SRAM cells if the number of successful simulations with this V_{cc} reaches the yield requirement (e.g., 99.9% yield requires 9990 successful simulated cells out of 10,000 randomly generated cells). To find the V_{ccmin}, we use a binary search (40× faster than exhaustive search). To further improve the runtime of yield analysis, we use the statistical blockade method [24] which uses rejection sampling, speeding up the total process by over 10×.

In Fig. 7, V_{ccmin} is reported for JL and IM SRAM cells with different technology nodes and LER amplitudes. The improved V_{ccmin} for IM-based SRAM compared with JL-based SRAM is explained by the fact that IM devices are more robust against LER-induced variability [5]. This shows that JL transistors in current technology nodes would not be a good option for memory design. Interestingly for JL technologies, at low LER amplitudes the 32-nm devices perform best, whereas at high LER amplitudes the trend is reversed and

TABLE II
NOMINAL SNM AND SNM LOSS FROM VARIABILITY FOR JL FINFET TECHNOLOGIES

	32 nm		21 nm		15 nm	
	HD[1]	SYM[2]	HD	SYM	HD	SYM
Nominal SNM[3] [V]	0.264	0.268	0.26	0.262	0.251	0.252
SNM w/ variation[4] [V]	0.128	0.154	0.144	0.166	0.14	0.176
% SNM loss	51.50%	42.50%	44.60%	36.60%	44.20%	30.20%

[1] High density 6T SRAM design

[2] Symmetric N/P design

[3] SNM at $V_{cc} = 0.73$ V

[4] SNM with 99% yield constraint; LER variation ($\sigma_{\text{LER}} = 0.6$ nm) at $V_{cc} = 0.73$ V

the newest generation (15 nm) devices have the lowest V_{ccmin}. This trend is more obvious in Fig. 8, where the more stringent requirement of 99.9% yield exacerbates the effect of variations on SNM.

This trend can be understood by remembering that V_{ccmin} is dictated by both variability and the nominal SNM. We have already seen that nominal SNM degrades under size scaling and dominates the trends in Figs. 7 and 8 at small σ_{LER}, but JL devices also become less sensitive to variability as technology scales [5], allowing the operating conditions to relax. Our largest considered σ_{LER} of 0.6 nm is in line with the ITRS-projected σ_{LER} requirements of 1, 0.8, and 0.5 nm for the 32, 21, and 15-nm nodes, respectively. Therefore our results hold out hope that for realistic variability levels, JL SRAM technologies will become more competitive if scaling trends continue.

C. SNM Versus Technology

We also explored SYM SRAM designs using three PMOS with two NMOS fins, which can optimize nominal SNM and mitigate the effects of variability due to statistical averaging over the multiple fins. To characterize the impact of variability on the design, we define SNM loss as the percentage difference between the nominal SNM and the variability-affected SNM. Table II compares SNM loss for JL HD and SYM cells. We find as expected that under scaling and/or use of SYM designs, SNM loss is significantly reduced. On the other hand, the SYM design sacrifices read noise margin and cell area.

To better understand the impact of process variability on JL FinFETs, we also attempted to incorporate both RDF and LER effects in our simulations, assuming the fluctuations to be uncorrelated. This assumption of statistical independence may not be strictly justified, but forms a best-case scenario for real-world situations. Even under this relaxed assumption, we find that no realistic V_{ccmin} can be realized for 99% yield and 100-mV SNM, reinforcing our conclusion that process variations will be a serious roadblock for JL FinFETs in memory applications.

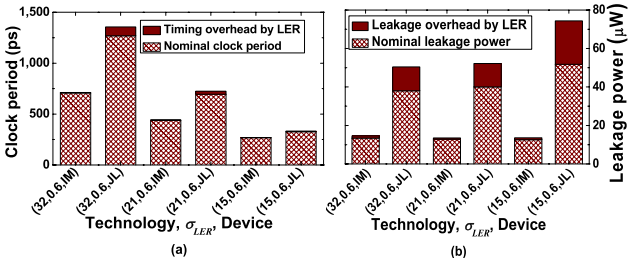

Fig. 9. (a) Nominal clock period and clock period increase (mean shift and variation) and (b) nominal leakage power and leakage power increase (mean shift and variation) due to LER variation ($\sigma_{\mathrm{LER}} = 0.6$ nm) for IM and JL FinFET-based MIPS processors at typical clock speeds.

IV. LER Impact on Logic Circuit Variability

Although variability in JL FinFETs has a large impact at the device and cell level, large-scale circuits can mitigate and av-erage out uncorrelated fluctuations. Analyses using closed-form analytical equations have shown how the number of gates and paths can decrease the overall circuit timing and power variations for conventional CMOS technologies [25]–[27]. We extend our methodology to analyze the usage of JL devices at the microprocessor level.

A. Overview

A typical way to analyze the statistical timing and power of circuit benchmarks uses a large number of library samples based on the Monte Carlo method [3]. However, this method is time-consuming and results in roundoff errors when synthesizing tool outputs, losing statistical information. To fix these errors, more simulations are needed, with the quantity dependent on the size of the variability impact. In this paper, we use block-based statistical timing and leakage analysis [9], [10] to complete this step, drastically improving computational efficiency; in some cases, simulations that would previously require weeks of computation can be reduced to several tens of seconds.

B. Circuit Statistical Timing and Power Analysis

To build the input to the statistical timer, the timing and leakage standard deviation for cells need to be extracted from library samples (we use 200 library samples in this step). We observe that timing variation is highly sensitive to input slew and output load capacitance. Hence, to find accurate timing variation information, a cubic model of delay standard deviation as a function of load capacitance and input slew is fitted to statistical timing information extracted from library samples. This model is found to be accurate enough for the following analyses. Leakage variation is modeled as a lognormal distribution with the standard deviation and mean extracted from the library samples.

The input to the statistical timer includes extracted timing models, extracted leakage lognormal standard deviations, a synthesized and routed circuit benchmark, the baseline library, timing constraints, and SPEF file containing parasitic information. For our benchmarking we select two processors, MIPS [28] and CortexM0 [29]. To cover all working applications, we synthesize them in three operating clock frequencies for fast, typical, and slow speeds as shown in Table III.

TABLE III
Circuit Benchmarks

Tech. node	Freq. for CortexM0 [GHz]			Freq. for MIPS [GHz]		
	Fast	Typ	Slow	Fast	Typ	Slow
32 nm	0.92	0.79	0.7	1.02	0.79	0.75
21 nm	1.47	1.3	1.12	1.61	1.44	1.09
15 nm	2.29	2.23	1.85	3.29	3.07	2.04

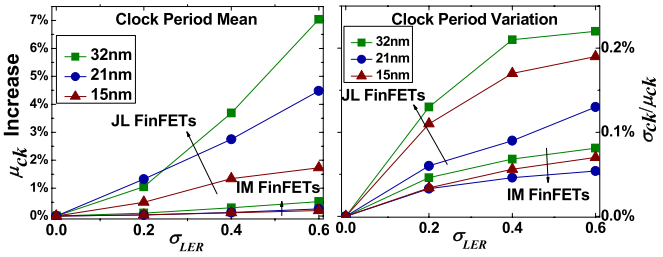

Fig. 10. (a) Increase in clock period mean and (b) variation of critical clock period as a function of technology node and LER amplitude for JL and IM FinFET circuit benchmark (Cortex M0).

C. Circuit Simulation Results

Fig. 9 shows our results for MIPS designs. The clock period increase due to device variability is calculated as the sum of mean shift and delay uncertainty (3 σ_{clock}), covering around 99.9% of the possible clock period cases. All uncertainty in our timing results is below 1.20% of nominal delay. The mean clock period shift contributes the most; the highest mean shift is 7.04%. Thus, a delay margin of up to 8.2% may be needed to guarantee sufficient yield in the presence of LER. JL-based processors show a greater improvement in nominal speed with scaling compared with IM-based circuits.

The leakage power is assumed to follow a lognormal distribution. The uncertainty is calculated based on [10] at 99.9% yield point of leakage cases. Leakage increase is the sum of the mean shift and leakage uncertainty. As shown in Fig. 9(b), leakage power is severely impacted by LER. Our results show the increase mainly comes from a mean shift, in which the highest observed shift value is 43.02% of the nominal leakage. Leakage uncertainty has a considerable impact, inducing up to 15.57% increase. However, we expect that the leakage uncertainty will be negligible in industrial-scale designs (random leakage variation averages over number of devices in the design). High leakage variations are also predicted by device level simulations, where σI_{OFF} is over 10× nominal leakage for individual JL FinFETs [5].

Figs. 10 and 11 show the JL-based high speed Cortex-M0 results for clock period mean and leakage mean compared with IM-based processors [3]. JL devices are more severely affected by variability in terms of both mean shift and standard deviation, with circuit clock period mean shift over 10× that of IM FinFETs. Table IV shows the average results from all six circuit benchmarks. For example, at $\sigma_{\mathrm{LER}} = 0.6$ nm (near the

TABLE IV
AVERAGE MEAN SHIFT AND STANDARD DEVIATION OF TIMING AND LEAKAGE FOR SIX BENCHMARK CIRCUITS

Node	σ_{LER} [nm]	Timing		Leakage	
		μ_{delay}	σ_{delay}	$\mu_{leakage}$	$\sigma_{leakage}$
32 nm	0.2	1.01%	0.12%	1.4%	0.2%
	0.4	2.56%	0.17%	12.6%	0.6%
	0.6	4.44%	0.22%	26.2%	1.0%
21 nm	0.2	1.26%	0.13%	1.7%	0.2%
	0.4	2.30%	0.20%	9.6%	0.5%
	0.6	3.62%	0.27%	25.3%	0.9%
15 nm	0.2	0.70%	0.17%	0.6%	0.1%
	0.4	1.32%	0.25%	6.8%	0.4%
	0.6	1.60%	0.28%	36.8%	1.1%

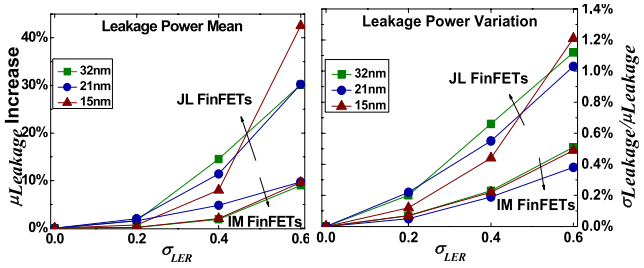

Fig. 11. (a) Increase in leakage power mean and (b) variation of leakage power as a function of technology node and LER amplitude for JL and IM FinFET circuit benchmarks (Cortex M0).

ITRS predicted LER requirement of 0.5 nm), a 36.8% leakage mean increase is observed at the 15-nm node. However, these impacts are not severe at the logic circuit level.

We have simulated the combined effects of RDF and LER variability, but the huge variations encountered (e.g., normalized $\sigma V_{T,sat} = 70\%$) can lead to statistically significant failure rates in SPICE convergence. Therefore these results are not presented. However, as previously observed [25]–[27], the mean increase of timing variations for circuits is linearly related to the variation of a single logic gate. We can estimate the combined variability to have 3× impact on timing compared with our results considering only LER. For leakage power, a model-based analysis [10] using our library extraction results shows the effects of combined variability will have 2× impact on leakage mean compared with the standalone LER variations.

V. CONCLUSION

Device-level TCAD simulation showed that JL FinFETs were more susceptible to process variability (LER and RDF) than IM FinFETs. Fluctuation in threshold voltage reached up to 40% and 60% due to LER and RDF, respectively. The large-scale digital circuit benchmarks showed LER induces <10% mean shift in timing and below 1% standard deviation over the nominal clock period. Leakage power mean shift up to 43% with standard deviation <2% (i.e., following lognormal distribution) was observed. The results suggested that large-scale digital circuits will not be affected much by LER-induced variability and that manageable timing and power margins may resolve the issue. However, for memory cells which had fewer transistors, the large degree of device fluctuation resulted in a stronger circuit-level impact. Under the LER target reported by the 2011 ITRS, JL FinFET SRAMs required twice the $V_{\rm ccmin}$ compared with IM FinFET SRAMs. After considering LER and RDF combined variability, JL FinFETs totally fail to produce yields higher than 99%. Fortunately, technology scaling alleviates the effect of LER and RDF variability, with JL FinFET SRAMs at the 15-nm node achieving better noise margin and V_{ccmin} compared with the 32-nm node. On the other hand, IM FinFET SRAMs became more vulnerable going from 32 to 15 nm. This suggested that JL FET technology may eventually become a viable solution in future digital logic generations, especially if circuit-level memory robustness enhancement solutions were considered.

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