Design-Aware Defect-Avoidance Floorplanning of EUV Masks

Abde Ali Kagalwalla, *Student Member, IEEE*, and Puneet Gupta, *Member, IEEE*

***Abstract*—Fabricating defect-free mask blanks remains a major obstacle for the adoption of EUV lithography. We propose a simulated annealing based gridded floorplanner for single project, multiple die reticles that minimizes the design impact of buried defects. Our results show a substantial improvement in mask yield with this approach. For a 60-defect mask, our approach can improve the mask yield from 0% to 26%. If additional design information is available, it can be exploited for more accurate yield computation and further improvement in mask yield to 99.6%. These improvements are achieved with a limited area overhead of less than 0.2% on the exposure field. Our simulation results also indicate that around $10\%-30\%$ mask yield improvement is possible as a result of floorplanning compared to shifting the entire mask pattern. Our floorplanner can tolerate a defect position error (due to mask blank inspection tools) of $0.25\mu m$ with just a 2% reduction in yield. The impact of defect dimensions and multi-layer EUV patterning on the viability of floorplanning is also analyzed in this work.**

***Index Terms*—EUV, Mask Defects, Buried Defects, DFM, CAD, Mask Manufacturing, Mask Floorplanning, Reticle Floorplanning, Semiconductor Manufacturing.**

I. Introduction

Extreme ultraviolet (EUV) lithography is considered one of the most promising next-generation lithography solutions to replace the current deep ultraviolet (DUV) lithography [1]. But the technology still faces several challenges before it can actually be used for volume production. In addition to source and resist, fabricating defect-free mask blanks remains one of the major challenges that could delay the adoption of EUV lithography [2].

High energy ultraviolet light used in EUV lithography is absorbed by all materials, which prevents the use of refractive optics like DUV. As a consequence, EUV optics is reflective. Creating reflective masks or mirrors for EUV uses the principle of Bragg reflectors, which rely on constructive interference at the interface of materials with different absorbtion rates. EUV mask blanks are constructed by stacking several molybdenum-silicon bilayer reflectors which can achieve a reflectivity of approximately 70%. The layout patterns that need to be printed on wafer are then written on the multilayer mask blank as an absorber layer.

A key problem associated with the fabrication of these multilayer EUV mask blanks is buried defects. These defects can propogate to the top of the multilayer stack as a bump on the surface causing the path of the reflected EUV light to change. Even a $3.5nm$ tall buried phase defect can easily print on the wafer, causing a massive critical dimension (CD) change of $20nm$ on the wafer [3]. Figure 1 illustrates the potential damage that a buried defect can cause by shorting two parallel lines.

Buried defects are caused by pits on the substrate surface, or particles that get introduced either on the substrate surface or during multi-layer deposition. Around 75% of defects are caused due to substrate defects [4]. Current technology has enabled mask makers to reduce the density of buried defects down to 0.005 defects$/cm^2$ for defects wider than $53nm$ [4]. But these figures may be optimistic since most current generation mask inspection tools miss several printable buried defects [5]. Although these defects can be partially repaired using an e-beam tool, there is considerable risk of damaging the multi-layer structure [6]. Because of these issues, it might not be feasible to produce defect-free EUV mask blanks at a reasonable cost.

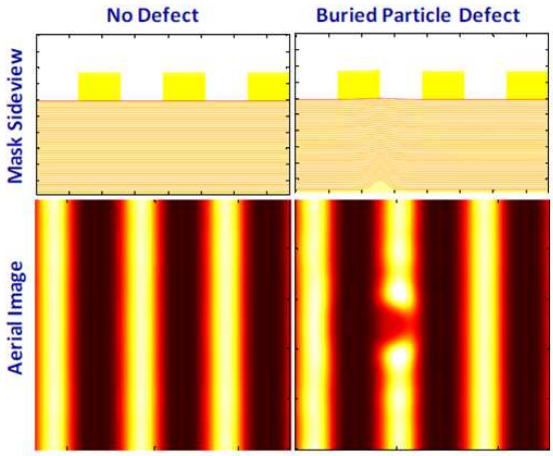


Fig. 1. EUV masks along with the aerial image illustrating the impact of buried defects [7].

A. EUV Defect Mitigation Approaches

Due to the defective and hard-to-repair nature of EUV mask blanks, the ability to tolerate some of these defects without any impact on yield is an attractive proposition. Recently, several techniques have been proposed to mitigate these buried defects in EUV masks. Buried defect mitigation techniques can be applied either before patterning the mask blank or after mask writing. In this section, we offer a brief survey of some of these approaches.

This work was supported by the generous support of IMPACT UC Discovery Grant and NSF CAREER award number 0846196.

Abde Ali Kagalwalla and Puneet Gupta are with the Department of Electrical Engineering, University of California, Los Angeles.

The basic premise of compensating for EUV mask defects after mask writing relies on comparing the aerial image of the patterned mask to the target pattern. Any significant critical dimension (CD) changes that are caused by a buried defect can be compensated for by removing some absorber material using a repair tool [8]. Note that this mask repair step is significantly less complicated than repairing the multilayer stack, which we mentioned earlier. Clifford et. al. [7] demonstrated a simple notch shaped absorber removal compensation technique. Unfortunately such mask repair approaches are limited due to their inability to repair large defects or work with focus variation [9]. More complicated repair approaches include using a fast defect printability simulator iteratively to modify the absorber patterns based on the thresholded difference between target and simulated images [10], or using conventional computational lithography based approaches such as proximity correction or inverse lithography [11], [12]. These approaches are also known to not work well in the presence of defocus variation. In addition to this, the tedious process of repairing each defect separately may make this approach infeasible for production.

The second class of approaches that can be used to mitigate buried defects require the inspection of the mask blanks to find the position and dimensions of defects before patterning. This information can then be exploited to adapt the design layout pattern before it is written on the mask. This can be done by using the same absorber compensation based techniques we mentioned above for post-write mask repair. An alternative, less intrusive solution would be to shift the location of the layout pattern relative to the mask coordinates. This option, first suggested by Yan [13], is viable since the usable area on a mask blank is typically larger than the standard field size of $104mm \times 132mm$, as illustrated in Figure 2. Burns et. al. [14] proposed a simple enumerative technique to move the entire mask pattern to cover defects with absorbers. A more efficient approach for pattern shifting, based on prohibited rectangle construction, has been proposed recently by Zhang et. al. [15]. The potential benefits of such pattern shift approaches to avoid buried defects have been explored recently by Gallagher et. al. [16] and Yan et. al. [17].

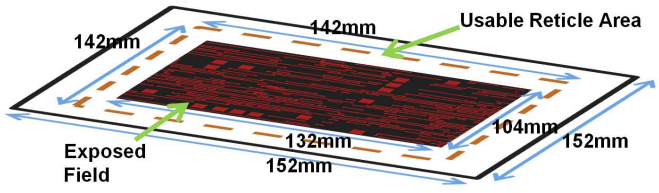


Fig. 2. Standard EUV mask form factor with dimensions obtained from SEMATECH [18].

In this work, we propose a novel floorplanning based approach that allows greater flexibility compared to shifting the entire mask pattern. Since most commercial masks contain patterns for multiple die copies, floorplanning allows additional degrees of freedom for improving mask yield with a limited overhead of wasting some scribe line space on the wafer. One important point to note here is that the solution set of an optimal pattern shift based approach is a subset of an optimal floorplanner's solution space. If the field exposure area of the mask cannot accomodate more than one die, floorplanning becomes equivalent to shifting the entire mask pattern. An alternative formulation of floorplanning that attempts to maximize the number of dies that can be safely placed on the reticle has been proposed recently by Du et. al. [19].

Although pattern shift or floorplanning may allow us to mitigate bigger defects for a larger process window compared to repair based approaches, a significant limitation is the need for accurate mask blank inspection. Current mask blank inspection tools suffer from serious limitations as they miss several printable defects and the error in reported defect position is large [5]. Hence, the applicability of any pre-mask patterning compensation relies on the improvement of blank inspection tools.

B. Our Work

This work is an extension of our earlier conference work [20]. The key contributions of this work are as follows:

- We propose a comprehensive simulated annealing based reticle floorplanning algorithm that can help alleviate the problem of buried defects in EUV masks. To the best of our knowledge, this is the first work on reticle floorplanning for EUV masks. The floorplanner can also utilize design information in the form of different tolerable CD change for each absorber shape.
- Several improvements were made to the floorplanning methodology we proposed in [20]. Instead of starting floorplanning by placing the mask pattern at the bottom left corner of the field area, we place it at the center of the usable reticle area and first perform pattern shift. If the mask does not work, we then perform floorplanning using the result of pattern shifting as a starting point. In addition to this, our floorplanner allows the entire mask pattern to be rotated or flipped by enumerating the different scenarios and picking the best solution[1].
- The CD impact of a buried defect is modeled by assuming a Gaussian-shaped defect with impact proportional to the height of the defect at absorber edge, based on existing work on EUV defect simulations.
- In addition to the model used in [20], we have enhanced the model to account for error in defect position due to the limitations of current blank inspection tools. We also corrected the model by accounting for the fact that an absorber covered defect has less CD impact compared to an uncovered defect.
- Our cost estimation and floorplanning methodology is enhanced to account for the scenario where multiple layers of a particular design are patterned using defective EUV masks.
- In constrast to the recently proposed approach in [19], we optimize a continuous CD impact metric for a fixed number of die copies on a mask. A continuous metric helps discover the minimum electrical impact solution,

[1]Note that rotating the entire mask pattern incurs little manufacturing overhead compared to rotating individual die patterns, which was explored earlier [20].

even if the tolerance target cannot be met. We do not change the number of die copies that can be placed on the mask, since that can lead to large wasted scribe line space on the mask, and consequently the wafer. In addition, our approach is design-aware and results are shown for the multiple layer scenario as well.

This paper is organized as follows. Section II discusses the formal problem definition. This is followed by the definition of CD impact and mask yield metrics which are optimized during floorplanning in Section III. Section IV then discusses the algorithm used for solving the problem. Experimental results are covered in Section V, and Section VI concludes this paper.

II. Problem Formulation

Floorplanning of dies on a mask is a well studied problem in DUV lithography. The problem is typically solved for multi-project reticles with dies of different dimensions, because for a single-project scenario, a simple gridded floorplan suffices. The earliest works focused on achieving the most compact placement of rectangles in a given area [21]. B*-tree is an efficient data structure to solve the compact floorplan problem [22]. Many later approaches looked at maximizing the number of chips after dicing the wafer. Kahng et al [23] solved this problem using quadrisection based simulated annealing. The problem was solved as a mixed-ILP in [24].

In this work, we tackle the reticle floorplanning problem for EUV lithography. The need for reticle floorplanning in EUV, even for single-project masks, stems from the yield loss caused by buried defects in EUV mask blanks. We focus only on single-project reticles because the likely adopters of EUV lithography will be high volume chips, that do not use multi-project shuttle masks. Since multiple layers of a single design may be patterned using EUV lithography, the method needs to ensure that all the relevant layers can be patterned on different mask blanks simultaneously, such that none of them are affected by these mask defects. We consider four critical layers; polysilicon, active, contact and metal 1 since other less critical layers will most likely be patterned using conventional DUV lithography, where mask blanks do not suffer from defects.

With these considerations in mind, the reticle floorplanning problem for defective EUV mask blanks can be formally stated as follows:

Given a design of dimensions $L_d \times W_d$ with K physical layers that need to be patterned using EUV lithography, and K reticles, each with the same usable area of dimensions $L_r \times W_r$, but a distinct defect map (location + size of buried defects), find a floorplan such that the impact of buried defects on mask yield is minimized.

III. Metrics for Defect-Aware Reticle Floorplanning

A. CD Impact Metric

Estimating the impact of buried defects on wafer has been extensively studied through experimental work (wafer exposure followed by inspection) [25] and lithography simulations [26] for different defect dimensions and optical conditions. These approaches typically study minimum pitch grating patterns and look at printability and CD change caused by these mask defects for different defect height, width and position relative to the absorber pattern. Using their EUV lithography simulator, Clifford and Neureuther [3] proposed a simple linear model to estimate the CD change of a grating pattern as a function of defect height for a fixed width and position. Using this model as starting point, with the assumption that it is valid even for non-grating layout patterns, we make the following assumptions to evaluate the CD impact of buried defects on a general layout pattern:

- All defects have a 3D symmetric Gaussian shape as shown in Figure 3. The application of a smoothing process during the multi-layer deposition [3] step for EUV mask manufacturing makes this a fairly accurate assumption for defect modeling. As shown in Figure 3, H is the maximum height of the Gaussian defect and full width half maximum (FWHM) is the width of the defect where the height is $H/2$.
- The CD impact of a defect on a particular absorber is assumed to be proportional to the height of the defect at the closest edge of the absorber. Hence as a defect moves away from an absorber, it's effect reduces exponentially. But, as shown in Figure 4, this assumption implies that two defect locations D1 and D2 lead to the same CD impact. In reality, intensity drop of an aerial image, and hence CD impact, would be more when most of the defect is not covered by the absorber. To correct for this, we apply an additional correction factor, D_A, to our model. We chose $D_A = 0.5$ if the center of the defect lies under the absorber, and $D_A = 1.0$ if the defect center lies outside the absorber, based on simulation results in [27].
- To account for defocus, which can have a significant impact on CD change due to the phase nature of these buried defects [25], [26], we scale up the values obtained from the linear model by $3\times$. This is a pessimistic approximation based on existing simulation results for defocus value of $\pm 75nm$ [27].
- A single absorber pattern cannot be affected by more than one defect. This assumption is reasonable, considering that typical defects are randomly distributed across an entire $6in. \times 6in.$ mask. Unless defect density is very high, two defects are unlikely to lie close to a single absorber pattern, a situation illustrated in Figure 5.
- Current mask blank inspection tools are unable to accurately locate the position of the defect. In order to make the mask floorplanner robust to positional error, we consider a circular region of uncertainty around the most likely defect center location (as per the blank inspection tool). We then assume that the distance between the defect and an absorber edge is equal to the smallest distance between the uncertainty region and the absorber. This assumption is illustrated in Figure 6.

With these assumptions, the CD impact for a buried defect, which is at a distance r from an absorber edge as shown in Figure 7, can be calculated using Equations 1 - 3. a is the positional error value and r_c is the worst case distance between

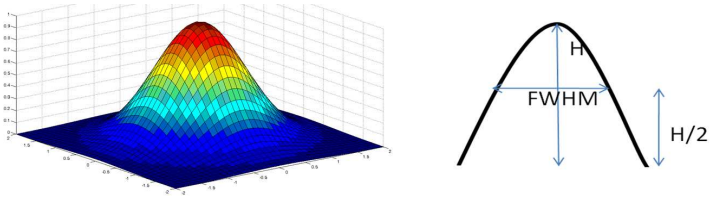


Fig. 3. A 3D, symmetric Gaussian defect on the left and its planar projection with height H and full width at half maximum FWHM.

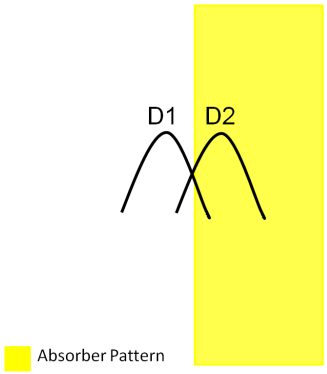


Fig. 4. Two potential locations of a defect, D1 and D2 relative to absorber edge. We assume that D1 has twice the CD impact of D2.

the defect and the absorber. $I_{NoDefect}$, m_{defect}, b_{defect} and $ImageSlope$ are constants whose values are taken from [3] [2].

$$r_c = max(r - a, 0) \tag{1}$$

$$DefHeight = He^{-r_c^2/(FWHM/2)^2} \tag{2}$$

$$CD_{def} = \frac{3D_A \cdot \sqrt{I_{NoDef}} \cdot (m_{def} \cdot DefHeight + b_{def})}{ImageSlope} \tag{3}$$

B. Design Level Metrics

To find out whether a buried defect will cause a design to fail or not, we also need to know the acceptable CD deviation

[2] $m_{defect} = 0.191nm^{-1}, b_{defect} = 0.094, I_{NoDefect} = 0.3$ and $ImageSlope = 0.0471nm^{-1}$

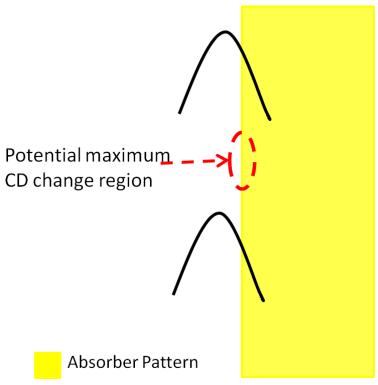


Fig. 5. A scenario with two defects changing CD of a single absorber. The worst case CD change may not lie at minimum distance edge fragement of either defect.

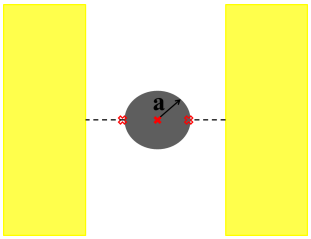


Fig. 6. Pessimistic approach to model a uncertainty in defect position.

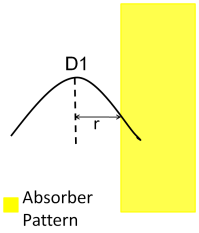


Fig. 7. A defect and absorber with r as distance between center of defect and closest absorber edge.

that each design shape can tolerate. This CD tolerance can be computed using the method proposed in [28] if some design information is available to mask manufacturers. If not, a single conservative CD tolerance can be assigned to each shape in the design. Using a CD tolerance assignment and the CD impact of of each defect on every absorber shape, we develop a concise metric to estimate the overall design impact of buried mask defects, which can then be optimized for by our floorplanner.

A design is said to work if $CD_{def} < CD_{tol}$ for the all the defects and absorber shapes of each layer of the entire mask pattern. This binary requirement can be treated as a constraint to find a valid floorplan. But a better alternative is to minimize a continuous metric that minimizes the overall CD change of the entire mask so that the impact of defects on the printed patterns is minimized, even if the mask does yield. To do this, we propose a simple cost metric that estimates the design impact of all the buried defects on a mask for a particular physical layer l of one die d as shown in Equation 4, where $BD(l)$ is the set of buried defects on the mask and $S(l)$ is the set of absorber shapes in the corresponding layer l of the die. The net cost metric for the entire reticle, which we minimize during floorplanning, is obtained by summing the cost function of Equation 4 over all layers and dies on the reticle as shown in Equation 5, where D is the set of all dies on a reticle and L is the set of physical layers that are patterned using EUV lithography.

$$Cost(d,l) = \sum_{b \in BD(l)} \sum_{s \in S(l)} e^{CD_{def}(d,b,s) - CD_{tol}(d,s)} \tag{4}$$

$$Cost = \sum_{d \in D} \sum_{l \in L} Cost(d,l) \tag{5}$$

The runtime to compute this metric is $O(|D| \cdot \sum_{l \in L} |BD(l)| \cdot |S(l)|)$. But instead of computing the cost for each polygon for every defect we can consider only those polygons which lie in a region of influence R from the defect center. This region R is taken as a function of defect FWHM and defect position

error as shown in Equation 6. Finding all polygons which lie within R can be done in $O(\log|S(l)|)$ using 2D region query tree data-structure to represent the entire die pattern [29]. Hence the runtime for computing the cost reduces to $O(|D| \cdot \sum_{l \in L} |BD(l)| \cdot \log|S(l)| \cdot |S_R(l)|)$, where $S_R(l)$ is the set of polygons inside the region of influence ($|S_R(l)| << |S(l)|$ for typical defect size and alignment error).

$$R = 3 \cdot FWHM + a \tag{6}$$

Note that this cost metric is not equivalent to yield but it is indicative of the overall electrical impact of buried defects on the design. For example, if a single die has multiple defects, moving the die may not improve yield at all, but it could still reduce this cost metric. Another important point is that although we have used a closed form expression to calculate the CD impact of a buried defect, our floorplanner is agnostic to the defect model. It is possible to use a fast simulator such as RADICAL [26] for layout snippets around each buried defect to evaluate the design impact more accurately.

IV. Floorplanning Algorithm

To solve the single project, multiple die reticle floorplanning problem formulated above, we consider only gridded solutions because they guarantee that no die is lost after side-to-side wafer dicing. A non-gridded solution can potentially be more compact, but will usually lose some dies during dicing which need to be accounted for during yield computation. Enforcing a gridded solution also limits the solution space and simplifies the floorplanning algorithm. We chose the simulated annealing framework [30] to solve this optimization problem since previous work on floorplanning [21], [23] suggests that it is a good heuristic for floorplanning problems.

In simulated annealing based optimization, an initial solution is randomly chosen, which in our case is a floorplan with no space between any die, starting from the center of the usable reticle area. An appropriate perturbation or move is applied to the solution, which increases or decreases the metric we wish to minimize. If a change or move reduces the cost it is accepted. But the move increases the cost, it is accepted with a finite probability depending on the increase in cost and the number of prior iterations. Temperature is usually used as a parameter that reduces with each iteration of the optimization, in analogy to thermal annealing. So, initially when the system is hot, most moves, even those that increase cost, are accepted. As the system cools down, the optimizer behaves more like a greedy algorithm.

To define moves for gridded solutions, we first define a set of horizontal and vertical gridlines. If we have an initial compact floorplan with m rows and n columns of dies, then we have m horizontal gridlines and n vertical gridlines. Each horizontal(vertical) gridline has its corresponding y(x) coordinate linked to all die whose bottom (left) coordinate is the same. So, each die is linked to two gridlines, one vertical and one horizontal. Both horizontal and vertical gridlines are sorted by their respective coordinates. Each gridline coordinate (and all the linked dies) can be moved by a predefined value $\pm\delta$. This is a move or perturbation for our optimization. Hence

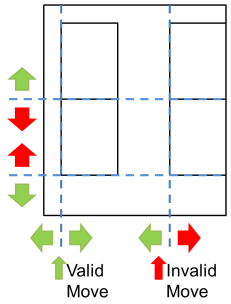


Fig. 8. Illustration of valid and invalid moves

any vertical (horizontal) gridline L_i^V (L_i^H) has two possible moves:(1) $x_i(y_i) = x_i(y_i) + \delta$;(2) $x_i(y_i) = x_i(y_i) - \delta$. A move is labeled as valid or invalid based on whether spatial constraints are obeyed after the move is made. The three main types of spatial constraints that must be obeyed by every gridline are listed below, where $W_R(H_R)$ is the usable reticle width (height), $W_D(H_D)$ is die width (height), $i \in \{1, 2...n\}$, $j \in \{1, 2...m\}$ and, $x_1(y_1)$ and $x_n(y_m)$ are the smallest and largest co-ordinates of the gridlines.

- Reticle Boundary Constraints ($i(j) \neq 1$):
  $x_1(y_1) \geq 0$, $x_n(y_m) + W_D(H_D) \leq W_R(H_R)$.
- Die Overlap Constraints:
  $x_i(y_j) - x_{i-1}(y_{j-1}) \geq W_d(H_d)(i(j) \neq 1)$.
- Maximum Allowed Field Size Constraints:
  $x_n(y_m) + W_D(H_D) - x_1(y_1) \leq fieldX(fieldY)$

Figure 8 graphically illustrates these moves and their validity. There are a total of $2 * m + 2 * n$ potential moves and $4 + (m - 1 + n - 1) + 2$ spatial constraints which must be checked to determined which of the potential moves are valid.

Apart from moving dies, their orientation can also be changed. Each die can have four possible orientations as shown in Figure 9[3]. However, these orientation changes can have significant manufacturing overheads. Flipping the die would lead to dies with different pin locations and hence require a different package. Rotation by 180^o makes wafer testing significantly harder (potentially requiring a different probe-card). Due to these manufacturing overheads, we have disallowed any orientation changes in our algorithm.

Although die level orientation changes are disallowed, rotation of the entire mask pattern (all $m \times n$ dies) will not suffer from any of the manufacturing issues discussed above. In order to allow this orientation change, we apply our simulated annealing based floorplanning described above to four rotated versions (default, 180^o, flipX, flipY) of the entire mask pattern. We then choose the best solution among them.

We noted earlier that floorplanning incurs an overhead in the form of wasted scribe and consequently, wafer area. It is possible that for a certain defect distribution on the mask, just shifting the entire mask pattern is sufficient. In order to circumvent this limitation of floorplanning, we first perform pattern shift and then check if the mask works. If the mask does not work after pattern shift, we perform floorplanning.

[3] $90^o/270^o$ rotation is not considered due to lithographic patterning constraints.

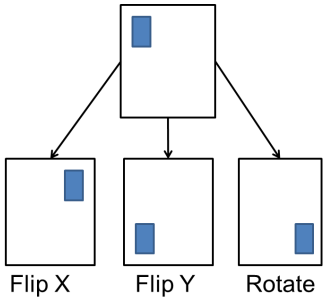


Fig. 9. Illustration of various orientations for a die

Additionally, the minimum CD impact position returned by pattern shifting is used as a starting solution for reticle floorplanning.

Algorithm 1 summarizes the complete algorithm. Lines $1-2$ define an initial partition where dies are placed in a compact grid on the reticle such that the mask pattern is at the center of the usable reticle area. Lines $3-12$ iterate over the four orientation options for the mask pattern and performs floorplanning for each orientation and the best orientation is chosen in Line 13. Lines $4-7$ incorporate the step of shifting the entire mask pattern by calling the function PATTERNSHIFT(). Reticle floorplanning is then performed in Line 11 by calling FLOORPLAN(), if the mask still fails.

The function PATTERNSHIFT() in Lines $14-20$ of Algorithm 1 essentially merges all the dies on the mask to create a single larger pseudo-die, $D_{fullMask}$. With this new die, it calls the existing simulated annealing based FLOORPLAN() function. The final shifted position of the pseudo-die is returned.

The function FLOORPLAN() in Lines $21-41$ of Algorithm 1 is the key function that actually performs the simulated annealing based gridded floorplanning. In each iteration of the while loop the best valid move (maximum cost reduction or minimum increase) is chosen in lines $29-31$. The simulated annealing criteria is then applied to determine if the move should be accepted or not in Lines $32-37$. To improve runtime, we stop the annealing optimization as soon as the mask yields, in Lines $26-28$. This helps reduce the runtime by stopping the optimization when a solution that yields is found.

The runtime of our approach summarized in Algorithm 1 is dominated by the cost computation for each valid move during the FLOORPLAN() function. Among the $2*(m+n)$ potential moves, we first find the set of valid moves and then evaluate the cost change of each valid move. Although this cost computation is done incrementally in the sense that cost needs to be computed only for the dies which move, at worst it needs to be done for each defect on the mask. For a simulated annealing schedule with initial temperature $T_{initial}$, final temperature T_{final} and cooling rate cr the overall complexity of this approach is therefore, $O(log_{cr}(\frac{T_{final}}{T_{initial}}) \times (k_1 * (m+n) \times f_{cost}))$, where k_1 is a constant and f_{cost} is the time to calculate the cost function of Equation 5 for one die which is $O(\sum_{l \in L} |BD(l)| \times \log |S(l)|)$ where L layers patterned with EUV, and a particular physical

Algorithm 1 Reticle floorplanning algorithm for EUV mask

Require: Width (W_D) and Height (H_D) of reticle, width(W_R) and height (H_R) of each die, location/size of defects on mask blank BD and all design layout shapes (S) with CD tolerances.

Ensure: Location of die such that number of defects in critical areas is minimized.

1: $m = H_R/H_D$ rows of dies, $n = W_R/W_D$ columns of dies.
2: Place $m \times n$ dies on the reticle such that the reticle field is at the center of the usable reticle area.
3: **for all** orientation $\in$ (default, 180^o, flipX, flipY) **do**
4: **if** Number of die > 1 **then**
5: (X_i, Y_i) $\leftarrow$ PATTERNSHIFT(D, BD, S).
6: Shift all $d \in D$ by (X_i, Y_i).
7: **end if**
8: **if** Mask works **then**
9: Exit for loop, choose current solution.
10: **end if**
11: $D_{fp}(orientation) \leftarrow$FLOORPLAN($D$, BD, CD_{tol}).
12: **end for**
13: $D_{final} = argmin(Cost(D_{fp}))$.

14: **function** PATTERNSHIFT(D, BD, S).
15: Merge dies $d \in D$ into one large die $D_{fullMask}$.
16: $D_{shift} \leftarrow$FLOORPLAN($D_{fullMask}$, BD, S).
17: $X = D_{shift} -> left - D_{fullMask} -> left$.
18: $Y = D_{shift} -> bottom - D_{fullMask} -> bottom$.
19: Return (X, Y).
20: **end function**

21: **function** FLOORPLAN(D, BD, S)
22: Define vertical gridlines for each column of dies in D.
23: Define horizontal gridlines for each row of dies in D.
24: $T = T_{initial}$, cr is cooling rate .
25: **while** $T > T_{final}$ **do**
26: **if** Mask works **then**
27: Exit while loop, choose current solution.
28: **end if**
29: Find all valid gridline moves.
30: Compute cost change $\Delta Cost$ for each valid move.
31: $c^* = min(\Delta Cost)$, $m^* = argmin(\Delta Cost)$
32: **if** $c^* <= 0$ **then**
33: Accept m^*.
34: **end if**
35: **if** $c^* > 0$ **then**
36: Accept m^* with probability $P = exp(-c^*/T)$.
37: **end if**
38: $T = T * cr$.
39: **end while**
40: Return D with updated coordinates.
41: **end function**

layer l has $|S(l)|$ shapes and is patterned on a mask with $|BD(l)|$ defects as described in Section III-B.

V. Experimental Results

A. Setup

The entire floorplanning algorithm was implemented in C++ using the OpenAccess API [31]. The schedule for simulated annealing is taken as $T_{initial} = 10^5$, $r = 0.995$ and $T_{final} = 10^{-5}$. Instead of using a single value of move distance, we chose a range of values for move distances, restarting the annealing iterations for each move distance value. We chose the move distance values in a decreasing geometric sequence with common ratio as 0.5. The largest move distance was taken as one-tenth of the biggest move that can be made without causing a spatial constraint violation. The smallest move distance was taken as $50nm$, which is close to the defect width considered in most experiments. This strategy allows the optimizer to explore a large part of the solution space in a reasonable runtime. But an important point to note here is that this approach is not optimal since the full continuous solution space is not explored. Hence all the reported results in this section are a lower bound on what defect avoidance can achieve.

We perform floorplanning with three different die sizes which are shown in Table I along with the number of dies that can be fit inside a standard field size of $104mm \times 132mm$ [4]. All three benchmark designs are constructed by tiling copies of a $45nm$ MIPS design, which was placed and routed with 70% utilization in Cadence SoC Encounter [32] using Nangate $45nm$ library [33]. Since EUV lithography, is unlikely to be adopted before the $11nm$ technology node, the $45nm$ design is scaled down to $11nm$ before tiling it. Hence, all reported results are valid for the $11nm$ technology node unless otherwise stated.

TABLE I
Different die sizes considered

Design Label	Die Size ($mm \times mm$)	# Die/reticle	Field Size ($mm \times mm$)
Design A	51.97×65.99	4	104.05×132.11
Design B	51.97×43.94	6	104.05×131.96
Design C	34.60×32.99	12	103.90×132.11

We assume that the entire usable area of the mask blank ($142mm \times 142mm$), as described in Figure 2, can be utilized for placing the mask pattern. Since the size of the mask pattern is approximately $104mm \times 132mm$, total shift area of $38mm \times 10mm$ is available. The maximum scribe area is constrained at 0.2%. These spatial constraints are modified to evaluate their impact in Section V-G.

For our experiments we chose a single size for all buried defects, with height $H = 2nm$ and width, $FWHM = 50nm$ except in Section V-F, where we explore the impact of defect size on mask yield. These values are typical defect sizes currently being reported, as illustrated in [34]. We show results with different number of defects on the mask to highlight mask defectivity levels that are acceptable after floorplanning. Due to the absence of any industrial data on the spatial distribution of buried defects on the mask we assume that they are uniformly distributed over the usable reticle area of $142mm \times 142mm$. 500 different spatial distributions of defects on the mask are considered and all reported results are an average of these Monte Carlo simulations.

[4] All dimensions in this section are mask scale unless explicitly stated

B. Impact of Design Information

In the absence of any design information, the mask maker can assign a fixed CD tolerance to each absorber shape and then use that to perform floorplanning. In this work, we assign a conservative CD tolerance of 10% of the minimum feature size, which is equal to $1.1nm$ in a $11nm$ design (wafer scale). The results with this design-unaware approach for polysilicon layer reticle is shown with different number of defects in Table II. The table lists the average value of proposed cost function before and after the floorplanning, along with mask yield (*fraction of masks with all die functioning*). We also report the maximum scribe area among all the random defect distributions, which is the percentage of field area that is lost due to gap between multiple die copies. This scribe area loss, which we constrainted to 0.2% as mentioned earlier, translates to wasted space on the wafer and hence must be kept small.

Without any floorplanning, a 40-defect reticle will not yield for any of the 500 random defect maps, but floorplanning can improve the mask yield to more than 99% with scribe area of only 0.19% in the worst case scenario[5]. Note that the initial yield is not affected by the number of die copies per reticle, as expected.

If mask makers are provided with some design information, they can exploit it to assign different CD tolerances to different absorber shapes based on their criticality. One approach to do this has been discussed in [28]. Assigning CD tolerances based on criticality reduces the pessimism in yield computation caused by assigning a single CD tolerance to each shape. This can be clearly seen if we compare the initial mask yield of Table III compared to Table II. Design awareness also allows the floorplanner more opportunities to improve yield by placing non-critical absorber shapes close to buried defects. The post-floorplanning mask yields of Table II and Table III illustrate this advantage of design awareness as post-floorplanning mask yield is more than 99% for a 60-defect reticle, compared to 26% in the design-unaware case.

The substantial improvement in yield as a result of design-awareness stems from the fact that a significant fraction of the layout shapes are not timing-critical, allowing us to relax their CD tolerance. To validate this hypothesis, we increased the clock frequency of the design, which shifts the slack histogram, as shown in Figure 10. As a result, the number of timing-critical layout shapes increases slightly and the yield before and after floorplanning reduced by approximately $0.5 - 1\%$. An important point to note here is that the benefit of design-awareness depends strongly on the particular design

[5] These yield values reflect the reality more accurately than our previous work [20], where the mask yield was overestimated due to a software bug.

TABLE II
EXPERIMENTAL RESULTS FOR POLYSILICON LAYER RETICLE FLOORPLANNING WITHOUT DESIGN INFORMATION

Design Label	# Defects	Initial		Final		
		Cost	Mask Yield(%)	Cost	Mask Yield(%)	Max. Scribe Area(%)
Design A	20	5370.72	1.0	4.49	100.0	0.11
	40	11301.90	0.0	21.92	99.2	0.16
	60	17332.90	0.0	5145.05	26.8	0.19
	80	21575.60	0.0	10838.30	0.2	0.19
	100	28008.60	0.0	15189.20	0.0	0.20
Design B	20	4975.88	1.2	4.36	100.0	0.16
	40	11135.60	0.0	23.74	99.8	0.19
	60	17003.80	0.0	5586.01	25.6	0.19
	80	22618.80	0.0	10489.70	0.6	0.19
	100	27370.20	0.0	15422.20	0.0	0.19
Design C	20	5144.43	1.6	4.25	100.0	0.00
	40	11299.80	0.0	25.46	99.8	0.19
	60	16351.00	0.0	5407.53	25.8	0.20
	80	22327.70	0.0	10492.30	0.4	0.20
	100	27336.60	0.0	14333.90	0.0	0.19

TABLE III
EXPERIMENTAL RESULTS FOR POLYSILICON LAYER RETICLE FLOORPLANNING WITH DESIGN INFORMATION

Design Label	# Defects	Initial		Final		
		Cost	Mask Yield(%)	Cost	Mask Yield(%)	Max. Scribe Area(%)
Design A	20	440.86	4.6	0.70	100.0	0.12
	40	927.72	0.0	1.49	100.0	0.00
	60	1422.77	0.0	8.07	99.4	0.18
	80	1771.03	0.0	495.35	45.8	0.18
	100	2299.09	0.0	1162.00	4.2	0.19
Design B	20	408.44	5.2	0.76	100.0	0.09
	40	914.06	0.6	1.51	100.0	0.00
	60	1395.76	0.0	9.78	99.2	0.18
	80	1856.66	0.0	482.58	48.2	0.19
	100	2246.69	0.0	1204.89	4.8	0.20
Design C	20	422.28	4.8	0.71	100.0	0.00
	40	927.54	0.0	1.47	100.0	0.00
	60	1342.17	0.0	5.67	99.6	0.20
	80	1832.77	0.0	478.51	48.8	0.19
	100	2243.92	0.0	1164.59	4.0	0.20

being analyzed and the power or delay optimization choices made during architecture or physical design (retiming, gate sizing, V_{th} assignment, etc.).

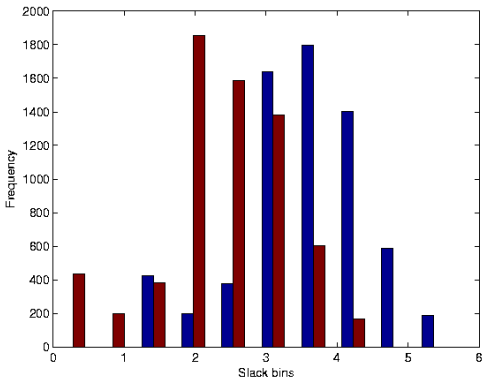


Fig. 10. Slack Histogram of MIPS design used as our testcase (blue), and the shifted histogram (red) after increasing the clock frequency.

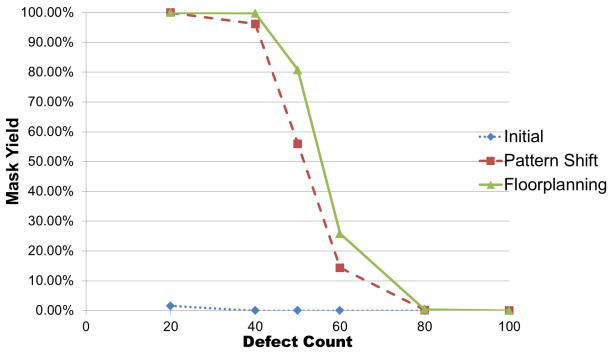
Incorporating design information during EUV mask manufacturing can have significant benefits as shown above. But the current design to manufacturing handoff does not include such timing information. Hence we have chosen to report results for both design-unaware and design-aware scenarios in all the analysis below.

C. Comparison with Pattern Shift

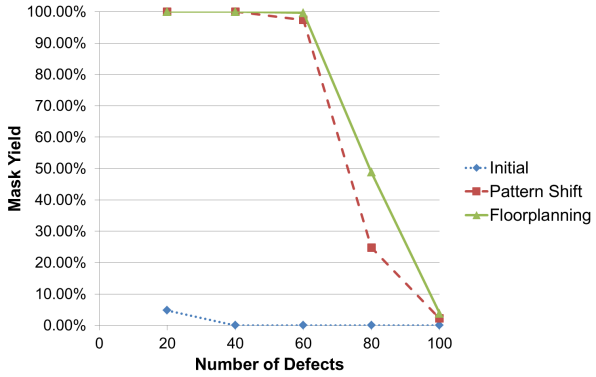
In this subsection, we empirically quantify the benefit of floorplanning compared to pattern shift. In order to make this comparison, we compute the mask yield after performing the PATTERNSHIFT() step in Algorithm 1 to the mask yield after floorplanning.

Figure 11 illustrates the mask yield benefit of floorplanning compared to pattern shifting. If the defect density is low (~ 40 defects/mask), the mask yield is comparable. But as the defect density increases, there is $10 - 30\%$ improvement in mask yield due to floorplanning. This yield improvement came with an area loss of less than 0.2% in all cases. These results clearly show that for reticles which contain multiple die patterns, the additional degrees of freedom that floorplanning plays a significant role in EUV mask defect mitigation.

Since pattern shift explores a smaller solution space for mask yield enhancement, it is expected to have a better runtime. This is illustrated in Figure 12, where the runtime of pattern shift is compared to floorplanning for different number of defects. Runtime is strongly related to the number of defects since it affects the time taken to compute our cost function. More importantly, in our approach, the optimization iterations terminate as soon as a yielding solution is found. This improves runtime significantly for lower defect density cases.



(a) Design-unaware case



(b) Design-aware case

Fig. 11. Comparison of mask yield for Design C before any defect avoidance techniques, after pattern shift and after floorplanning for different number of defects (Defect height $2nm$, FWHM $50nm$)

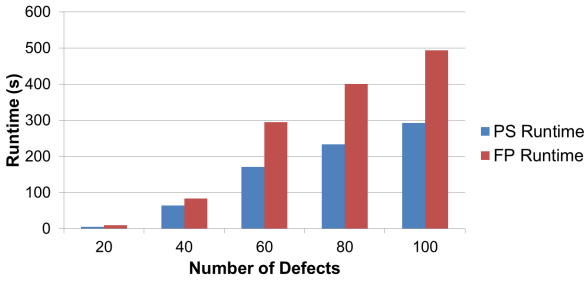


Fig. 12. Comparison of runtime of pattern shift (PS) and floorplanning (FP) for Design C (design-unaware case) for different number of defects (Defect height $2nm$, FWHM $50nm$). Note that our floorplanning implementation utilizes the fact that our design comprises tiled copies of a small MIPS design to reduce runtime. Hence these runtime numbers only offer a comparison between pattern shift and floorplanning, and runtime for large industrial designs will be significantly larger.

D. Impact of Multiple Layers for Floorplanning

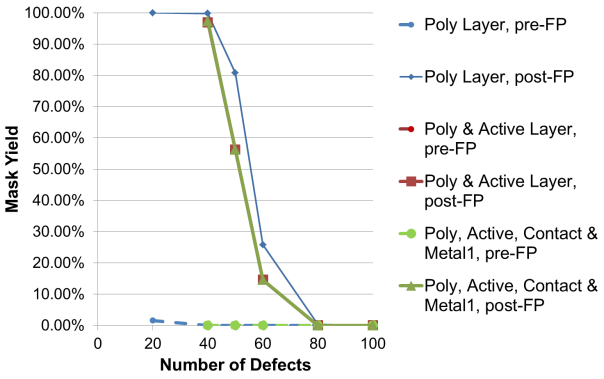
An important concern with floorplanning is that if multiple layers of the design need to be patterned with EUV lithography, then the mask shapes of all these layers must be aligned. In order to accomplish this, our cost function and estimation of mask yield must account for all the relevant layers. One important aspect of multiple-layer floorplanning is blank-to-layer mapping, i.e. choosing the appropriate defective mask blank to pattern each of the K layers of one design. Du et. al. [35] proposed one method to solve this problem in the context of mask patterns that correspond to different designs with different production volumes. In our case, the problem is slightly different since the focus is on different layers of a single design. Since developing a method to perform blank to layer mapping is not the focus of this work, we chose a random blank-to-layer mapping to illustrate the impact of patterning multiple layers of a design using EUV.

The need to keep multiple layers aligned during floorplanning is a significant limitation that reduces the potential yield benefit. But pattern shift does not suffer from this limitation, and each physical layer of a design can be placed independently. This implies that a multi-layer floorplanning solution must ensure that only the relative coordinates of different die copies are aligned for different layers, not their absolute coordinates. This aspect of multi-layer floorplanning has also been discussed recently by Du et. al. [19]. In order to accoplish this, we first perform pattern shift for each layer independently. Using those results, we perform multi-layer floorplanning such that the relative die location for each layer is the same.

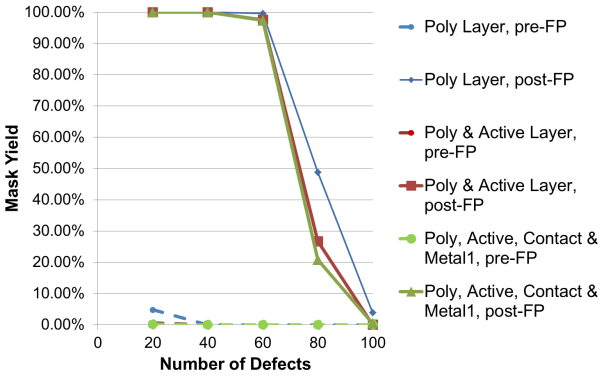
The results in Figure 13 highlight that adding more critical layers lowers mask yield both before and after floorplanning. For example, with a 50-defect mask, if only the polysilicon layer is patterned, mask yield is 81% after floorplanning in the design-unaware case. If the active layer is also patterned along with polysilicon on a 50-defect mask, the yield drops to 56%. Patterning via and metal 1 layers on 50-defect masks as well does not lead to any further drop in mask yield. This suggests that contact and metal 1 layers are relatively easier to pattern. These results clearly show that patterning multiple layers of a design on defective EUV masks is challenging. It may benefit from smarter blank-to-layer mapping but that remains to be investigated. *Note here that the definition of mask yield is slightly different compared to the single layer case. Mask yield here refers to the fraction of designs which work. A design works only if the mask corresponding to every relevant layer works.*

Figure 14 illustrates the additional benefit provided by floorplanning compared to pattern shift when multiple layers are patterned using EUV. Note that the mask yield after pattern shift corresponds to the product of yield of each layer after the pattern shift step. From the plot, it is clear that the benefit of floorplanning over pattern shift is negligible for multiple layers. This can be explained by the fact that the "effective" defect density seen by the floorplanner is significantly higher in the multiple layer scenario. For example, when polysilicon and active layer are patterned on EUV masks with 50 defects on each mask, the pattern shift step attempts to avoid 50 defects on the two masks independently. But since the floorplanner must ensure that the polysilicon and active layer are aligned, it must find a solution to effectively avoid 100 defects.

Another observation from Figure 14 is that the pattern shift yield for multiple layers is very close to the pattern shift yield of the single layer case. This shows that the polysilicon layer is the most challenging layer for pattern shift based defect avoidance. It is comparatively easier for pattern shift to avoid defects for active, contact and metal 1 layers. This observation, though, is strongly design-dependent and may not hold for a

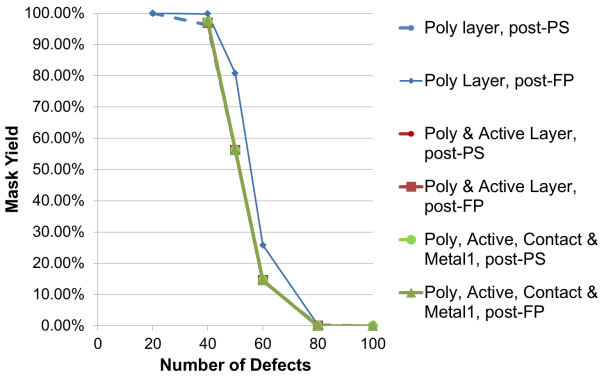


(a) Design-unaware case

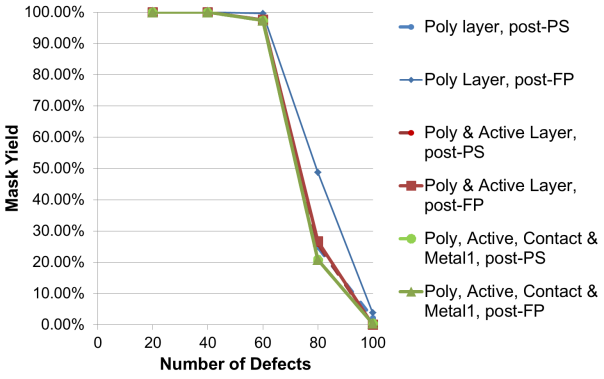


(b) Design-aware case

Fig. 13. Mask yield for Design C before and after floorplanning for different number of layers patterned using EUV (defect height $2nm$, FWHM $50nm$)



(a) Design-unaware case



(b) Design-aware case

Fig. 14. Comparison of mask yield for Design C after pattern shift and after floorplanning for different number of layers patterned using EUV (defect height $2nm$, FWHM $50nm$)

different design, or even a different technology library.

E. Defect Position Inaccuracy

Floorplanning or pattern shifting based approaches to mitigate EUV mask defects rely on the fact that mask blank inspection tools can accurately report the location of defects. Unfortunately, blank inspection technology is currently unable to achieve this. In fact, defect position misalignment of the order of $0.25\mu m$ are being considered as reasonable targets for future blank inspection tools [36]. In light of this limitation, we evaluate our floorplanner at different position inaccuracy values using the model described in Section III.

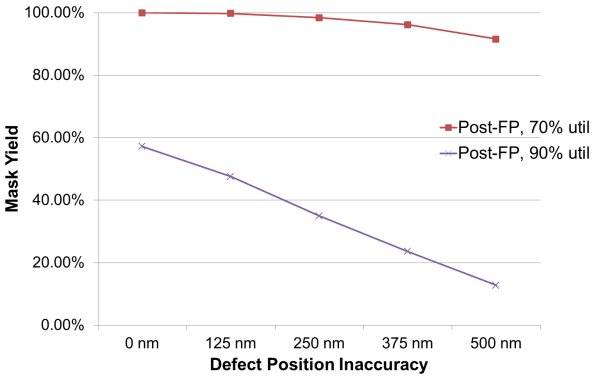
Figure 15 illustrates the impact of defect position inaccuracy on mask yield for a 40-defect mask in the design-unaware case, and a 60-defect mask in the design-aware case. The results show that although mask yield post floorplanning reduces by 2% in the design-unaware case (25% in the design-aware case) for a position inaccuracy of $0.25\mu m$, floorplanning still offers substantial improvement compared to mask yield without floorplanning, which is close to 0% in all the cases shown in Figure 15. This suggests that even with a large defect position error, mask floorplanning can still be used to improve mask yield.

The surprisingly low yield loss of just 2% in the design-unaware case for $0.25\mu m$ position error in a $11nm$ design is due to the availability of ample empty regions in the layout. For a design with 70% core utilization, it is easy for the floorplanner to find such empty regions for just 40 defects. To confirm this, we placed and routed the same MIPS design at 90% utilization and the yield for that case is compared to our default case. as shown in Figure 15(a). There is a 22.0% drop in post-floorplanning mask yield for this denser layout, which validates our justification. Modern technologies often impose strict density constraints as a result of which the empty regions of polysilicon layer would be filled with dummy features. Information about such dummy patterns must be passed on to the mask shop, otherwise the benefit of mask floorplanning with position inaccuracy will be limited.

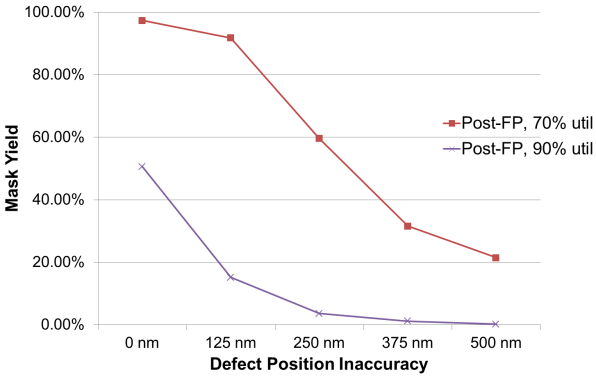
The significant drop in post-floorplanning mask yield of the design-aware, 60-defect case compared to the design-unaware 40-defect case in Figure 15 can be the explained due to the difference in defect density. With 60 mask defects, the empty filler cell regions are not sufficient in preventing yield loss due to position inaccuracy.

F. Impact of Defect Dimensions

Because the size of a buried defect can have a significant impact on CD change and consequently mask yield, we need to validate our approach for different defect dimensions as well. In order to do this, we first assume that all the masks have exactly 40 defects for the design-unaware case, and 60 defects in the design-aware case. Defect alignment error is set

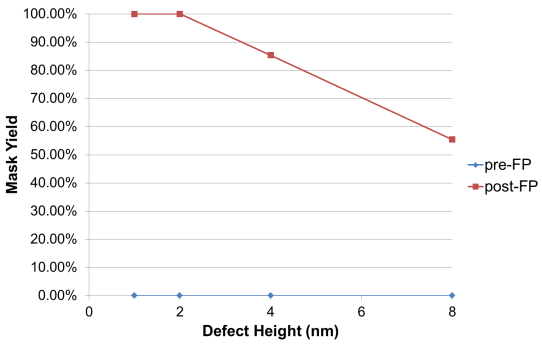


(a) Design-unaware, 40-defect mask

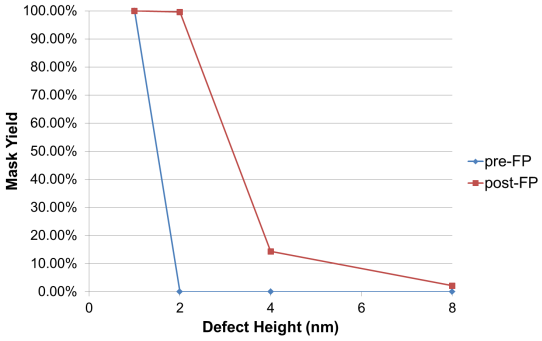


(b) Design-aware, 60-defect mask

Fig. 15. Mask yield for Design C (single layer, 70% utilization) after floorplanning versus defect position inaccuracy with defect height $2nm$, FWHM $50nm$. Mask yield for a higher 90% utilization implementation of the same MIPS design is also shown for comparison.



(a) Design-unaware, 40-defect mask



(b) Design-aware, 60-defect mask

Fig. 16. Mask yield for Design C (single layer) before and after floorplanning versus defect height for defect FWHM $50nm$

to $0nm$. We analyze only the polysilicon layer and compare the yield before and after floorplanning.

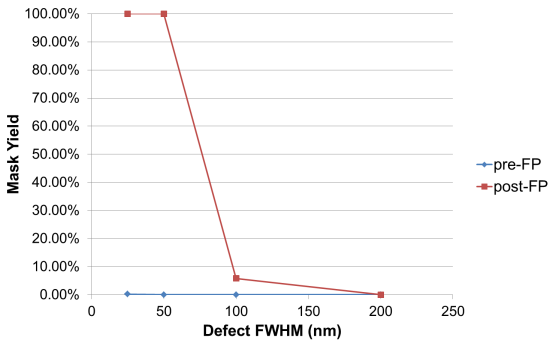
Figure 16 shows a plot of mask yield versus defect height with FWHM kept fixed at $50nm$, and Figure 17 shows the mask yield versus defect FWHM for $2nm$ high buried defects. The results highlight that defects with height more than $2nm$ or FWHM more than $50nm$ would lead to unacceptable mask yield even after floorplanning. A key observation here is the sudden drop in mask yield for both design-unaware and design-aware cases as the defect height changes from $2nm$ to $4nm$, and the FWHM changes from $50nm$ to $100nm$. This sudden drop can be explained by the fact that the mask scale half pitch for $11nm$ is a little less than $100nm$. Hence defects for which the radius of influence is larger than this value will suffer from significant mask yield loss due to limited space for placing such defects.

G. Impact of Adjusting Spatial Constraints

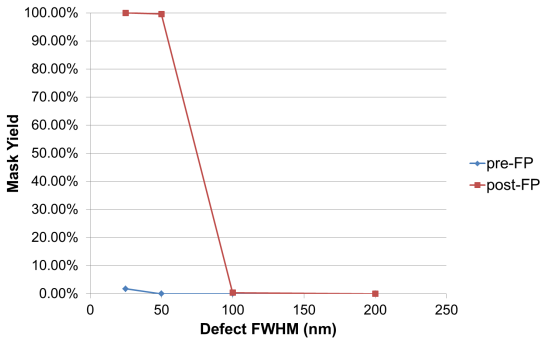
In all our experiments so far, the total area available for placing the entire mask pattern has been kept at $142mm \times 142mm$ and the scribe area constraint has been kept fixed at 0.2%. In this subsection, we shall analyze the impact of change in these constraints on mask yield. Since the trend is expected to be similar for both design-unaware and design-aware scenarios, we shall focus only on the design-unaware case.

Modifying the scribe area constraint provides additional freedom to mask floorplanning at the expense of wasted scribe area on the wafer. To illustrate the impact of scribe area constraint on mask yield, we plot the post-floorplanning mask yield versus scribe area constraint for a single-layer and two-layer case in Figure 18. For the single layer case, increasing the scribe area can significantly improve mask yield. But in the two layer case, there is no benefit of increasing the scribe area constraint up to 2%. This is consistent with our earlier observation that multiple layer scenarios do not derive any additional benefit from floorplanning after pattern shift. Since pattern shift mask yield is unaffected by the scribe area constraint, post-floorplanning yield in the multiple layer case remains unchanged.

Based on the SEMATECH mask standard [18], our current experiments assume a usable reticle area of $142mm \times 142mm$, which translates to a shift area of $10mm \times 34mm$ for placing the mask pattern. But recent studies on pattern shift suggest that the shift area may be constrained to around $200\mu m \times 200\mu m$ by exposure tool vendors [17]. In addition, choosing a usable reticle area value closer to the field size makes it easier to meet defect density and flatness specifications [37]. Hence, we analyze the impact of reducing the total shift area in Figure 19. The figure shows that pattern shift mask yield is significantly impacted by the reduction in usable mask area. But a significant portion of this loss can be made up by floorplanning. As a result, for a scenario where the total shift area is reduced to $50\mu m \times 50\mu m$, pattern shift mask yield



(a) Design-unaware, 40-defect mask



(b) Design-aware, 60-defect mask

Fig. 17. Mask yield of Design C (single layer) before and after floorplanning versus defect FWHM with defect height $2nm$

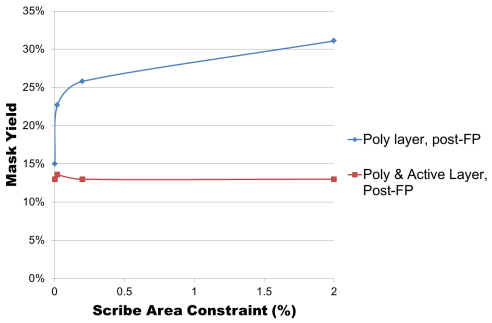


Fig. 18. Post-floorplanning mask yield versus scribe area constraint for 60-defect masks with defect height $2nm$, FWHM $50nm$ (design-unaware case)

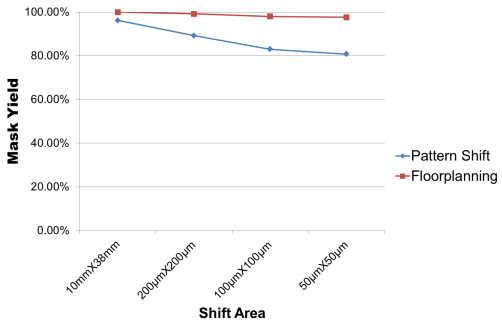
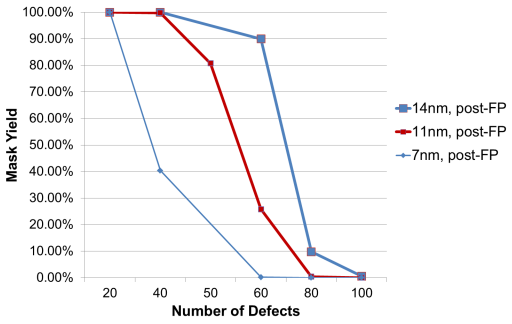
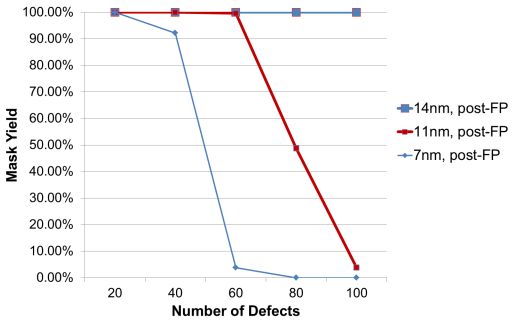


Fig. 19. Post-floorplanning and post-pattern shift mask yield for different total shift values for 40-defect masks with defect height $2nm$, FWHM $50nm$ (design-unaware case)



(a) Design-unaware



(b) Design-aware

Fig. 20. Post-floorplanning mask yield of $14nm$, $11nm$ and $7nm$ Design C (single layer case) versus defect count, with defect height $2nm$, FWHM $50nm$

reduces by 17%, but the drop in yield after floorplanning is only 2%.

H. Impact of Technology Scaling

The persistent delay in adoption of EUV lithography has meant that it might be be adopted at $7nm$ instead of $11nm$ technology node, which is assumed in all our results so far. In order to verify if the benefits of floorplanning hold after scaling, we scale the same layout appropriately to analyze mask yield after floorplanning for $14nm$, $11nm$ and $7nm$ technology nodes.

Figure 20 shows the result of our floorplanner for Design C. The results show that for a 60-defect mask with defect height $2nm$ and FWHM $50nm$, mask yield after floorplanning drops from 90% for $14nm$ to 26% for $11nm$ and 0.00% for $7nm$ in the design-unaware case. The gap worsens with increasing defectivity. These results suggest that although floorplanning is effective in improving mask yield as designs scale, defectivity levels will need to be controlled better at future technology nodes.

VI. Conclusions and Future Work

In this work, we proposed a novel reticle floorplanning based approach to mitigate the impact of buried defects on EUV mask yield. We first proposed a simple model to estimate the CD impact of Gaussian shaped buried defects in the presence of absorber patterns, utilizing the existing literature pertaining to EUV defect simulations. Using this model, we implemented a simulated annealing based gridded floorplanning algorithm for multiple die, single project reticles.

Our results show that reticle floorplanning is an extremely effective approach to deal with buried defects in EUV masks, as it can improve mask yield from 0% to 26% for a $60-$defect mask. Adding design information, which essentially allows assigning different CD tolerances to different shapes, allows the floorplanner to achieve further improvements in mask yield (99% for a 60-defect mask). Our results also suggest that the additional degrees of freedom in moving mask pattern provided by reticle floorplanning compared to pattern shift, translates to a substantial improvement in mask yield (12% point for a 60-defect mask), with a scribe area overhead of just 0.2%.

We made our floorplanner robust to defect position inaccuracy of EUV mask blank inspection tools by incorporating the position error as a part of our defect model. Our results show that reticle floorplanning is an effective strategy to mitigate EUV defects even with large position inaccuracy in mask blank inspection tools. Even $0.25\mu m$ defect position inaccuracy causes only a 2%-point yield loss. Evaluation of our floorplanner at different defect dimensions suggests that defects higher than $2nm$ or wider than $50nm$ can severely limit the benefit of floorplanning. For the same mask defectivity levels, technology scaling has a significant impact on post-floorplanning mask yield. Our results show that scaling from $11nm$ to $7nm$ reduces mask yield by up to 60% point.

One sobering result is that when multiple layers of a design need to be patterned using EUV lithography, the benefits of floorplanning are negligible. Since our analysis was done assuming a random mask-to-layer mapping and a sub-optimal simulated annealing based heuristic, these results indicate a need for smarter approaches to tackle the multilayer defect avoidance problem. Whether that would be sufficient to achieve acceptable mask yields at current defectivity levels remains to be seen, and is a part of our ongoing investigation.

ACKNOWLEDGEMENT

We would like to acknowledge the generous support of IMPACT UC Discovery Grant (http://www.impact.berkeley.edu/) and NSF CAREER award in accomplishing this work. We would especially like to thank Dr. Chris Clifford (Globalfoundries Inc.) for insightful discussions on the issue of EUV mask defects. We would also like to thank Dr. Alexander Starikov (I&I Consulting), Dr. Chul-Hong Park (Samsung Inc.) and Dr. Chris Progler (Photronics Inc.) for their valuable insights and feedback.

REFERENCES

[1] "International Technology Roadmap for Semiconductors(ITRS)," http://www.itrs.net/, 2009.

[2] H. J. Levinson, "Extreme ultraviolet lithography's path to manufacturing," *SPIE Journal of Micro/Nanolithography, MEMS and MOEMS (JM3)*, vol. 8, no. 4, 2009.

[3] C. H. Clifford and A. R. Neureuther, "Smoothing based model for images of buried EUV multilayer defects," in *SPIE/BACUS Symposium on Photomask Technology and Management*, vol. 7122, no. 1, 2008.

[4] A. Rastegar, "Overcoming mask blank defects in EUV lithography," *SPIE Newsroom*, 2009.

[5] R. Jonckheere, D. V. den Heuvel, T. Bret, T. Hofmann, J. Magana, I. Aharonson, D. Meshulach, E. Hendrickx, and K. Ronse, "Evidence of printing blank-related defects on EUV masks missed by blank inspection," in *SPIE Advanced Lithography Symposium*, vol. 7985, no. 1, 2011.

[6] Y. Deng, B. L. Fontaine, and A. R. Neureuther, "Performance of repaired defects and attPSM in EUV multilayer masks," in *SPIE/BACUS Symposium on Photomask Technology and Management*, vol. 4889, no. 1, 2002.

[7] C. H. Clifford, T. T. Chan, and A. R. Neureuther, "Compensation methods for buried defects in extreme ultraviolet lithography masks," in *SPIE Advanced Lithography Symposium*, vol. 7636, no. 1, 2010.

[8] R. Jonckheere, T. Bret, D. V. den Heuvel, J. Magana, W. Gao, and M. Waiblinger, "Repair of natural EUV reticle defects," in *SPIE/BACUS Symposium on Photomask Technology and Management*, vol. 8166, no. 1, 2011.

[9] R. Jonckheere, D. V. D. Heuvel, M. Lamantia, B. Baudemprez, E. Hendrickx, and K. Ronse, "EUV Mask Defectivity Status and Mitigation Towards HVM," in *International Symposium on Extreme Ultraviolet Lithography*, 2010.

[10] C. H. Clifford, T. T. Chan, A. R. Neureuther, Y. Li, D. Peng, and L. Pang, "Compensation methods using a new model for buried defects in extreme ultraviolet lithography masks," in *SPIE/BACUS Symposium on Photomask Technology and Management*, vol. 7823, no. 1, 2010.

[11] L. L. Pang, C. Clifford, P. Hu, D. Peng, Y. Li, D. Chen, M. Satake, V. Tolani, and L. He, "Compensation for EUV multilayer defects within arbitrary layouts by absorber pattern modification," in *SPIE Advanced Lithography Symposium*, vol. 7969, no. 1, 2011.

[12] L. Pang, P. Hu, M. Satake, V. Tolani, D. Peng, Y. Li, and D. Chen, "EUV multilayer defect compensation (MDC) by absorber pattern modification: from theory to wafer validation," in *SPIE/BACUS Symposium on Photomask Technology and Management*, vol. 8166, no. 1, 2011.

[13] P.-Y. Yan, "EUVL ML mask blank fiducial mark application for ML defect mitigation," in *SPIE/BACUS Symposium on Photomask Technology and Management*, vol. 7488, no. 1, 2009.

[14] J. Burns and M. Abbas, "EUV mask defect mitigation through pattern placement," in *SPIE/BACUS Symposium on Photomask Technology and Management*, vol. 7823, no. 1, 2010.

[15] H. Zhang, Y. Du, M. Wong, and R. Topalaglu, "Efficient pattern relocation for EUV blank defect mitigation," in *Proc. Asia and South Pacific Design Automation Conference*, 2012.

[16] E. Gallagher, K. Badger, L. Kindt, M. Lawliss, G. McIntyre, A. Wagner, and J. Whang, "EUV masks: ready or not?" in *International Symposium on Extreme Ultraviolet Lithography*, 2011.

[17] P.-Y. Yan, Y. Liu, M. Kamna, G. Zhang, R. Chen, and F. Martinez, "EUVL multilayer mask blank defect mitigation for defect-free EUVL mask fabrication," in *SPIE Advanced Lithography Symposium*, vol. 8322, no. 1, 2012.

[18] S. Hector, "Standards for EUV Masks," Sematech Mask Strategy Program, Tech. Rep., 2004.

[19] Y. Du, H. Zhang, M. D. F. Wong, Y. Deng, and R. O. Topaloglu, "Efficient multi-die placement for blank defect mitigation in EUV lithography," in *SPIE Advanced Lithography Symposium*, vol. 8322, no. 1, 2012.

[20] A. A. Kagalwalla, P. Gupta, D.-H. Hur, and C.-H. Park, "Defect-aware reticle floorplanning for EUV masks," in *SPIE Advanced Lithography Symposium*, vol. 7974, no. 1, 2011.

[21] S.-Y. Chen and E. C. Lynn, "Effective placement of chips on a shuttle mask," in *SPIE Advanced Lithography Symposium*, vol. 5130, no. 1, 2003.

[22] Y.-C. Yao-Wen, Y.-C. Chang, Y.-W. Chang, G.-M. Wu, and S.-W. Wu, "B*-trees: A New Representation for Non-Slicing Floorplans," in *Proc. ACM/IEEE Design Automation Conference*, 2000.

[23] A. B. Kahng, I. I. Mandoiu, X. Xu, and A. Z. Zelikovsky, "Enhanced Design Flow and Optimizations for Multiproject Wafers," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 2, 2007.

[24] M.-C. Wu, R.-B. Lin, and S.-C. Tsai, "Chip placement in a reticle for multiple-project wafer fabrication," *ACM Transactions on Design Automation of Electronic Systems*, vol. 13, no. 1, 2008.

[25] T. Terasawa, T. Yamane, T. Tanaka, O. Suga, T. Kamo, and I. Mori, "Actinic phase defect detection and printability analysis for patterned EUVL mask," in *SPIE Advanced Lithography Symposium*, vol. 7636, no. 1, 2010.

[26] C. H. Clifford and A. R. Neureuther, "Fast simulation methods and modeling for extreme ultraviolet masks with buried defects," *SPIE Journal of Micro/Nanolithography, MEMS and MOEMS (JM3)*, vol. 8, no. 3, 2009.

[27] C. H. Clifford, "Simulation and Compensation Methods for EUV Lithography Masks with Buried Defects," Ph.D. dissertation, EECS Department, University of California, Berkeley, 2010.

[28] A. Kagalwalla, P. Gupta, C. Progler, and S. McDonald, “Design-Aware Mask Inspection,” in *Proc. IEEE/ACM International Conference on Computer-Aided Design*, 2010.
[29] J. L. Bentley, “Multidimensional binary search trees used for associative searching,” *Commun. ACM*, vol. 18, September 1975.
[30] S. Kirkpatrick, C. D. Gelatt, and M. P. Vecchi, “Optimization by Simulated Annealing,” *Science*, vol. 220, no. 4598, 1983.
[31] “Openaccess API,” http://www.si2.org/.
[32] “Cadence SoC Encounter,” http://www.cadence.com/.
[33] “Nangate Open Cell Library,” https://www.nangate.com/.
[34] H. J. H. Kwon, “EUVL Defect Printability: An Industry Challenge,” Sematech/Samsung, Tech. Rep., 2011.
[35] Y. Du, H. Zhang, M. D. F. Wong, and R. O. Topaloglu, “EUV mask preparation considering blank defects mitigation,” in *SPIE/BACUS Symposium on Photomask Technology and Management*, vol. 8166, no. 1, 2011.
[36] T. Terasawa, T. Tanaka, O. Suga, and T. Tomie, “Optics design and performance analysis of actinic EUV mask blank inspection with dark-field imaging,” in *EUVL Symposium*, 2007.
[37] T. Shoki, M. Mitsui, M. Sakamoto, N. Sakaya, M. Ootsuka, T. Asakawa, T. Yamada, and H. Mitsui, “Improvement of total quality on EUV mask blanks toward volume production,” in *SPIE Advanced Lithography Symposium*.

Abde Ali Kagalwalla (http://www.ee.ucla.edu/~abdeali) is a Ph.D. student at the Department of Electrical Engineering, University of California, Los Angeles. He received his B.Tech degree in Electrical Engineering from the Indian Institute of Technology, Bombay, India in 2009. He received his M.S. in Electrical Engineering at the University of California, Los Angeles in June 2011.

His research interests lie in computer-aided design of VLSI circuits, semiconductor design-manufacturing interface, lithography and algorithms.

Puneet Gupta (http://nanocad.ee.ucla.edu) is currently a faculty member of the Electrical Engineering Department at UCLA. He received the B.Tech degree in Electrical Engineering from Indian Institute of Technology, Delhi in 2000 and Ph.D. in 2007 from University of California, San Diego. He co-founded Blaze DFM Inc. (acquired by Tela Inc.) in 2004 and served as its product architect till 2007.

He has authored over 80 papers, 15 U.S. patents, a book and a book chapter. He is a recipient of NSF CAREER award, ACM/SIGDA Outstanding New Faculty Award, European Design Automation Association Outstanding Dissertation Award and IBM Faculty Award. Dr. Puneet Gupta has given tutorial talks at DAC, ICCAD, ISQED, Intl. VLSI Design Conference and SPIE Advanced Lithography Symposium. He has served on the Technical Program Committee of DAC, ICCAD, ASPDAC, ISQED, ICCD, SLIP and VLSI Design. He served as the Program Chair of IEEE DFM&Y Workshop 2009, 2010, 2011.

Dr. Gupta’s research has focused on building high-value bridges across application-architecture-implementation-fabrication interfaces for lowered cost and power, increased yield and improved predictability of integrated circuits and systems.