Single-Mask Double-Patterning Lithography for Reduced Cost and Improved Overlay Control

Rani S. Ghaida, George Torres, and Puneet Gupta
EE Dept., University of California, Los Angeles
rani@ee.ucla.edu, torresg@ucla.edu, and puneet@ee.ucla.edu

***Abstract*—[1] We propose shift-trim double patterning lithography (ST-DPL), a cost-effective double patterning technique for achieving pitch relaxation with a single photomask. The mask is re-used for the second exposure by applying a translational mask-shift. An additional non-critical trim exposure is applied to remove extra printed features. ST-DPL can be used to pattern critical layers and is very suitable for regular and gridded layouts, where redesign effort and area overhead are minimal. In this paper, the viability of ST-DPL is demonstrated through a design implementation at the poly and contacts layers in bidirectional layouts. Standard-cell layouts are constructed so as to avoid layout decomposition conflicts, which are found to be the limiting factor for the pitch relaxation that can be achieved with double-patterning (ST-DPL as well as standard DPL). 2× pitch relaxation being associated with a considerable area overhead, 1.8× pitch relaxation is achieved in our implementation while ensuring no layout decomposition conflicts and a small area overhead. Specifically, in comparison to layouts assumed to be feasible with a hypothetical single-patterning process, we observe virtually no area overhead when ST-DPL is applied to the poly layer (<0.3% cell-area overhead) and no more than 4.7% cell-area overhead when ST-DPL is applied at both the poly and contacts layers. The proposed method has many benefits over standard pitch-split double-patterning: (1) cuts mask-cost to nearly half, (2) reduces overlay errors between the two patterns, (3) alleviates the bimodal line-width distribution problem in double patterning, and (4) slightly enhances the throughput of critical-layer scanners.**

***Index Terms*—Double patterning, shift-trim, photomask, trim exposure, overlay, bimodal CD distribution, manufacturing throughput, mask cost.**

I. Introduction

Double-patterning lithography (DPL) is one of the most likely short-term solutions for keeping the pace of scaling beyond 32nm node [2]. It is one of the many resolution enhancement techniques (RET) that have been introduced to push the limit of optical lithography. DPL can be implemented with different manufacturing processes: litho-etch-litho-etch (LELE), litho-litho-etch (LLE), and self-aligned double patterning (SADP), a.k.a. spacer double patterning (SDP). In SADP, sidewall spacer defines either spaces or lines depending on the tone of the process and extra printed features are trimmed away using a cut or block mask. Many patterns cannot be printed using SADP, which make it more suitable for well-structured memory cells than random logic layout [2]. This paper focuses on LELE and LLE processes referred to as standard-DPL processes hereafter.

[1]This is an extended version of paper [1].

DPL has four major impediments: high mask-cost, low throughput, within-layer overlay errors, and the CD bimodality problem. DPL mask-cost is estimated to twice that of single patterning because of the need for two critical masks. The additional processing steps required for double patterning significantly reduce the fabrication throughput. The overlay budget being determined by interactions between different layers in single patterning (e.g., metal overhang on via), 20% of half-pitch estimated by ITRS is considered sufficient. In DPL however, overlay budget is much tighter since overlay translates directly into CD variability [3], which has a budget three times tighter than inter-layer overlay according to ITRS [4], and, hence, introduces an extra source of variability [5]. CD typically follows a normal distribution with some σ and μ, which deviates slightly from the target. Since DPL has two separate exposure and etch steps, two populations exist: one for features formed by the first exposure/etch step and another for features formed by the second exposure/etch step.

An attempt to use DPL with a single photomask and, hence, reduce its cost, is reported in [6]. It consists of splitting the mask area into two regions, each corresponding to a different pattern (similar to a multi-layer reticle). As reported in [6], this approach renders fabrication throughput even worse than that of standard-DPL and does not address other DPL technical challenges including within-layer overlay and CD bimodality.

In this paper, we extend our work presented in [1]. In particular, we propose shift-trim DPL (ST-DPL), an effective method to use a single mask to achieve pitch-relaxation. Essentially, the method consists of applying a translational mask-shift to re-use the same photomask for both exposures of DPL. Extra printed features are then removed using a non-critical trim exposure. ST-DPL can be applied to all layers including, but not limited to, active, polysilicon, contacts, metal, and via layers. Moreover, the method can be used for any type of design as long as some basic layout restrictions (discussed in Section III) are met. In this paper, we demonstrate the viability of the proposed method when employed to pattern the polysilicon (poly) and contacts (CA) layers in standard-cell based designs. Cell layouts are constructed so that to avoid layout decomposition conflicts. Resolving decomposition conflicts between features of different cells is found to be the limiting factor for the pitch relaxation that can be achieved with double patterning (ST-DPL as well as standard DPL). As a result, 2× pitch relaxation without conflicts is achieved only at high area overhead. ST-DPL designs show little area overhead, however, while ensuring 1.8× pitch relaxation and no layout decomposition conflicts.

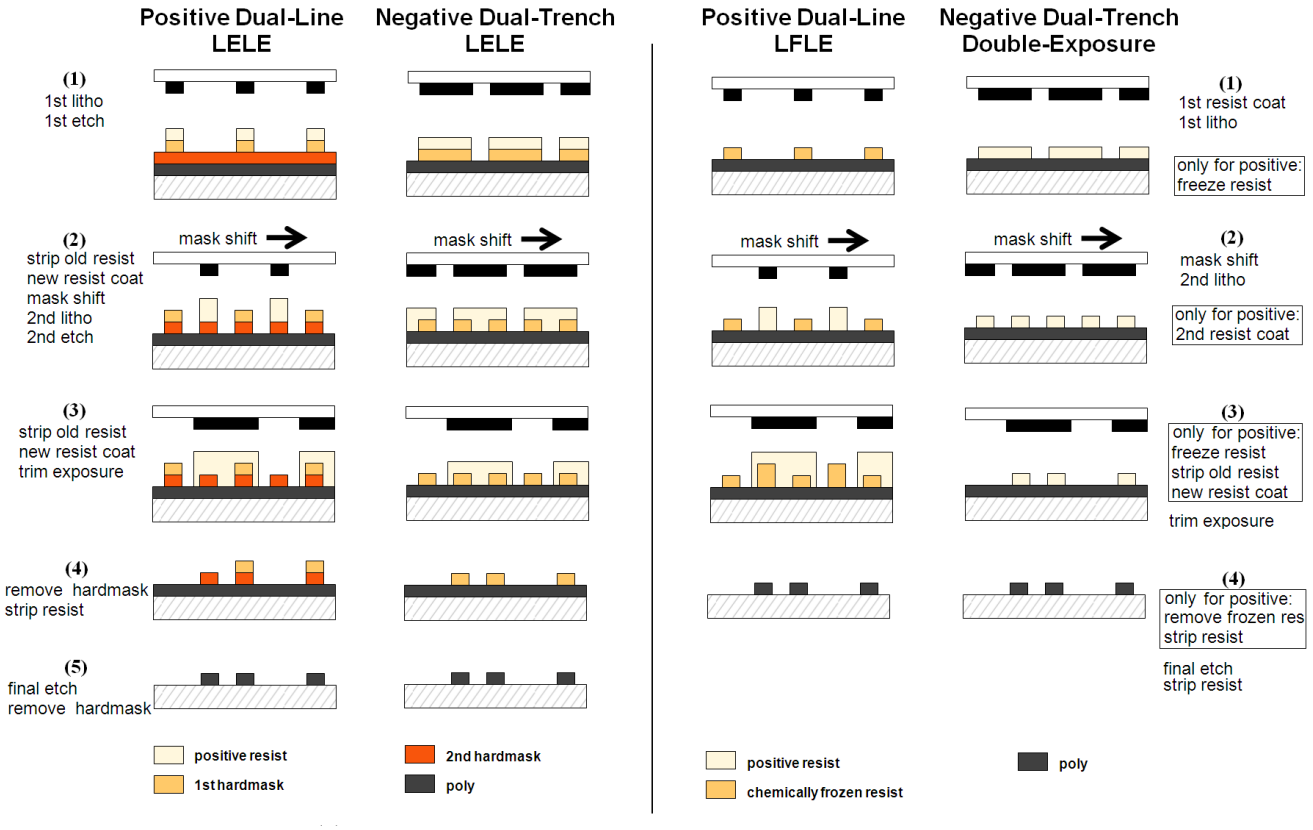


Figure 1. Proposed manufacturing processes for ST-DPL: positive dual-line and negative dual-trench LELE, positive dual-line LLE, a.k.a. litho-freeze-litho-etch (LFLE) process, and negative dual-trench double-exposure processes.

ST-DPL manufacturing process and design requirements are discussed in Section II. In Section III, ST-DPL feasibility at the poly and CA layers are demonstrated by creating a compatible standard-cell library by layout migration of Nangate open cell-library [7] and generating compatible real designs. When compared to the original Nangate layouts (assumed to be feasible with a hypothetical single-patterning process), ST-DPL designs show virtually no area overhead for ST-DPL implementation at the poly layer and an affordable area overhead of at most 4.7% for ST-DPL implementation at both the poly and CA layers. In both ST-DPL implementations, the generated trim mask layouts are simple and lead to an easy-to-fabricate photomask. Benefits of the proposed method in terms of cost, overlay control, CD performance, and throughput are discussed in Section IV, while Section V concludes with a summary.

II. Shift-Trim DPL Overview and Layout Restrictions

This section presents an overview of ST-DPL technique and its associated layout restrictions and challenges.

A. Manufacturing Process

ST-DPL involves the following steps:

1. print the first pattern as in standard DPL processes;
2. shift the photomask of step (1) by a predetermined nanoscale amount X (equal to minimum gate pitch for poly-layer ST-DPL) and print the second pattern;
3. apply a non-critical trim (a.k.a. block) exposure to remove unnecessary features.

The translational mask shift in step (2) is accomplished without any unloading and reloading of the photomask from the exposure tool and no extra requirements on exposure tools. Today's scanners have the capability to perform such translational shift automatically with high precision ($\approx$ 0.6nm) [8].

ST-DPL can be implemented using positive dual-line and negative dual-trench LELE and LLE processes with little modifications as demonstrated in Figure 1[2]. We only show the case of positive resist since it is more commonly used in modern lithography. Negative resist can also be used with little changes to the manufacturing process. In this figure, the processes are presented in order of popularity with the first process on the left being the most popular. Although LLE has higher throughput and lower cost than LELE, to best of our knowledge, LLE is currently not production-worthy. For our design implementation of ST-DPL, we use a positive dual-line LELE process. Nevertheless, ST-DPL implementation with the other less popular/realistic alternatives can be performed with little modifications.

ST-DPL requires an extra step on top of standard-DPL. It consists of an inexpensive and non-critical trim-exposure cycle (resist coat-expose-develop) and removal of hardmask corresponding to extra printed features before the final etch. The trim exposure is a mature and well-known method used in many patterning techniques such as SADP [9, 10], alternating phase-shift mask [11], and subtractive-litho patterning [12, 13]. It was recently employed to trim-away printing

assist features (PrAF) introduced to enhance the resolution of conventional single patterning [14]. A second hardmask layer is necessary in case of positive LELE process, but this does not represent an extra requirement because many standard DPL implementations favor the use of a second hardmask [3, 15]. Relaxed CD and overlay requirements of the trim exposure, which are demonstrated by the results of our implementation, make process control an easy task. Consequently, the cost of trim mask is minor compared to the cost of conventional masks and the trim exposure can be realized using second-tier scanners if this is desirable to enhance throughput.

B. ST-DPL Challenges and Downsides

In addition to the downside of the need for three exposures (two critical and one non-critical trim exposure) and the extra processing steps associated with the trim exposure, ST-DPL has two other challenges.

Although the same features with exactly the same surroundings are on the mask of the first and second exposures, features of different exposures printed on wafer may vary due to process-differences (e.g., resist thickness, hardmask characteristics, etch-interference, etc...). One way to compensate for this difference consists of using different OPC features for the different patterns [16]. In ST-DPL, this method is no longer possible since the same mask is used for the first and second exposures. As a result, other means to correct for processing differences between the two patterns must be employed (e.g., dose-mapping [17]).

Because the ST-DPL mask-shift is performed just uniformly across the design, the minimum gate-pitch must be set to the contacted gate-pitch (typically equal to the amount of the mask-shift) and all gates in the design must follow the same orientation. When memory and logic are integrated, this gate-pitch limitation may impose restrictions on the allowed contacted pitch for memory if it is not the same as the logic contacted pitch.

C. Layout Restrictions at Poly-line Layer

Basic layout restrictions are imposed for implementing ST-DPL at the poly layer. X being the amount of mask shift and X_0 being the minimum gate pitch on the mask[3], the following restrictions apply.

1. For every gate, the pitch to the neighboring gates from one side (subsequent gate to the right or left side) must be either X or $\geq X_0$ and the pitch between the left and right neighboring gates must be $\geq X_0$. This is illustrated by the example of three gate-poly lines shown in Figure 2.
2. In light of (1), minimum gate spacing is equal to contacted-gate spacing (equal to X minus poly-line width).
3. "Wrong-direction" (horizontal) poly routing is restricted to top and bottom routing channels of the cell (i.e. poly-routing in the center of the cell is not allowed).

In addition, some design rule restrictions (especially line-end to field-poly spacing and line-end gap) may be necessary to guarantee a simple trim-mask as we show later in this paper.

[2]BARC layers are not shown for brevity.

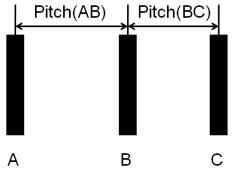


Figure 2. Example illustrating gate-pitch restriction. In case $Pitch(AB)$ is $< X_0$ but different than X, then $Pitch(BC)$ must be either X or $\geq X_0$ and $Pitch(AC)$ must be $\geq X_0$. Similarly, if $Pitch(BC)$ is unrestricted, $Pitch(AB)$ is restricted to X or $\geq X_0$ and $Pitch(AC)$ to $\geq X_0$.

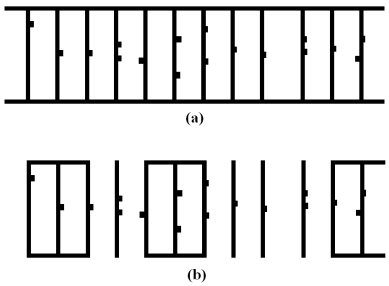


Figure 3. Poly layer ST-DPL critical mask snippet corresponding to a flip-flop cell with two structure-options (a) and (b).

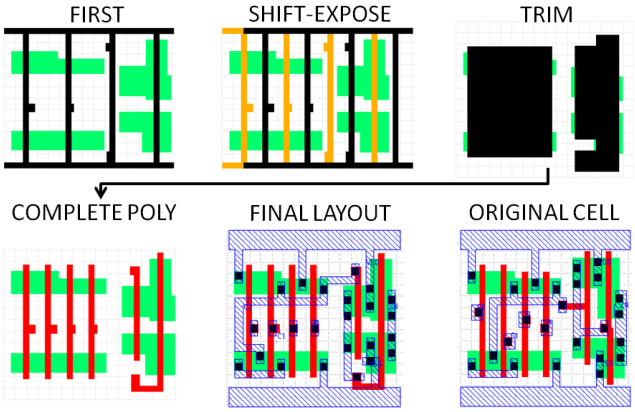


Figure 4. Example of 4-input OAI cell layout migrated for the application of ST-DPL at the poly-line layer.

ST-DPL implementation for fixed pitch poly grating is straightforward and requires no redesign effort. In this case, ST-DPL critical mask still consists of fixed-pitch grating but with a perfect $2\times$ pitch relaxation. ST-DPL for unidirectional-poly designs with non-fixed pitch requires small redesign effort. In particular, adjustment of the pitch between some lines might be necessary to enforce restriction (1). This restriction is easily met in real designs, however, because most gates are at contacted-pitch (equal to X) from at least one of its two neighbors. The critical mask for this type of designs consists of simple unidirectional lines with twice the minimum pitch of single patterning. The most challenging type of designs is conventional logic and sequential circuits that involve bidirectional-poly. To handle such designs, two lines in the opposite direction are added at the top/bottom of the critical mask of the cell leading to the ladder-like shapes illustrated in Figure 3[4]. This permits the use of "wrong-way" poly to connect gates internally within the cell in the

[3]X_0 is typically $2X$.

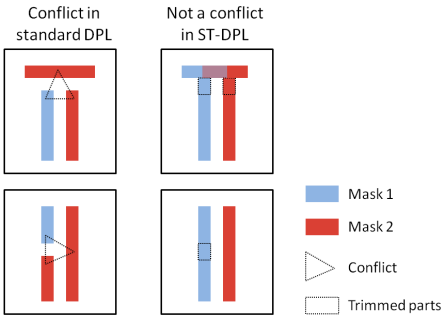


Figure 5. Examples showing how the trim exposure resolves decomposition conflicts.

top/bottom routing channels. Both critical-mask options of Figure 3 are possible without any effects on the complexity of the trim-mask. Option (a) has wrong-way lines whether they are needed or not. On the other hand, option (b) has these lines only when needed. As a results, option (b) leads to less corner-rounding than option (a). Yet, we assume option (a) in our implementation because it is very regular and, consequently, more favorable for lithography [18, 19]. In these structures, gate-pitch is twice the minimum pitch of single patterning, which ensures pitch-doubling, and small notches that appear on vertical lines correspond to contact-landing pads, which are avoidable in processes in some processes (e.g. Intel's 45nm process [12]).

For all types of designs, layout decomposition of the poly-line layer into critical and shifted exposures is trivial as we show in Section III-B. It is worth noting that the use of the trim exposures allows the elimination of layout decomposition conflicts that may occur when using standard DPL. This is because all vertical spacings are formed with the trim exposure and do not appear on the critical mask. Figure 5 illustrates some examples on how the use of a trim exposure resolves the decomposition conflicts.

ST-DPL steps applied at the poly-line layer of a 4-input OAI (OR-AND-Invert) CMOS standard-cell from Nangate 45nm open library [7] are illustrated in Figure 4. In this example, the cell-layout is made compatible with ST-DPL without any area overhead. ST-DPL application at the poly-line layer of most standard-cells is straightforward and introduces no or little area overhead as we show in the next section.

D. Layout Restrictions at Contacts Layer

ST-DPL implementation at the CA layer imposes more restrictions on the layout than in the case of poly-line layer. X being the amount of mask shift and X_0 being the minimum contact pitch, the following restrictions apply.

1. Contacts pitch is restricted similarly to gate-poly pitch. For every contact, the pitch to the neighboring contact from one side (subsequent contact to the right or left side) must be either X or $\geq X_0$ and the pitch between the left and right neighboring contacts must be $\geq X_0$.
2. Assuming the mask shift is to the right, subsequent contacts at pitch equal to X where the left contact is assigned to the first exposure and the right contact is assigned to the second exposure must be aligned to the same vertical location. Alignment of contacts is not a requirement specific to ST-DPL; it is currently performed to improve patterning quality in state-of-the-art process technologies.
3. The pitch of double-contacts is restricted to the minimum pitch X_0 on the mask (i.e. single-patterning pitch). This restriction makes diffusion double-contacts possible only for very large transistors and poly double-contacts possible only in non-condensed cells with small transistors. This restriction may not be a problem for layout methodologies that avoid double contacts because they worsen channel strain and, hence, device performance.

It is important to note that ST-DPL implementation for fixed pitch grating of contacts (e.g., similar to [20]) is trivial and requires no extra layout restrictions or redesign efforts.

Figure 6 illustrates a 4-input OAI standard-cell layout migration for combined compatibility with ST-DPL at the poly-line and CA layers. Due to the proximity of diffusion and poly contacts in the layout and the difference of their depths, it is impractical to form both types of contacts with a single exposure in sub-32nm technologies. As a result, we assume in our ST-DPL implementation that poly and diffusion contacts are formed with two separate exposures. In the example of Figure 6, $1.8\times$ pitch relaxation at the poly layer as well as the CA layer are achieved without any area overhead. $2\times$ pitch relaxation at the CA layer, however, leads to a large area overhead as we will show later in Section III-C. In both cases, ST-DPL design implementation at the CA layer leads to a reduced number of double contacts and a negligible change of the diffusion regions of certain transistors. In our implementation, a single trim mask is used for both poly and diffusion contacts patterning as illustrated in Figure 6. Unlike the trim mask of the poly layer, the trim mask of the CA layer is very basic and requires no additional changes to the design rules to simplify it.

III. STDPL Design Implementation

In this section, we demonstrate the application of ST-DPL at the poly layer for standard cell-based designs and extend ST-DPL implementation to the CA layer.

A. Limitation on Pitch Relaxation of Double Patterning

For cells to be compatible with double patterning, layouts are constructed so that no conflicts occur during decomposition of same-cell features between first and second exposures. Yet, decomposition conflicts can still occur between features of different cells whenever two cells are placed close to each other. Inter-cell conflicts are handled either by constructing cell-layouts that ensure no conflicts can occur no matter how cells are placed (e.g., as in [21]) or by detailed placement perturbation to resolve conflicts as in [22]. In this paper, we follow the former correct-by-construction approach and generate cells that guarantee a conflict-free chip layout. In this approach, the limiting factor for the pitch relaxation that can be achieved in ST-DPL *as well as standard DPL* is the spacing between features of different cells assigned to the

[4]The shape shown in this figure is for illustration purposes and do not include RET-related features.

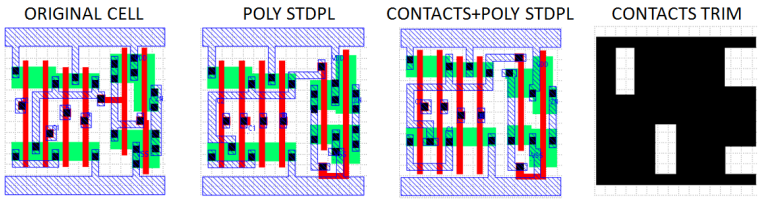


Figure 6. Example of 4-input OAI cell layout migrated for the application of ST-DPL at the poly and CA layers with 1.8× pitch relaxation.

Table I
POLY-LINE ST-DPL COMPATIBLE STANDARD-CELL LIBRARY AND ASSOCIATED AREA WITH 1.8× PITCH RELAXATION. NOTE THAT THE AREA OVERHEAD IS QUANTIZED BECAUSE OF CELL-PITCH RESTRICTIONS FROM PLACE AND ROUTE.

Cell	**Original Area** $[um^2]$	**ST-DPL Area** $[um^2]$	**Area overhead** $[um^2]$
AND2{X2, X4}	1.064/1.064	1.064/1.064	0
AND3{X1}	1.33	1.33	0
AOI211{X1}	1.33	1.33	0
AOI21{X1}	1.064	1.064	0
AOI221{X2}	1.596	1.596	0
AOI222{X2}	2.128	2.128	0
AOI22{X1, X2}	1.33/1.33	1.33/1.33	0
BUF{X1, X2}	0.798/0.798	0.798/0.798	0
CLKBUF{X1, X2, X3}	0.798/1.064/1.33	0.798/1.064/1.33	0
INV{X1, X2}	0.532/0.532	0.532/0.532	0
INV{X4}	0.532	0.532	0
INV{X8}	0.798	1.064	0.266
INV{X16}	1.33	1.596	0.266
NAND2{X1, X2, X4}	0.798/0.798/1.33	0.798/0.798/1.33	0
NAND3{X1}	1.064	1.064	0
NAND4{X2}	1.33	1.33	0
NOR2{X1, X2}	0.798/0.798	0.798/0.798	0
NOR4{X2}	1.33	1.33	0
OR2{X1, X2}	1.064/1.064	1.064/1.064	0
OR3{X2}	1.33	1.33	0
OR4{X2}	1.596	1.596	0
OAI21{X1, X2}	1.064/1.064	1.064/1.064	0
OAI22{X1}	1.33	1.33	0
OAI33{X1}	1.862	1.862	0
OAI211{X1, X2, X4}	1.33/1.33/2.128	1.33/1.33/2.128	0
XOR2{X1, X2}	1.596/1.596	1.596/1.596	0
DFF{X1}	5.054	5.054	0
SDFF{X2}	6.916	6.916	0

same exposure. By increasing the spacing between features and the left/right edges of the cell, we can trade area for pitch relaxation. Because the cell width is quantized, a small increase of this spacing can cause a considerable area increase in most cells. In ST-DPL implementation at the poly layer, 1.8× pitch relaxation is achieved without the need to modify the spacing between poly-lines and the cell edge. Whereas, 2× pitch relaxation requires a 40nm increase of this spacing and, thus, causes a significant area overhead. A larger increase of the spacing between contacts and the cell edge is necessary for ST-DPL implementation at the CA layer. Despite this fact, 1.8× pitch relaxation is achieved with a reasonable cell-area overhead as we will show in Section III-C.

B. Poly-line ST-DPL Standard-Cell Library and Mask Layout Generation

We develop poly-line ST-DPL compatible standard-cell library by manual layout migration of Nangate open cell library [7] using FreePDK [23] 45nm process design rules. Details on ST-DPL cell library are presented in Table I. Most standard-cells have fairly simple layouts and are made compatible with ST-DPL technology with little or no redesign effort. However, layout migration of large cells, which have a lot of poly landing pads and use poly to route gate signals in the horizontal direction, requires more layout modifications and effort. The primary reason for this complication comes from contact landing pads being printed in the shifted exposure whether they are needed or not. So, unless the part of the line containing the landing pad is trimmed away in the shifted version, enough room must be available so that poly-to-active spacing design rule is not violated. This requires location adjustment of active regions in some cases. For a process enabling trench contacts (e.g. Intel's 45nm process [12]), this complication is eliminated and layout migration can be easily automated. Layout modifications are performed so that transistors width and length are untouched. Yet, few diffusion regions in complicated cells (i.e. flip-flops) have to be increased/decreased by more than 2× to align PMOS and NMOS transistors. Alternatively, diffusion gaps can be introduced/removed and limit the change of the size of diffusion regions.

As discussed in Section III-A, the amount of pitch relaxation on the mask is limited by the spacing between features and the cell edge. The maximum poly-line pitch on the mask that is achieved without changing this spacing is 340nm, which corresponds to a 1.8× pitch relaxation. However, 2× pitch relaxation could still be achieved by increasing this spacing rule from 40nm to 60nm and bearing the associated area overhead.

Layout decomposition into first and second exposures is

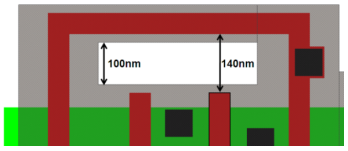


Figure 7. Poly line-tip to poly side spacing rule of 140nm to ensure a minimum hole width of 100nm.

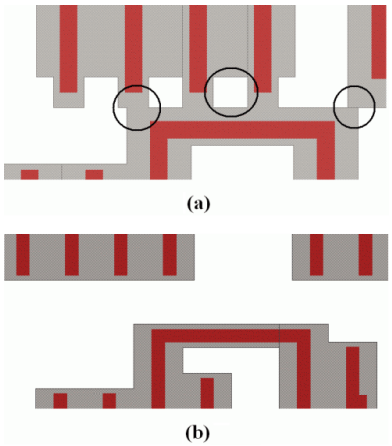


Figure 8. Trim-mask complexity at cell-boundaries before (a) and after (b) enforcing rules (2) and (3).

automated (C++ program based on OpenAccess 2.2 API [24]). Since wrong-way poly (horizontal lines of Figure 3(a)) is printed in both exposures, the decomposition problem is reduced to assigning gate-poly lines (vertical lines of Figure 3(a)) to the two exposures. Traversing each cell in the library from left to right, the following decomposition rules apply:

- if the pitch with the previous line is X, the line is assigned to the shifted-exposure (i.e. second exposure) and the previous line is assigned to the first exposure;
- if the pitch with the previous line is $< X_0$ and different than X, the line is assigned to the first exposure and the previous line is assigned to the second exposure;
- if the pitch with the previous line is $> X_0$, the line can be assigned to either of the two exposures.

Because the trim-mask covers the entire poly-layer in our ST-DPL proposed process, we start by the poly-layer as the base structure of the trim-mask and apply a series of expansions to simplify the mask. Trim-mask structures of two successive gates with pitch $< X_0$ are joined. For gates with larger pitch and gates at the cell-edge, trim-mask structures of each gate are expanded by $S_{min}/2$, where S_{min} is the minimum separation between gates (i.e. X minus gate line-width). This large trim-mask coverage of gates is to have a large resist thickness at sidewalls after development preventing etch interference with gate features under imperfect overlay and etch control (see process details in Figure 1). Trim-mask coverage of field-poly is limited to 20nm on all sides to maximize spacing between trim-mask features. Here, sidewall resist thickness requirement is much smaller than in the case of gate-poly because CD control is much less important. Since poly line-ends are formed by printing a long line in one exposure and cutting its ends in another exposure (i.e. trim-exposure), line-end tapering [25] and pull-back (a.k.a. shortening) are substantially reduced [13]. Hence, we assume line-end extension rule, which only addresses trim-to-STI overlay error and possible damage of line-end by etch in ST-DPL, can be reduced from 55nm to 35nm. With this setup, the overall margin of trim-mask overlay error is at least 20nm in X as well as Y directions.

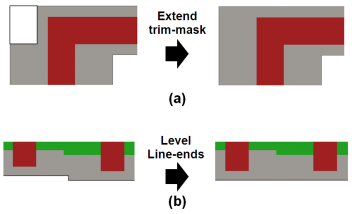


Figure 9. Trim-mask notch-fill by (a) trim-mask extension and (b) poly line-end leveling.

To guarantee an easy-to-fabricate trim-mask and quality trimming, we enforce few design rule restrictions.

1. Poly line tip-to-side and tip-to-tip within-cell spacing rules are increased from 75nm to 140nm.
2. Top/bottom "wrong-way" poly lines used for routing are pushed 35nm toward the center of the cell.
3. Line-ends are extended at most up to the starting location of "wrong-way" lines.

Rule (1) is to ensure reasonable dimensions of the holes in the trim-mask (at least 100nm wide) that can occur in such situations within a cell as illustrated in Figure 7. Rule (2) and (3) are introduced to avoid small holes in the trim-mask that might occur at cell boundaries, as illustrated in Figure 8, resulting in a relaxed separation of at least 100nm between trim-mask features of different cells.

All these rules are specific to FreePDK 45nm process that the cell library is based on and might not be needed for other process technologies. For example, rules (2) and (3) are very likely to be unnecessary (or at least smaller) for commercial processes where line-end gap is considerably larger than the minimum field-poly spacing to meet manufacturability requirements unlike in the case of FreePDK where line-end gap rule is equal to the minimum field-poly spacing. In addition, rules (2) and (3) might be avoided for a cell-library designed for ST-DPL technology rather than migrated from an existing library. In particular, the trim-mask simplification at cell-boundaries is better handled during optimization of cell-height and line-end gap rules.

It is important to note that there is a tradeoff between how critical the trim exposure is and the area overhead. Relaxing the values of the design rules listed earlier lead to a less critical trim exposure but might cause an area overhead; whereas, tight design rules lead to a more critical trim exposure but cause no area overhead. In our implementation, we have made a few sensible tradeoff points but others are possible.

A final step of trim-mask simplification is performed to avoid notches wherever possible as illustrated in Figure 9. In Figure 9(a), notch-filling is performed by extending the trim-mask coverage of field-poly. In Figure 9(b), notch-filling is performed by leveling line-ends of neighboring gates (by extension of the shorter line-end).

After generating the different masks for all cells in the library and all possible cell-orientations, mask generation for

Table II
DETAILS OF POLY-LINE ST-DPL COMPATIBLE DESIGNS SHOWING NEGLIGIBLE AREA OVERHEAD.

	Description	Cell instances	Cell-types	Flip-flops	INV/BUF	Cell-area [um^2]	Area overhead
mips789	processor core	10529	35	2011	1465	22867.5	0.02%
or1200	combinational logic	3070	35	0	890	3014.8	0.34%
usb	com. controller	478	31	93	52	880.2	0%

(a) (b)

Figure 10. Trim-mask layout snippet for poly-lines (a) and contacts (b). In (a), simple large blocks correspond to cells with unidirectional poly-lines and more complex shapes correspond to flip-flops with bidirectional poly-routing. In (b), both flip-flop and combinational logic regions have simple trim-mask features.

Table III
DETAILS ON TRIM-MASK AT THE POLY-LINE LAYER FOR THE DESIGN OF TABLE II SHOWING VERY BASIC FABRICATION REQUIREMENTS.

	Line-width [nm]	Notch Size [nm]	Hole dimensions [nm]	Overlay margin [nm]	Trim-mask fractures	Post-OPC poly fractures
MIPS789	$\geq$ 90	$\geq$ 70	$\geq$ 190 x 145	20	78597	367633
OR1200	$\geq$ 90	$\geq$ 70	$\geq$ 380 x 100	20	5189	43150
USB	$\geq$ 90	$\geq$ 70	$\geq$ 190 x 145	20	2770	14404

ST-DPL compatible designs is a simple step. For each cell-instance, cell-type and orientation are determined and mask-features are copied from the corresponding cell in the library to the instance location in the design. The generated mask layout is free of errors at cell-boundaries because critical-mask features outside the cell (or close to the cell-edge) are trimmed away and enough spacing between trim-mask features of different cells is guaranteed by construction.

Poly-line ST-DPL standard-cell library is implemented with 1.8$\times$ pitch relaxation and no area overhead compared to the original Nangate library layouts except for three cells as shown in Table I. This overhead is caused by layout restrictions imposed to simplify the trim-mask. In case these restrictions are avoided for the reasons discussed earlier, none of the ST-DPL compatible cells will have any area overhead. Moreover, if option(b) of Figure 3 is used instead of option(a), i.e. having "wrong-way" poly tracks only when needed, ST-DPL implementation of these three inverter-cells results in no area overhead because rule (2) can be avoided.

Three designs from [26] are synthesized in Cadence RTL Compiler ^{TM}v6.2 using the developed poly-line ST-DPL standard-cell library. Designs are placed and routed using Cadence SOC Encounter ^{TM}v6.2. Details on the designs and associated *cell-area* overhead are presented in Table II. *Cell-area* overhead for all three designs is negligible (at most 0.34%). The reason is attributed to low utilization of the cells where area overhead occurs (low utilization of large-size inverters is typical).

Mask layouts are automatically generated for all three designs. A snippet of trim-mask layout at the poly-line layer for the USB design is shown in Figure 10(a). In this figure, simple blocks with few vertices correspond to cells with uni-directional poly and more complex shapes correspond to flip-flops involving bidirectional poly-routing. Hence, the trim for purely unidirectional poly designs consists of extremely simple features (large rectangles mostly). Trim-mask complexity is further analyzed. In Table III, we report minimum line-width, notch size, hole dimensions, overlay margin, and number of fractures of the trim-mask. These minimum dimensions are fairly large compared to the minimum feature size of the process (i.e. 50nm) resulting in simple trim-mask for all designs. The dimensions listed in the table are not to be compared directly to dimensions of the critical-mask because trim-mask features do not define patterns but rather protect existing patterns by larger coverage. The number of fractures of the trim-mask (determined using Calibre MDP^{TM}v2008), which affects mask-cost, is 5 to 8 times smaller than the number of feature for post-OPC poly-layer (OPC generated using Calibre OPC^{TM}v2008). In addition, the trim-mask does not require expensive RET features such as OPC and SRAF which substantially increase mask-complexity and cost.

C. Poly-line Plus Contacts ST-DPL Standard-Cell Library and Mask Layout Generation

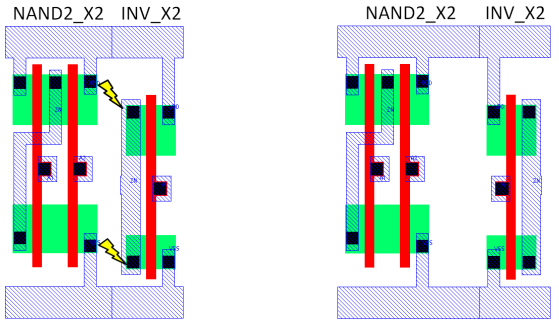
For DPL implementation (ST-DPL *as well as standard DPL*) to be possible at the CA layer without decomposition conflicts, poly contacts need to be well spaced apart from diffusion contacts. In many cells, this can result in a large area increase that makes this approach impractical. Alternatively, poly and diffusion contacts can be formed separately with different

Table IV
POLY-LINE PLUS CA ST-DPL COMPATIBLE STANDARD-CELL LIBRARY AND ASSOCIATED AREA (IN $[um^2]$) WITH $1.8\times$ PITCH RELAXATION. NOTE THAT THE AREA OVERHEAD IS QUANTIZED DUE TO CELL-PITCH RESTRICTIONS FROM PLACE AND ROUTE.

	Original	Poly ST-DPL		Poly+CA ST-DPL		Poly+Hybrid CA ST-DPL	
	Area	Area	Overhead	Area	Overhead	Area	Overhead
AND2{X2}	1.064	1.064	0	1.064	0	1.064	0
BUF{X2}	0.798	0.798	0	1.064	0.266	0.798	0
CLKBUF{X2}	1.064	1.064	0	1.064	0	1.064	0
INV{X2}	0.532	0.532	0	0.532	0	0.532	0
INV{X4}	0.532	0.532	0	0.532	0	0.532	0
NAND2{X2}	0.798	0.798	0	1.064	0.266	0.798	0
NOR2{X2}	0.798	0.798	0	1.064	0.266	0.798	0
OR2{X2}	1.064	1.064	0	1.064	0	1.064	0
OAI211{X4}	2.128	2.128	0	2.128	0	2.128	0
XOR2{X1}	1.596	1.596	0	1.596	0	1.596	0
DFF{X1}	5.054	5.054	0	5.586	0.532	5.586	0.532
SDFF{X2}	6.916	6.916	0	6.916	0	6.916	0

Table V
CELL-AREA (IN $[um^2]$) OF THREE DESIGNS SYNTHESIZED USING POLY PLUS CA ST-DPL COMPATIBLE CELLS FOR THE DIFFERENT SCHEMES.

					Original	Poly ST-DPL		Poly+CA ST-DPL		Poly+Hybrid CA ST-DPL	
	Cell instances	Cell-types	Flip-flops	INV/BUF	Area	Area	Overhead	Area	Overhead	Area	Overhead
MIPS789	20192	12	2011	3878	29733	29733	0%	33289	12%	29931	0.7%
OR1200	4240	10	0	889	3759	3759	0%	4436	18%	3759	0%
USB	674	10	93	49	1011	1011	0%	1154	14.2%	1058	4.7%



(a) (b)

Figure 11. Example of layout decomposition conflicts (marked with the arrows) between features of different cells (a) and our correct-by-construction cell layout that guarantees no conflicts (b).

exposures. In addition to the area benefit, the latter approach has improved printability because the process can be optimized separately for each type of contacts that have different depths and may even have different shapes and dimensions. The latter approach is assumed in our implementation.

As discussed in Section III-A, to resolve inter-cell layout decomposition conflicts and generate correct-by-construction cell layouts, the spacing between features and the cell edge need to be increased. In case of contacts, this increase is large because contacts can be placed very near the cell edge. To reduce the associated area overhead, we perform the following strategy. We assign the leftmost features in every cell (including cells flipped during placement) to the first exposure. In this way, when abutting two cells side by side, decomposition conflicts can occur only if the rightmost contacts of the left cell is assigned to the first exposure as illustrated in Figure 11(a). Therefore, only for those particular cells, the spacing between the rightmost contacts and the right edge of the cell need to be increased as shown in Figure 11(b). The amount of this increase to achieve $1.8\times$ pitch relaxation (345nm pitch) at the CA layer is 190nm (or a single cell-width unit in FreePDK design rules).

In ST-DPL implementation at the contacts layer, diffusion contacts are the principal cause of area overhead due to their proximity to the cell edge. To deal with this issue, we introduce hybrid ST-DPL method as a workaround. Only for cells with the rightmost diffusion contacts assigned originally to the first exposure, the method consists of assigning these contacts to be patterned with the poly contacts in a separate exposure. Consequently, no cell will have the rightmost contacts assigned to the first exposure and there is no need to increase the spacing between diffusion contacts and the cell edge as in the original CA ST-DPL implementation. It is also worth noting that, by preventing the placement of poly contacts between the horizontal location of the first/last gate and the cell edge, ST-DPL can be safely employed to form poly contacts without causing any area overhead.

For the two different styles (ST-DPL and hybrid ST-DPL), we construct a small set of compatible cells by manual layout migration of poly-line ST-DPL compatible cells that were presented in Section III-B. Table IV summarizes the implemented cells and the area overhead associated with each style. Unlike ST-DPL at poly-line layer, layout migration for ST-DPL implementation at the CA layer is a difficult task. The main reason for this complication is because contacts that are shifted replica of one another must be perfectly aligned at the same vertical location and at a pitch equal to the amount of mask shift X. Layout modifications are performed so that transistors width and length are untouched. Length of diffusion have to be increased by 5nm to ensure contacts are at a distance equal to X. Double-contacts pitch being restricted to the single-patterning pitch, double-contacts were not possible in our ST-DPL design implementation because all cells have small transistor sizes.

We synthesize the three designs used in the implementation of ST-DPL at the poly-line layer (shown in II using poly-line plus CA ST-DPL compatible cells of Table IV. Cell-area of the three designs after placement and routing for the different ST-DPL flavors are presented in Table V. Implementation of ST-DPL at poly-line and CA layers (Poly+CA ST-DPL) results in 12 to 18% cell-area increase. Whereas, poly-line plus hybrid

Table VI
DETAILS ON TRIM-MASK AT THE CONTACTS LAYER FOR THE DESIGN OF TABLE II SHOWING VERY BASIC FABRICATION REQUIREMENTS.

	Line-width [nm]	**Notch Size** [nm]	**Hole dimensions** [nm]	**Overlay margin** [nm]
MIPS789	$\geq$ 100	$\geq$ 165	$\geq$ 155 x 155	65
OR1200	$\geq$ 160	none	$\geq$ 200 x 195	65
USB	$\geq$ 100	$\geq$ 165	$\geq$ 155 x 155	65

CA ST-DPL implementation (Poly+Hybrid ST-DPL) results in a negligible cell-area increase except for USB design (4.7% increase) where the area of flip-flops constitute the largest part of the design area. It is clear from the results that the area overhead of CA ST-DPL is mainly caused by the cell-extension rule we enforce to avoid any possibility of inter-cell decomposition conflicts. This is to say that, if such conflicts are left for the placer to handle, the cell area overhead would be the same as the affordable area overhead associated with Poly+Hybrid CA ST-DPL.

Generation of mask-layout at the CA layer is similar to that of mask-layout at the poly-line layer discussed in Section III-B. A snippet of trim-mask layout at the CA layer for the USB design is shown in Figure 10(b). Here, the trim-mask layout constitute of simple features with a few number of vertices. Trim-mask complexity is further analyzed for each design. In Table VI, we report minimum line-width, notch size, hole dimensions, and the overlay margin. These minimum dimensions are fairly large compared to the minimum feature size of the process (i.e. 65nm) resulting in simple trim-mask for all designs. The dimensions listed in the table are not to be compared directly to dimensions of the critical-mask because trim-mask features do not define patterns but, rather, protect existing patterns by larger coverage. Moreover, the trim-mask does not require expensive RET features such as OPC and SRAF, which substantially increase mask-complexity and cost.

IV. ST-DPL BENEFITS

In addition to cutting mask-cost to nearly half that of standard DPL because of critical-mask reuse for both exposures and a cheap trim-mask as shown in Section III, ST-DPL has many benefits over standard pitch-split DPL in terms of overlay and CD control and throughput.

A. Overlay and Throughput Benefits

The negative dual-trench double exposure process (shown in Figure 1) has higher throughput than other processes [27]. This process does not require wafer removal from the exposure tool chuck between the two exposures (as illustrated in Figure 1). In case such process becomes feasible, its implementation in combination with ST-DPL allows the second exposure to be performed after a blind translational shift without any alignment of the second exposure. This practically eliminates any overlay error between the two patterns and, also, saves alignment time.

An important source of overlay is reticle metrology errors [28], which is caused by reticle mounting and heating as well as particle contamination of the reticle alignment marks. Since mask loading and unloading between both exposures is not necessary in ST-DPL, this source of overlay error is virtually eliminated in all ST-DPL process implementations. Moreover, reticle alignment, which is another source of overlay, is again eliminated in all ST-DPL processes for the same reason. The time spent on mask loading/unloading as well as reticle alignment is saved.

Table VII
SUMMARY OF ST-DPL OVERLAY BENEFITS.

Source	**Benefit**
All sources	almost eliminated in case of -ve LLE
Reticle/mask related	eliminated for all ST-DPL processes
Reticle alignment	reduced for all ST-DPL processes
Wafer stage	not affected

A major source of overlay is registration error ($\approx 25\%$) [29]. In DPL, registration error of the two exposures is observed to be correlated and, as a result, the impact on overlay is greatly reduced. This correlation is mainly attributed to mask-layout similarity [29, 30]. In ST-DPL, registration error is expected to have a higher correlation factor than in the case of standard DPL since mask-layout is exactly the same for both exposures.

B. Alleviating CD Bimodality Problem

Whenever two patterns are formed in different exposure and etch steps, lines and spaces have bimodal CD distributions [31] that can have severe implications for the digital design flow [32]. Because the same mask is used for both exposures in ST-DPL, mask CDU, which is the second most important contributor to the overall CD variation as reported in [31, 33], no longer affects the difference between the two distribution and the bimodal problem is alleviated.

Considering CD of the first (CD_a) and second (CD_b) patterns as random variables, then

$$\begin{aligned} CD_a &= \mu_a + m_a + nm_a, \\ CD_b &= \mu_b + m_b + nm_b, \end{aligned} \tag{1}$$

where μ_a and μ_b are the mean of CD_a and CD_b respectively, m is mask CDU random variable and nm (short for non-mask) is a random variable corresponding to all other contributors to line CDU. Assuming CD_a, CD_b, and all other random variables of Equation 2 have independent normal distributions in standard-DPL, the covariance of the two CD distributions is zero and CD difference has a normal distribution with $\mu_{diff} = \mu_a - \mu_b$ and $\sigma_{diff} = \sqrt{\sigma_a^2 + \sigma_b^2}$, where σ_a and σ_b are the standard deviations of CD_a and CD_b distributions respectively. In case of ST-DPL, $m_a = m_b = m$ and, consequently, the covariance is

$$\begin{aligned} Cov(a,b) &= E(a.b) - \mu_a \times \mu_b \\ &= \mu_a \times \mu_b + \mu_a(m + nm_b) + \mu_b(m + nm_a) \\ &\quad + m(nm_a + nm_b) + nm_a \times nm_b + m^2 \\ &\quad - \mu_a \times \mu_b \\ &= \mu_a(m + nm_b) + \mu_b(m + nm_a) \\ &\quad + m(nm_a + nm_b) + nm_a \times nm_b + m^2. \end{aligned} \tag{2}$$

Since m, nm_a, and nm_b have zero mean, Equation 3 simplifies to

$$Cov(a,b) = m^2 = \sigma_m^2, \tag{3}$$

where σ_m is the standard deviation of mask CDU normal distribution. The distribution of CD difference has

Table VIII
SUMMARY OF COMPARISON BETWEEN STANDARD-DPL AND ST-DPL METHODS.

	Standard-DPL	ST-DPL
Pitch doubling	yes	yes
Mask-cost	high	reduced
Trim exposure	no	yes
Area overhead (for 2D layouts)	small	small
Designing effort (for 2D layouts)	easy	hard
Decomposition conflicts (for 2D layouts)	yes	eliminated
CD bimodality	yes	reduced
Same-layer Overlay	yes	reduced
Throughput of critical scanner	low	slightly improved

$\mu_{diff} = \mu_a - \mu_b$ and $\sigma_{diff} = \sqrt{\sigma_a^2 + \sigma_b^2 - 2Cov(a,b)} = \sqrt{\sigma_a^2 + \sigma_b^2 - 2\sigma_m^2}$ (from Equation 3).

Using line-CDU breakdown values for LELE positive dual-line 32nm process from [31] (i.e. 2.7nm 3σ from etch, 1.4nm 3σ from mask-CDU, 0.7nm 3σ from dose, and 0.5nm 3σ from focus), σ_{diff} is 1.49nm in the case of standard-DPL and 1.34nm in the case of ST-DPL which corresponds to a 10.3% reduction in standard deviation.

C. Comparison with Popular Double-Patterning Technologies

In this section, ST-DPL technology is compared to other popular patterning techniques including standard-DPL. A summary of attributes is presented in Table VIII. ST-DPL has advantages over standard-DPL as discussed earlier. The drawbacks of ST-DPL in this comparison are higher redesign effort and the use of a trim-exposure. Because ST-DPL layouts are very regular and successive features are perfectly symmetrical, ST-DPL designs are compatible with self-aligned double patterning (SADP) technology and require little mask-assignment effort. Hence, cell/block reuse from one technology to the other is possible. Trim-exposure non-criticality allows its processing on less expensive fabrication-lines and its use permits the reduction of line-end extension rule and the elimination of layout decomposition conflicts as discussed earlier in this paper.

Another popular double-patterning technology is subtractive-litho of [12]. Essentially, subtractive-litho consists of printing a grating and removing dummy-poly with a trim-exposure. Subtractive-litho is preferred over DPL (standard and ST-DPL) because it has lower cost and less process control requirements. Although the poly grating can cause an area overhead subtractive-litho improves printability due to its imposed regular layout, this method does not achieve pitch-doubling that might be necessary to scale down to future technology nodes (beyond 32nm). Subtractive-litho can also suffer from a considerable area overhead when a poly grating is imposed as reported in [34–36].

V. CONCLUSIONS

Extreme ultraviolet (EUV) and other next generation lithography technologies such as nanoimprint and electron beam direct write [4] being potentially unready for volume manufacturing at the 22nm node [37, 38], there has been a trend toward regular and gridded layouts that allow the continuation of scaling using 193nm wavelength optical lithography [12, 18, 19, 39]. Because ST-DPL is very suitable for such layout style, the industry can make use of this lithography solution for a reduced mask-cost and improved process control of double-patterning. With the ever increasing mask cost [40], cutting this cost by almost half that of standard double patterning – achieved using ST-DPL – can significantly reduce the production cost especially for low-volume manufacturing. In case a negative dual-trench double exposure process becomes feasible, the implementation of this process with ST-DPL can virtually eliminate within-layer overlay errors. Although it may be argued that good printability can be achieved by good optimization of the illumination source in gridded layouts, we believe that pitch relaxation through double patterning will be inevitable in future technology nodes. In this paper, we also demonstrate the viability of ST-DPL in conventional bidirectional layouts. While guaranteeing no inter-cell layout decomposition conflicts, design implementation of ST-DPL at the poly-line layer is achieved with $1.8\times$ pitch relaxation with virtually no area overhead; the same pitch relaxation is achieved for ST-DPL combined implementation at poly-line and CA layers with no more than 4.7% *cell-area* overhead.

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Rani S. Ghaida (S'03) is a PhD student and researcher at the department of Electrical Engineering at UCLA and a research intern at IBM Austin Research Lab. He received the Master's degree in Computer Engineering from the University of New Mexico in 2008. His research work has been focused on semiconductor design/technology co-optimization, design for manufacturability, and yield prediction. He has several conference and journal publications in the field. Rani is a student member of the Integrated Modeling Process and Computation for Technology (IMPACT) research center, the Semiconductor Research Corporation (SRC), and major professional associations in his field including: IEEE, ACM, and SPIE.

George Torres (S'09) is a student at the University of California - Los Angeles pursuing his B.S. degree in Computer Science and Engineering. He has interned at Hewlett Packard for one summer, as well as BAE Systems, for two summers. He has been a research assistant for two years at the NanoCAD lab at UCLA where his research has focused on Double Patterning Lithography. He also has just begun as a research assistant in the new Center for Domain-Specific Computing (CDSC), also at UCLA, where his research focuses on algorithm and application speedup by use of hardware specific accelerators. George is HP Intern Scholar Leader, an Intel Scholar, Computer Science Boeing scholarship recipient, Semiconductor Research Corporation (SRC) scholar, as well as a member of SOLES, IEEE and CEED.

Puneet Gupta (S'02–M'08) is currently a faculty member of the Electrical Engineering Department at UCLA. He received the B.Tech degree in Electrical Engineering from Indian Institute of Technology, Delhi in 2000 and Ph.D. in 2007 from University of California, San Diego. He co-founded Blaze DFM Inc. (acquired by Tela Inc.) in 2004 and served as its product architect till 2007.

He has authored over 60 papers, six U.S. patents, and a book chapter. He is a recipient of NSF CAREER award, ACM/SIGDA Outstanding New Faculty Award, IBM Ph.D. fellowship and European Design Automation Association Outstanding Dissertation Award. Dr. Puneet Gupta has given tutorial talks at DAC, ICCAD, Intl. VLSI Design Conference and SPIE Advanced Lithography Symposium. He has served on the Technical Program Committee of DAC, ICCAD, ASPDAC, ISQED, ICCD, SLIP and VLSI Design. He served as the Program Chair of IEEE DFM&Y Workshop 2009, 2010.

Dr. Gupta's research has focused on building high-value bridges between physical design and semiconductor manufacturing for lowered cost, increased yield and improved predictability of integrated circuits.