Within-Layer Overlay Impact for Design in Metal Double Patterning

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***Abstract*—In double patterning lithography (DPL), overlay errors between two patterning steps of the same layer translate into CD variability. Since CD uniformity budget is very tight, meeting requirement of overlay control is one of the biggest challenges for deploying DPL. In this paper, we electrically evaluate overlay errors for back-end-of-line DPL with the goal of studying relative effects of different overlay sources and interactions of overlay control with design parameters. Experimental results show the following: 1) the expected electrical impact of overlay in a path is not significant (<6% worst-case *RC* variation) and should be the basis for determining overlay budget requirement; 2) the worst-case electrical impact of overlay in a single line remains a serious concern (up to 16.6% ΔRC and up to 50mV increase of peak crosstalk noise); 3) translational overlay error has the largest electrical impact compared to other overlay sources; and 4) overlay in *y* direction (*x* for horizontal metallization) has negligible electrical impact and, therefore, preferred routing direction should be taken into account for overlay sampling and alignment strategies. Design methods for reducing overlay electrical impact in wires are then identified. Finally, we explore positive/negative process options from an electrical perspective and conclude that positive process is preferred.**

***Index Terms*—Alignment strategy, congestion, design for manufacturability, double patterning, layout decomposition, negative process, overlay, positive process, wire spreading, wire widening.**

I. Introduction

DOUBLE patterning lithography (DPL) is one of the most likely short-term solutions for keeping the pace of scaling beyond 32 nm node [1]. DPL consists of printing patterns of the same layer using two separate exposure steps and, thus, allows a smaller pitch between features.

Overlay is the positional accuracy with which a pattern is formed on top of an existing pattern on the wafer [2]. In traditional single-exposure lithography, overlay errors occur between patterns of different layers. Design rules that define interactions between layers (e.g., metal overhang on via rule) make overlay errors less severe and reduce the requirements on overlay control (ITRS [3] estimates the overlay budget in single-exposure lithography to just 20% of the minimum feature size). Because two separate exposures are involved in DPL, overlay errors can also occur between patterns of the same layer. Such overlay errors effectively translate into CD variability [4], [5], which changes the electrical characteristics of devices and wires. In this case, design rules cannot help reducing this variability problem and, because the CD budget is already very tight (estimated by ITRS to 7% of the minimum feature size), overlay must be very well-controlled. Meeting this requirement for overlay control is seen as one of the biggest challenges for deploying DPL technology [6].

In positive dual-line process (with positive photoresist), where the line is the critical feature to be controlled [Fig. 1(a)], overlay errors translate into metal spacing variation, which affects interconnect capacitance (C). On the other hand, in negative dual-trench process (again with positive photoresist) where the space is the critical feature to be controlled [Fig. 1(b)], overlay errors translate into line width variation, as illustrated in Fig. 2, with an impact on interconnect resistance (R) as well as capacitance.

The impact of within-layer overlay on the electrical characteristics of wires has been studied in literature. A method for estimating delay variation due to overlay error is presented in [7]. A compact model to estimate interconnect delay variation due to overlay and focus variations in DPL is offered in [8]. A systematic method to compare the effects of overlay to that of CD variability on interconnect delay variation is proposed in [9]. In this paper, we extend our work presented in [10]. In particular, we electrically evaluate overlay errors for back-end-of-line (BEOL) DPL to study relative importance of different overlay sources and interactions of overlay control with design parameters and derive methods to alleviate within-layer overlay problem in DPL. In addition, we explore processing options including positive dual-line and negative dual-trench processes.

Models of overlay impact on electrical characteristics of wires in positive and negative DPL are derived in Section II. In Section III, experimental methodology and results are presented. Observations are discussed and overlay implications on design are analyzed in Section IV. In Section V, we explore processing options for next generation technology nodes. Finally, Section VI concludes with a summary and directions for future work.

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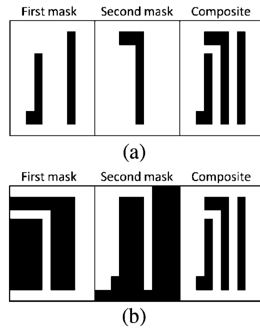


Fig. 1. Example layout with (a) positive DPL process, and (b) negative DPL process both using a positive-tone photoresist.

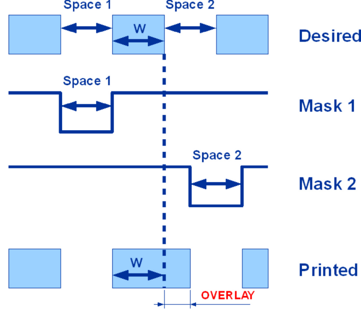


Fig. 2. Example showing translation of overlay error into CD variation in negative DPL.

II. Electrical Impact of Within-Layer Overlay

In BEOL process implemented with DPL, overlay error between two patterning steps at the same layer affects the electrical characteristics of wires. This section exhibits models for overlay and its electrical impact that are used in our experiments.

A. Overlay Modeling

Major overlay components are translation, magnification, and rotation in the wafer and field coordinate systems [11], [12] and are considered in a linear-type overlay model for overlay control and correction. High-order models can also be used to enhance overlay accuracy, but such models require more overlay sampling and excessive alignment [13]–[15]. In our study, we adopt the following widely used linear model [12]:

$$\begin{aligned}\delta_x &= T_x + M_{wx} \times X_w - R_{wx} \times Y_w + M_{fx} \times X_f \\ &\quad - R_{fx} \times Y_f + Res_x, \\ \delta_y &= T_y + M_{wy} \times Y_w + R_{wy} \times X_w + M_{fy} \times Y_f \\ &\quad + R_{fy} \times X_f + Res_y\end{aligned} \tag{1}$$

where δ_x (δ_y) is the total overlay error in the X (Y) direction. T, M, and R refer to translation, magnification, and rotation overlay parameters, respectively. Res is the residual parameter, which accounts for un-modeled secondary overlay components such as skewness and trapezoidal overlay. w and f denote the wafer and field, respectively. (X_w, Y_w) and (X_f, X_f) refer to Cartesian coordinates in the wafer and field, respectively.

Even though the model's parameters are refined continuously during processing, the model still does not correct for overlay error totally. This imperfect correction has many reasons: field to field and wafer to wafer overlay variations, limited overlay sampling that does not cover the entire wafer and lot, and un-modeled secondary overlay components.

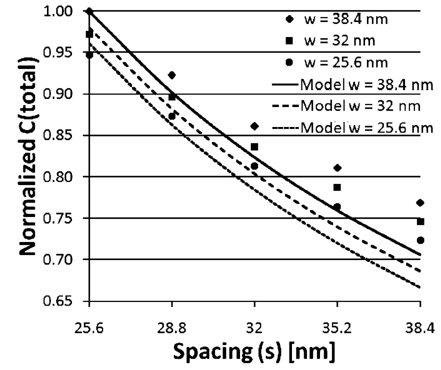


Fig. 3. Parallel plate capacitor model compared to simulation results for interconnect capacitance with varying interconnect width and spacing. Symbols represent simulated capacitances using Raphael [18] and lines represent the capacitance evaluated using the parallel plate model. Simulated and modeled capacitances are normalized with respect to their maximum values.

B. Capacitance Model

Interconnect capacitance can be evaluated using the parallel plate capacitor model or the more accurate models offered in [16] and [17]. In this paper, we use the parallel plate model to derive simple and closed form equations for the impact of overlay in DPL. In Fig. 3, we compare the model to simulation results[1] for varying interconnect width and spacing. It is clear from the figure that the model exhibits a trend similar to simulated data, but it slightly overestimates the overlay impact on capacitance variation.

C. Electrical Impact in Positive DPL

DPL can be implemented in a positive process, which prints lines, or negative process, which prints spaces [19], [20]. If positive process is implemented for BEOL, interconnect spacing (s) between the two patterns is affected leading to the change of interconnect line-to-line capacitance (C_{LL}).

We derive a closed form equation for C_{LL} between two parallel vertical lines of length L, where one line is printed perfectly and the other is printed with overlay error. Using the parallel plate capacitance model, C_{LL} can be expressed as follows:

$$C_{LL,2l} = \epsilon t \int_0^L \frac{1}{s^\star} dl \tag{2}$$

where ϵ is the dielectric constant, t is the interconnect thickness, and $s^\star$ is interconnect spacing with overlay error. Using the overlay model of (1) and converting from wafer and field coordinate system to design coordinate system, $s^\star$ is determined by

$$\begin{aligned}s^\star &= s - (T_x + M_{wx} X_o + M_x X_Q - R_{wx} Y_o \\ &\quad - R_x Y_Q + Res_x) - M_x x + R_x y + R_x L\end{aligned} \tag{3}$$

$$\text{where } R_x = R_{wx} + R_{fx}, \quad M_x = M_{wx} + M_{fx}$$

[1] Simulations are performed on Raphael, a capacitance simulation tool [18], for the structure of Fig. 4(b) and the interconnect characteristics of Table II.

where (X_o, Y_o) and (X_Q, X_Q) refer to the coordinates of field origin in the wafer plane and die origin in the field plane, respectively, and (x, y) are the coordinates of the bottom left corner of the line of interest in the design plane. Consequently, the closed form equation of C_{LL} as a function of structure coordinates in the design is

$$C_{LL,2l} = \frac{\epsilon t}{R_x} \ln \frac{s - b - M_x x + R_x y + R_x L}{s - b - M_x x + R_x y} \quad (4)$$

where $b = T_x + M_{wx} X_o + M_x X_Q - R_{wx} Y_o - R_x Y_Q + Res_x$.

Line resistance is evaluated using

$$R = \frac{\rho L}{t(w - wM_x)} \quad (5)$$

where ρ is the effective interconnect resistivity and w is the interconnect width. According to (5), the effect on R is minor since wM_x is orders of magnitude less than w.

Assuming a single ground plane in the layer below, the capacitance between the line of interest and ground plane is evaluated using

$$C_{LG} = \frac{\epsilon L(w - wM_x)}{H} \quad (6)$$

where H is the height of interlayer dielectric layer. From the equation, we note that the impact of overlay on C_{LG} is again minor.

Similar derivation is performed for a structure of three parallel vertical lines of length L where lines at the edge are printed perfectly and the middle line is printed with overlay error. The closed form equation of C_{LL} in this case becomes

$$C_{LL,3l} = \frac{\epsilon t}{R_x}\left[\ln \frac{s - b - M_x x + R_x y + R_x L}{s - b - M_x x + R_x y} + \ln \frac{s + b + M_x x - R_x y + wM_x}{s + b + M_x x - R_x y + wM_x - R_x L}\right]. \quad (7)$$

D. Electrical Impact in Negative DPL

In case of negative process, interconnect width (w) is affected, which causes interconnect resistance (R) and capacitance (C) variations.

Using the parallel plate capacitance model and overlay model of (1), closed form equations for R and C are derived in a similar manner to the derivation of R and C equations for positive DPL. Considering a structure of two parallel vertical lines where the line of interest is formed by printing one space perfectly and the other with overlay error, R of the line of interest is described by

$$R = \frac{\rho}{tR_x} \ln \frac{w - b - M_x x + R_x y - wM_x + R_x L}{w - b - M_x x + R_x y - wM_x}. \quad (8)$$

C_{LL} between the two lines is determined by

$$C_{LL,2l} = \frac{\epsilon t L}{s - sM_x}. \quad (9)$$

C_{LG} between the line of interest and ground plane of layer below is modeled by

$$C_{LG} = \frac{\epsilon L}{2H}[2(w - b - M_x x - M_x w + R_x y) + R_x L]. \quad (10)$$

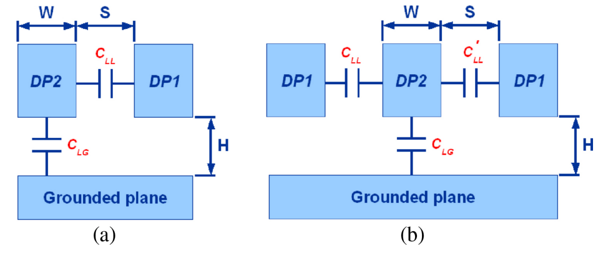


Fig. 4. Test structures used in the experiments: (a) 2-line structure; and (b) 3-line structure with single grounded plane at the layer below.

In (8)–(10), b, R_x, and M_x are the same as in (3) and (4), ρ is the wire resistivity, and H is the height of inter-level metal dielectric.

For a structure of three parallel vertical lines, R and C_{LG} are calculated using the same equations as for the 2-line structure, i.e., (8) and (10), but another equation is used for calculating C_{LL}. Assuming the space between first and second lines is printed perfectly while the space between second and third lines is printed with overlay error, C_{LL} is determined by

$$C_{LL,3l} = \epsilon t L\left(\frac{1}{s - sM_x} + \frac{1}{s}\right). \quad (11)$$

III. Experimental Methodology and Results

A series of experiments are conducted to evaluate the electrical impact of overlay in BEOL DPL. This section describes experimental setup and methodology and presents the results.

A. Experimental Setup

A 300 mm wafer with 63 33×26 mm fields each containing four copies of the same design is considered. The study is performed for BEOL 32 nm technology node (i.e., metal 1 half-pitch) at local interconnect levels with design rules adopted from ITRS [3]. Interconnect length (L) is set to 100 μm, which is close to maximum wire length for local interconnect levels where DPL is likely to be implemented.

The test structures used in the experiments are the 2-line and 3-line structures depicted in Fig. 4. In both structures, overlap capacitance (C_{LG}) is assumed to be between the line of interest and a single ground plane at the layer below. Also, lines of the first pattern are labeled as "DP1" and are assumed to be formed perfectly, while lines of the second pattern are labeled as "DP2" and are printed with overlay error. For the 2-line structure, total capacitance (C) of "DP2" wire is given by

$$C = C_{LL} + C_{LG} = C_{LL,2l} + C_{LG} \quad (12)$$

as for the 3-line structure, total capacitance (C) of "DP2" wire is given by

$$C = C_{LL} + C'_{LL} + C_{LG} = C_{LL,3l} + C_{LG} \quad (13)$$

where C_{LL} and C'_{LL} are line-to-line coupling capacitance between the line of interest and left and right lines, respectively.

In the experiments, we use *worst-case overlay*, which we assume to be equal to ITRS 3σ overlay for single patterning lithography in x and y directions (i.e., 20% of the minimum feature size). 50% of the total overlay error is assumed to *originate from un-modeled terms and random errors* and are

TABLE I
ESTIMATED OVERLAY BREAKDOWN USED IN THE REFERENCE EXPERIMENT

	% of Imperfect Correction	Exact Value [nm]
Translation	5.32%	0.34
Wafer magnification	14.18%	0.91
Field magnification	2.48%	0.16
Wafer rotation	25.53%	1.63
Field rotation	2.48%	0.16
Residual	50%	3.2

TABLE II
PARAMETERS AND CORRESPONDING VALUES USED IN THE EXPERIMENTS

Parameter	Value
Wafer diameter	300 mm
Number of fields	63
Field dimensions	33 × 26 mm
Number of dies per field	4
w	32 nm
s	32 nm
t	60.8 nm[2]
H	60.8 nm
L	100 μm
3σ overlay	6.4 nm

lumped into *Res* term; the remaining 50% is assumed to *originate from imperfect correction* of the six primary overlay components, i.e., translation, magnification, and rotation in field and wafer. This assumption conforms well to experimental results reported in [21] where, after correction with a linear overlay model and excessive overlay sampling, 58% of overlay is non-systematic error and 42% of overlay is from imperfect correction of systematic error. To study the relative importance of each overlay component, we perform a series of experiments using different scenarios of the overlay-breakdown. A set of experiments involves extreme cases where all error caused by imperfect overlay correction is from a single source: translation, magnification, rotation, field overlay, or wafer overlay. For field and wafer extreme cases, overlay from imperfect correction is split equally among translation, magnification, and rotation overlay components. In addition, we run a reference experiment with the overlay-breakdown of Table I, which is based on estimations of the required precision for overlay measurements offered in [22].

Overlay parameters in *RC* models of Section II can be inferred from the contributions of overlay components. T is equivalent to *total translation* and *Res* is *equivalent to total residual* because these two components are independent of location; whereas M_w, M_f, R_w, and R_f are inferred by considering worst-case location that happens to be at the edge of wafer and field. *Res* is assumed to be in *worst-case direction* across the entire wafer, which is the same direction as T.

All parameters used in the experiments and corresponding values are summarized in Table II.

B. Evaluation Methodology

Overlay impact on the electrical characteristics of test structures was evaluated at discrete locations of the structures in the design and for each copy of the design across the entire wafer.

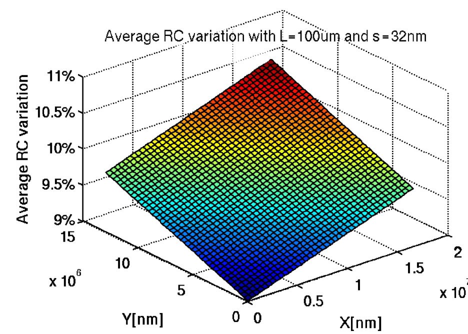


Fig. 5. Average *RC* variation for the 2-line structure as a function of its location in the design when overlay components are estimated.

We evaluate absolute worst-case impact as well as average impact over all design copies. For the case of average impact, minimum and maximum impacts for the different locations of the structures in the design are presented. The average and worst-case change of RC_{LL} and RC, which reflect the effect on interconnect delay variation, are reported for positive and negative DPL processes.

C. Results

The first set of experiments is for structures formed with positive DPL. Fig. 5 plots average *RC* variation for the 2-line structure as a function of its location in the design when overlay components are estimated. This figure indicates that ΔRC varies on average from 9% to 10.6% depending on the structure location in the design (all possible locations). Minimum variation occurs when the structure is located at the origin of the design, which is the center of the field in our experiments, and maximum variation occurs when the structure is located at the edge of the design, which is to the edge of the field. This experiment is repeated for all other overlay-breakdown cases for the 2-line and 3-line structures and average and worst-case impacts are reported. Results for positive DPL experiments are summarized in Table III.

Similarly for negative DPL, experiments for all overlay-breakdown cases are performed. Table IV summarizes the results for negative process experiments.

IV. OBSERVATIONS AND IMPLICATIONS FOR DESIGN

Experimental results are interpreted and important observations are brought forward in this section.

A. Results Analysis and Relative Importance of Overlay Sources

Results of Tables III and IV for the 2-line structure in positive and negative DPL processes are similar. In fact, with $s = w$ and same amount of line width and spacing variation, ΔRC is, to the first order, the same in positive and negative processes. In case of positive process

$$\Delta RC_{pos} = R \times \Delta C_{LL}. \tag{14}$$

In case of negative process

$$\begin{aligned}\Delta RC_{neg} &= R \times \Delta C_{LG} + \Delta R \times C_{LG} \\ &\quad + \Delta R \times C_{LL} + \Delta R \times \Delta C_{LG}.\end{aligned} \tag{15}$$

[2]Based on ITRS prediction of aspect ratio.

TABLE III

ΔRC RESULTS FOR THE 2-LINE AND 3-LINE STRUCTURES IN POSITIVE DPL

	2-Line Structure				3-Line Structure			
	Avg Variation		Worst Variation		Avg Variation		Worst Variation	
	ΔRC_{LL}	ΔRC	ΔRC_{LL}	ΔRC	ΔRC_{LL}	ΔRC	ΔRC_{LL}	ΔRC
Estimated components	11.5–13.6%	9–10.7%	21.2%	16.6%	1.5–1.6%	1.4%	3.2%	2.8%
Translation extreme	25%	19.6%	25%	19.6%	4.2%	3.7%	4.2%	3.7%
Mag extreme	7.9–14.8%	6.2–11.6%	24.9%	19.5%	1.5–2%	1.3–1.7%	4.1%	3.6%
Rotation extreme	8.6–14%	6.75–11%	23%	18%	1.4–1.8%	1.2–1.6%	3.6%	3.2%
Wafer extreme	15–15.9%	11.8–12.4%	21.8%	17.1%	1.8–1.9%	1.6–1.7%	3.3%	2.9%
Field extreme	11.6–19.6%	9.1–15.3%	23.9%	18.7%	1.4–2.4%	1.2–2.1%	3.9%	3.4%

TABLE IV

ΔRC RESULTS FOR THE 2-LINE AND 3-LINE STRUCTURES IN NEGATIVE DPL

	2-Line Structure				3-Line Structure			
	Avg Variation		Worst Variation		Avg Variation		Worst Variation	
	ΔRC_{LL}	ΔRC	ΔRC_{LL}	ΔRC	ΔRC_{LL}	ΔRC	ΔRC_{LL}	ΔRC
Estimated components	11.5–13.6%	9–10.7%	21.2%	16.6%	11.5–13.6%	10.1–11.9%	21.2%	18.6%
Translation extreme	25%	19.6%	25%	19.6%	25%	22%	25%	22%
Mag extreme	7.9–14.8%	6.2–11.6%	24.9%	19.5%	7.9–14.8%	7–13%	24.9%	21.9%
Rotation extreme	8.6–14%	6.8–11%	22.3%	18%	8.6–14%	7.6–12.3%	23%	20.2%
Wafer extreme	15–15.9%	11.8–12.4%	21.8%	17.1%	15–15.9%	13.2–14%	21.8%	19.2%
Field extreme	11.6–19.6%	9.1–15.3%	23.9%	18.7%	11.6–19.6%	10.2–17.2%	23.9%	21%

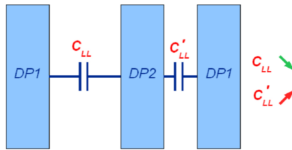


Fig. 6. Illustration of cancellation effect between line-to-line capacitances in the 3-line structure.

To the first order, ΔR is proportional to $1/\Delta w$ and C_{LG} is proportional to Δw causing $(R \times \Delta C_{LG} + \Delta R \times C_{LG})$ and $\Delta R \times \Delta C_{LG}$ in (15) to be very close to zero. Since ΔC_{LL} is, to the first order, proportional to $1/\Delta s$, then with $s = w$ and same amount of line width and spacing variation, $\Delta R \times C_{LL} \approx R \times \Delta C_{LL}$ and, consequently, $\Delta RC_{neg} \approx \Delta RC_{pos}$.

For the 3-line structure, results of positive and negative processes are substantially different. For positive DPL, ΔRC is much less in the 3-line structure (1.4% on average and 2.8% worst-case variation for the experiment of estimated components) than in the case of the 2-line structure ($9-10.7\%$ on average and 16.6% worst-case variation for the experiment of estimated components). This huge ΔRC reduction in the case of the 3-line structure is because line-to-line capacitance between the wire in the center and its left and right neighbors change in opposite directions as illustrated in Fig. 6. Hence, the total capacitance is not significantly affected. For negative DPL, Table IV shows that ΔRC is larger in case of the 3-line structure (10.1-11.9% on average and 18.6% worst-case variation for the experiment of estimated components) than in case of the 2-line structure (9–10.7% on average and 16.6% worst-case variation for the experiment of estimated components). C and R vary in opposite directions reducing the overall effect on ΔRC. For the 3-line structure, the additional C_{LL} term with the third line is unaffected by overlay resulting in the reduction of overall ΔC. This explains why ΔRC is larger in case of the 3-line structure than in case of the 2-line structure.

Relative importance of different overlay sources can be inferred from the results. For the 2-line structure, translation extreme experiment leads to 19.6% ΔRC; magnification extreme experiment leads to 6.2–11.6% average ΔRC and 19.5% worst-case ΔRC; and rotation extreme leads to 6.75–11% average ΔRC and 18% worst-case ΔRC. Translation impact on average ΔRC is much more important than magnification or rotation impact. This difference is because magnification and rotation overlay vectors can have opposite directions and their effects are canceled out when averaging over the entire wafer; whereas, translation is actually fairly uniform across the wafer.[3] Nevertheless, for worst-case ΔRC, translation, magnification, and rotation are almost equally important. Similar conclusions can be drawn from the results for the 3-line structure in case of positive and negative processes. Moreover, in both processes, magnification and rotation have very similar electrical impacts.

Results also show that field overlay has a slightly larger electrical impact than wafer overlay. In addition, field overlay is more dependent on location in the design plane, which is marked by a larger difference between minimum and maximum average variation in Tables III and IV. In practice, however, the amount of field overlay is much smaller than the amount of wafer overlay [22].

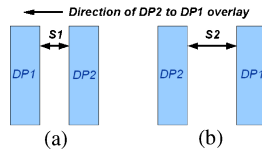
B. Effects of Design Parameters

Effects of wire length (L) and spacing (s) are evaluated by running the "estimated components" experiment for the case of the 2-line structure in positive DPL with different values of L and s. Average and worst-case RC variations are reported in Tables V and VI, respectively. These results show that the effect of L on overlay electrical impact is negligible. On the

[3]In the experiments, translation vector is assumed to have a uniform direction across wafer.

TABLE V
AVERAGE ΔRC ACROSS WAFER FOR DIFFERENT VALUES OF WIRE LENGTH (L) AND SPACING (s) IN CASE OF THE 2-LINE STRUCTURE WITH POSITIVE DPL

	s = 25.6 nm	s = 32 nm	s = 38.4 nm
L = 10 μm	13.46%	10.03%	7.91%
L = 100 μm	13.30%	9.84%	7.69%
L = 1000 μm	13.28%	9.82%	7.67%



(a) (b)

Fig. 7. Overlay impact dependence on layout decomposition in the 2-line structure with positive DPL. (a) Reduced spacing between lines for decomposition. (b) Increased spacing between lines for decomposition.

other hand, results show a large effect of s on overlay electrical impact; e.g., with 20% increase of s, ΔRC is reduced by 22% on average and 23% in the worst case. The effect of s is even larger for smaller dimension of the half-pitch; e.g., with 20% increase of s in 25.6 nm half-pitch, ΔRC is reduced by 26% on average and 28% in the worst case.

Similar experiments are run for negative DPL. Effects of wire length (L), width (w), and spacing (s) are evaluated by running the experiment for the case of the 2-line structure and estimated overlay components. Average and worst-case ΔRC are reported in Tables VII and VIII, respectively. Results show that the effect of L on overlay electrical impact is also negligible. On the other hand, results show a large effect of w and a minor effect of s on overlay electrical impact; e.g., with 20% increase of w, ΔRC is reduced by 22% on average and 23% in the worst case and, with 20% increase of s, ΔRC is reduced by 4% on average and in the worst case. The effect of w is even larger for smaller dimension of the half-pitch; e.g., with 20% increase of w in 25.6 nm half-pitch, ΔRC is reduced by 26% on average and 28% in worst case. On the contrary, the effect of s becomes smaller as the half-pitch gets smaller; e.g., with 20% increase of s in 25.6 nm half-pitch, ΔRC is reduced by 3% on average and in the worst case.

Referring to the equations describing electrical characteristics of wires, i.e., (4)–(11), overlay in y direction (x for horizontal metallization) only affects L term; since the impact of L is negligible as we demonstrated in the experiments, overlay in the y direction has virtually no electrical effects. Hence, preferred routing direction should be taken into account in overlay sampling and alignment strategies.

Significant effect of s and w in layouts fabricated with positive and negative DPL indicates the importance of wire spreading (in positive process) and widening (in negative process), which are widely used Design for Manufacturability (DFM) techniques. Nevertheless, the use of these methods is limited to non-congested regions of the layout where excess spacing is available.

C. Expected Worst-Case Overlay Impact in Critical Path

The analysis in previous sections considers a single line suffering a resistance or capacitance increase due to overlay

TABLE VI
WORST CASE ΔRC ACROSS WAFER FOR DIFFERENT VALUES OF WIRE LENGTH (L) AND SPACING (s) IN CASE OF THE 2-LINE STRUCTURE WITH POSITIVE DPL

	s = 25.6 nm	s = 32 nm	s = 38.4 nm
L = 10 μm	22.91%	16.60%	12.81%
L = 100 μm	22.90%	16.60%	12.81%
L = 1000 μm	22.86%	16.57%	12.78%

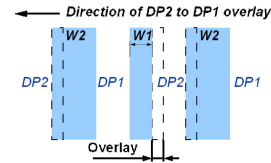


Fig. 8. Different overlay impact on wire width in negative DPL.

in the 2-line and 3-line structures. Nevertheless, overlay can cause a simultaneous resistance or capacitance decrease in other lines. In this section, we study the expected worst-case impact of overlay in a path with multiple line segments.

1) *Impact of Layout Decomposition:* In DPL, two features must be assigned to different exposures if their spacing is smaller than the required minimum spacing between features printed with the same exposure. This feature assignment between first and second exposure (a.k.a. layout decomposition) has a significant effect on the overlay impact in the 2-line structure with a positive process. Considering the 2-line structure of Fig. 7 and assuming the overlay of second exposure to first exposure is in one direction, the different decompositions of Fig. 7(a) and (b) lead to reduced spacing between lines in one case and increased spacing between lines in the other case. Layout decomposition has a significant effect on the overlay impact in negative process as well. In this case, spaces that are too close to each other are assigned to different exposures. Depending on the decomposition, some lines will see reduced width and direct neighboring lines will see an increased width as illustrated in Fig. 8. Results of Tables III and IV correspond to the line with worsened RC, i.e., reduced spacing in case of positive process and reduced width in case of negative process. We illustrate the magnitude of this decomposition effect on worst-case variation in a path with multiple line segments. Consider a path composed of two line segments where each segment is part of a 2-line structure in positive process. If both line segments have worsened RC, the worst-case interconnect ΔRC of the path is 16.6%; whereas, if one segment has worsened RC and the other segment has a relieved RC, the overall worst-case interconnect ΔRC of the path is only 2.5%.

Layout decomposition effect can be exploited to reduce ΔRC of wires on critical paths in positive process. This can be done using swizzled decomposition, where wires are split into segments and connected segments are assigned to different exposures as shown in Fig. 9. In this case, stitches need to be inserted with minor concern for manufacturability and wire resistance if enough overlap margin is ensured. The same benefit can also be achieved by actual wire swizzling (as in [23]). Actual wire swizzling, however, introduces additional vias with negative impact on wirelength and routability. Moreover,

TABLE VII
AVERAGE ΔRC ACROSS WAFER FOR DIFFERENT VALUES OF WIRE LENGTH (L), WIDTH (w), AND SPACING (s) IN CASE OF THE 2-LINE STRUCTURE WITH NEGATIVE DPL

	w = 25.6 nm			w = 32 nm			w = 38.4 nm		
	s = 25.6 nm	32 nm	38.4 nm	s = 25.6 nm	32 nm	38.4 nm	s = 25.6 nm	32 nm	38.4 nm
L = 10 μm	13.80%	13.30%	12.84%	10.28%	9.84%	9.43%	8.09%	7.68%	7.32%
L = 100 μm	13.80%	13.30%	12.84%	10.28%	9.84%	9.43%	8.09%	7.68%	7.32%
L = 1000 μm	13.80%	13.30%	12.84%	10.28%	9.84%	9.43%	8.09%	7.68%	7.32%

TABLE VIII
WORST CASE ΔRC ACROSS WAFER FOR DIFFERENT VALUES OF WIRE LENGTH (L), WIDTH (w), AND SPACING (s) IN CASE OF THE 2-LINE STRUCTURE WITH NEGATIVE DPL

	w = 25.6 nm			w = 32 nm			w = 38.4 nm		
	s = 25.6 nm	32 nm	38.4 nm	s = 25.6 nm	32 nm	38.4 nm	s = 25.6 nm	32 nm	38.4 nm
L = 10 μm	23.77%	22.91%	22.11%	17.36%	16.60%	15.91%	13.48%	12.81%	12.20%
L = 100 μm	23.77%	22.91%	22.11%	17.36%	16.60%	15.91%	13.48%	12.81%	12.20%
L = 1000 μm	23.72%	22.86%	22.06%	17.32%	16.57%	15.88%	13.45%	12.78%	12.17%

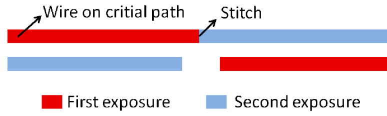


Fig. 9. Illustration of swizzled decomposition to reduce ΔRC of wires on critical paths.

timing-aware layout decomposition strategies (e.g., [24]) can be very useful for improving timing yield.

2) *Impact of Congestion:* Results of Table III for positive DPL show a much larger overlay impact in case of the 2-line structure than in case of the 3-line structure. On the contrary, results of Table IV for negative DPL show a larger overlay impact in the case of the 3-line structure than in the case of the 2-line structure. This dependence of overlay impact on the wire neighborhood gives motivation for considering congestion in electrical evaluation of overlay impact. Given the average congestion G in a layout, we estimate the probability of a line to have two neighboring lines (i.e., 3-line structure), one neighboring line (i.e., 2-line structure), and no neighbors (i.e., 1-line structure). This is done by considering three channels where each is occupied by a wire with probability equal to G. The probability of 3-line structure, P_{3l}, is G^3, the probability of 2-line structure at minimum spacing,[4] P_{2l}, is $G^2 \times (1 - G) \times 2$, and the probability of 1-line structure (only middle channel is occupied), P_{1l}, is $G \times (1 - G)^2$. Hence, the expected ΔRC of a randomly chosen line from the layout is

$$\begin{aligned}\Delta RC_{avg} &= \Delta RC_{3l} \times P_{3l} + \Delta RC_{2l} \times P_{2l} + \Delta RC_{1l} \times P_{1l} \\ &= \Delta RC_{3l} \times G^3 + \Delta RC_{2l} \times G^2 \times (1 - G) \times 2 \\ &\quad + \Delta RC_{1l} \times G \times (1 - G)^2. \end{aligned} \tag{16}$$

In positive DPL process, $\Delta RC_{1l} = 0$ because overlay has no effect on 1-line structure. In negative DPL process, overlay can result in line width variation in 1-line structure. Nevertheless, R and C_{LG}, which is the only capacitance term in this case, varies in opposite directions rendering the overall ΔRC_{1l} negligible. Using (16) and ΔRC_{2l} and ΔRC_{3l} values for the case of estimated overlay components in Table III (worst-case variation), we plot in Fig. 10(a) interconnect ΔRC of a path as a function of congestion for the case of positive process. This is performed for different splits of line segments in the path between worsened and relieved RC, namely, 50 to 100% of lines with worsened RC with 10% intervals and the remaining fraction of lines having a relieved RC. When assuming all line segments in the path have a worsened RC (i.e., most pessimistic worst-case split), interconnect worst-case ΔRC is at most 5.9% (for 72% congestion) and is less than 4.7% for highly congested layouts (90% and more). When assuming a 50-50% split of lines between worsened and relieved RC (i.e., most optimistic best-case split), interconnect worst-case ΔRC is at most 2.8%, which occurs at a 100% congestion.

The same plots are reproduced in Fig. 10(b) for the case of negative process. Here, if all line segments in the path are assumed to have a worsened RC (i.e., most pessimistic worst-case split), interconnect worst-case ΔRC increases monotonically to reach 18.6% at 100% congestion. When assuming a 50-50% split of lines between worsened and relieved RC (i.e., most optimistic best-case split), interconnect worst-case ΔRC increases monotonically to reach 2.8% at 100% congestion.

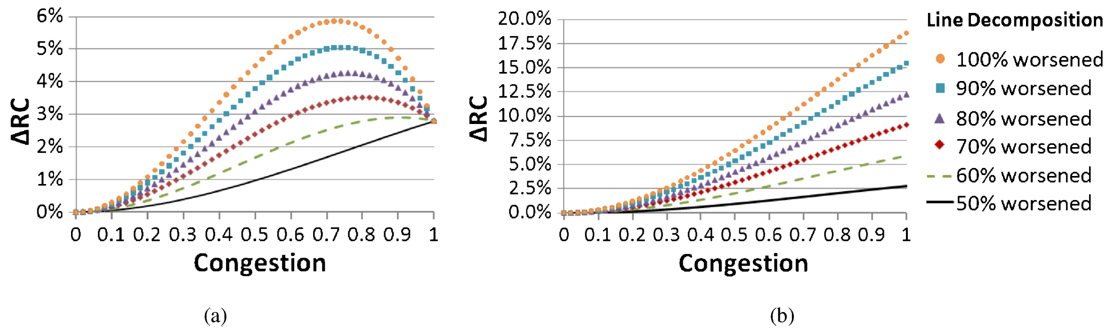
In Fig. 10(a) and (b), we assume an overlay budget equal to 20% of half-pitch, i.e., ITRS projected overlay budget for single patterning. In Fig. 11, we repeat the same experiments with an overlay budget of equal to 7% of half-pitch, which corresponds to ITRS projected CD budget for single patterning. In this case, overlay impact is small indicating that having a double patterning overlay budget equal to single patterning CD budget is certainly too conservative.

Congestion benefit can be exploited to reduce ΔRC in positive process. This is achieved by dummy fill insertion, which is also used to improve planarity.

D. Overlay Impact on Crosstalk Noise

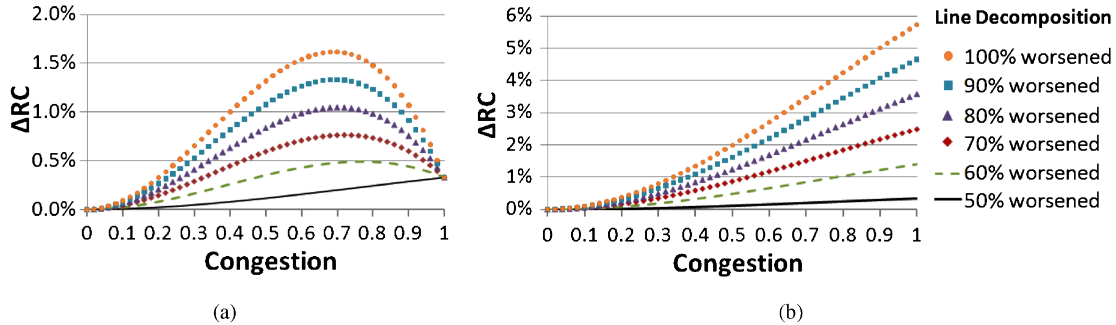
Adjacent lines are susceptible to crosstalk noise, which can lead to signal integrity issues when the noise amplitude exceeds some threshold for a duration long enough to cause a bit flip. A widely used measure of crosstalk noise is the maximum voltage change (a.k.a. peak crosstalk voltage) of the victim

[4]Multiplication by two accounts for the two possible locations of the 2-line structure, occupying either first two channels or last two channels.



(a) (b)

Fig. 10. Plot of path interconnect worst-case ΔRC versus congestion for different line splits between worsened and relieved RC variation in (a) positive DPL process, and (b) negative DPL process. The plots assume an overlay budget equal to 20% of half-pitch.



(a) (b)

Fig. 11. Plot of path interconnect worst-case ΔRC versus congestion for different line splits between worsened and relieved RC variation in (a) positive DPL process, and (b) negative DPL process. The plots assume an overlay budget equal to 7% of half-pitch.

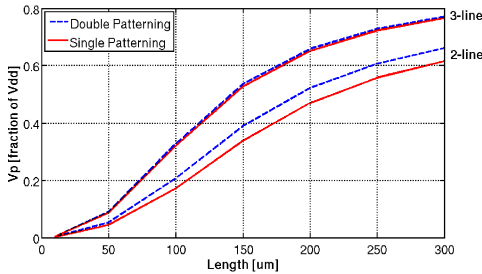


Fig. 12. Peak crosstalk noise versus interconnect length in positive DPL process.

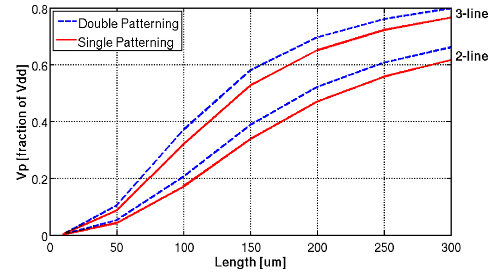


Fig. 13. Peak crosstalk noise versus interconnect length in negative DPL process.

line. Using a simplified lumped RC model, the peak crosstalk voltage is determined using the following model [26], [27]:

$$V_p = \begin{cases} V_{dd}\frac{R_v C_{LL,2l}}{t_f}(1 - e^{-(t_f)/R_v C}) & \text{for2} - \text{linestruct} \\ V_{dd}\frac{R_v C_{LL,3l}}{t_f}(1 - e^{-(t_f)/R_v C}) & \text{for3} - \text{linestruct} \end{cases} \quad (17)$$

where V_{dd} is the supply voltage, R_v is the resistance of the victim line, t_f is the rise time at the aggressor line, and C is the total capacitance of the victim line.

In Fig. 12, we plot the peak crosstalk voltage as a function of the length of adjacent lines for the 2-line and 3-line structures in 32 nm half-pitch for positive single and double patterning processes. Here, we assume a clock frequency of 2 GHz, t_f equal to 1/8 of the clock period (i.e., 62 ps), and effective resistivity of 48.3Ω-nm and effective dielectric constant of 2.6 that are the values projected by ITRS. Compared to single patterning, V_p in the case of double patterning is slightly higher by at most 0.05 of V_{dd} (e.g., 50 mV for V_{dd} =1-V) in the 2-line structure and is less than 0.01 of V_{dd} (e.g., <10 mV for V_{dd} =1-V) in the 3-line structure. The same study is repeated for negative DPL process and plots are reproduced in Fig. 13. For the 2-line structure, we observe the same results as in the case of positive process; however, results for the 3-line structure are substantially different. Compared to single patterning, V_p in the case of double patterning is slightly higher by at most 0.05 of V_{dd} (e.g., 50 mV for V_{dd} =1-V). This disparity between the results in positive and negative processes is attributed to the ΔC cancellation effect for the 3-line structure in positive process, which is absent in negative process.

E. Estimation of Overlay Requirement

Reduction of overlay budget requires challenging and expensive overlay control and alignment strategies. In some cases, this might even necessitate the replacement of scanners by newer ones with better alignment accuracy. As a result, determining how much overlay is "really" required can avoid unnecessarily tight and costly overlay control.

Even though overlay error translates into CD variation in DPL, our conjecture is that overlay requirement can be

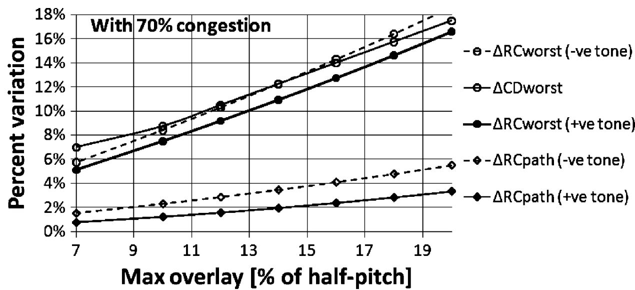


Fig. 14. Plots of average and worst case CD and C variations versus requirement of maximum overlay with 70% congestion in positive and negative DPL.

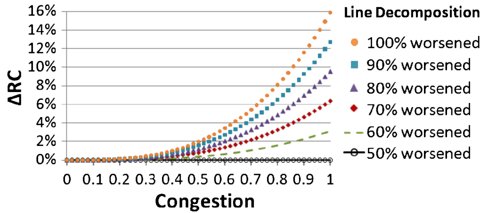


Fig. 15. Difference between worst-case interconnect ΔRC for a path in positive process and negative process as a function of congestion for different line splits between worsened and relieved RC variation.

alleviated if electrical variation is the basis for determining the requirement rather than CD variation, which may lead to excessively constricted budget [25].

In Fig. 14, absolute worst-case ΔRC in a single line and worst-case CD variations in positive and negative DPL processes are plotted. Even when considering absolute worst-case electrical variation in a single line, overlay requirement determined from electrical variation tolerance is significantly smaller than that determined from CD variation tolerance in positive process; e.g., 10% electrical variation tolerance in case of absolute worst-case ΔRC requires overlay < 4.3 nm, while the same CD tolerance requires overlay < 3.8 nm; this consists of a 13% reduction of overlay requirement. Fig. 14 also plots worst-case ΔRC in a path at 70% congestion (i.e., worst-case congestion in positive process) and assuming 70% of line segments of the path have a worsened RC and the remaining segments have a relieved RC. In this case, overlay requirement is greatly alleviated when electrical variation, instead of CD variation, is used to determine the requirement. For positive process, overlay requirement determined using worst-case ΔRC in a path is 5–9 times smaller than that determined using absolute worst-case CD variation. Similarly for negative process, overlay requirement determined using worst-case ΔRC in a path is 3–5 times smaller than that determined using absolute worst-case CD variation.

V. Exploring Processing Options

From the manufacturing perspective, negative dual-trench process is preferred over positive dual-line process because it requires less processing steps and the first pattern is better protected from the processing steps of the second pattern (i.e., exposure and etch) in negative process [6].

Positive process yield better *patterning quality* than negative process. In particular, positive process has a larger exposure latitude and smaller Mask Error Enhancement Factor and Line-End Roughness than negative process [6], [19].

Layout decomposition between first and second exposures is much more complex in the case of negative process than in the case of positive process as can be inferred from Fig. 1. The complication in negative process is attributed to the fact that the final pattern is formed by trimming unwanted area through either the first or second patterning steps, which substantially increases the number of possible decompositions for the same layout.

From the *electrical perspective*, experimental results of Table III and IV show that the absolute worst-case electrical variation in positive process (ΔRC for the 2-line structure) is slightly smaller than that in negative process (ΔRC for the 3-line structure), namely, ΔRC of 16.6% in positive process and ΔRC of 18.6% in negative process. Moreover, the expected worst-case electrical variation for a path is much smaller for the case of positive process than in the case of negative process. In Fig. 15, we plot the difference between this variation for positive process and negative process as a function of congestion for different line splits between worsened and relieved RC variation. The difference increases with the level of congestion and more pessimistic assumption on the line-split between worsened/relieved RC variation to reach up to 16% of ΔRC. This large difference between the results of positive process and that of negative process is attributed mainly to the cancellation effect between line-to-line capacitances in the 3-line structure, which only occur in positive DPL process.

As for signal integrity issues, we observe identical results in positive process and negative process if the worst case crosstalk noise is assumed to occur in the 2-line structure (i.e., single aggressors); whereas, if the worst case crosstalk noise is assumed to occur in the 3-line structure (i.e., two aggressors), positive process results in a much smaller increase of peak crosstalk noise compared to negative process as demonstrated in Section IV-D (less than 0.01 of V_{dd} versus 0.05 of V_{dd}).

As a result, positive process is preferred over negative process from an electrical perspective at 32 nm half-pitch. This conclusion is expected to remain valid at future technology nodes independent of scaling as long as $s = w$ as we have shown in Section IV-A.

VI. Conclusion and Future Work

In this paper, we electrically evaluated overlay impact in positive and negative DPL processes. Experimental results show that the expected electrical impact of overlay in a path is not severe especially when congestion and layout decomposition effects are considered. On the other hand, the absolute worst-case electrical impact of overlay in a line remains a serious problem (up to 16.6% ΔRC and up to 50 mV increase of peak crosstalk noise). Many methods are available for designers to reduce the absolute and expected overlay impacts, especially in critical paths, including wire spreading and widening, swizzled decomposition, and dummy fills. As a result, overlay requirement can be relaxed if electrical variation, rather than CD variation, is the basis for determining

the requirement. Furthermore, we analyzed process options for 32 nm half-pitch node and conclude that positive process is the preferable process option from an electrical perspective. Our study of the relative importance of different overlay sources reveals that translation overlay has the largest electrical impact among all the sources. In addition, overlay in y direction (x for horizontal metallization) has negligible electrical impact. Therefore, preferred routing direction should be taken into account for overlay sampling and alignment strategies. In future work, we will extend the results to cover front-end-of-line layers and try to relax overlay requirements by developing DPL-specific and design-aware alignment strategies.

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