Electrical Modeling of Lithographic Imperfections

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***Abstract*—Lithographic wavelength of 193nm has been used for past few generations of patterning and is likely to remain in use for next few technology generations (at least till 28nm technology half-node) as well. This deep sub-wavelength patterning has resulted in wafer shapes not resembling drawn rectilinear shapes. The resulting non-rectangular devices and wires are not handled by current generation modeling and analyses methods. In this paper, we present a survey of electrical modeling methods for such lithographic imperfections especially on transistor layers. We also discuss use contexts of such models as well as briefly present electrical implications of the likely future patterning candidate, namely double patterning.**

I. Introduction

Lithography has been the key enabler of Moore's law scaling. Several resolution enhancement techniques (RETs) and design for manufacturability (DFM) methodologies have allowed the semiconductor industry to keep using 193nm wavelength illumination to print as small as 32nm half-pitches. Unfortunately, even with these "tricks", sub-wavelength patterning has resulted in breakdown of WYSIWYG paradigm with (complex, non-rectilinear) silicon shapes not necessarily resembling the (simple, rectilinear) drawn geometries (e.g., lithography simulation contour in Figure 1 shows that transistor channels and line-ends are not rectilinear.). A wafer-shape based power and performance signoff is desirable for RET validation as well as for "closest-to-silicon" analysis. Existing compact device models (e.g., BSIM) and interconnect extraction techniques do not handle complicated non-rectangular geometries. In this paper, we review models of non-rectangular devices and their use contexts. Further, we briefly review electrical modeling of imperfections in double patterning lithography: the most likely sub-32nm patterning candidate.

A. Patterning methods - now and future

Innovative resolution enhancement techniques (RETs) such as optical proximity correction (OPC), immersion lithography, off-axis illumination, sub-resolution assist features, and phase-shift mask have successfully extended 193nm optical lithography well beyond its resolution physical limit. Scaling beyond 32nm technology node is likely to necessitate, however, more radical patterning solutions. Extreme ultraviolet (EUV) and other next generation lithography techniques such as nanoimprint and electron beam direct write [1] being potentially unready for volume manufacturing at the 22nm node [2,3], other alternative solutions have been proposed to preserve timely scaling:

- double patterning lithography (DPL) where patterns of the same layer are formed with two separate exposure/etch steps [4];
- interference assisted lithography which consists of printing a 1D grating in a first exposure and removing unwanted features with a subsequent trim-exposure [5];
- and source-mask optimization [2,7] with a limited set of layout-patterns to ensure manufacturability [6].

Unfortunately, all these patterning solutions impose restrictions on the layout and carry serious challenges and implications on the design. DPL being the most favored, we study the electrical impact of its imperfections later in the paper.

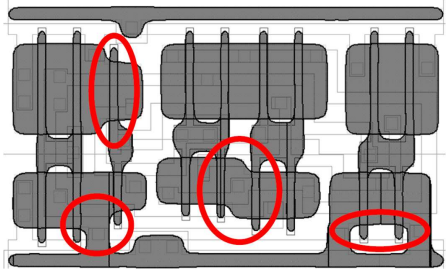

Figure 1. Lithography simulation contour showing non-rectangular gate transistors and line-end imperfections in a layout at 90 nm technology node. [60].

B. Where are electrical models of patterning imperfections needed?

Several use contexts of these models exist. The important ones are briefly discussed below.

- Cell Characterization. Power/timing characterization of standard cells based on lithography simulated wire/device shapes is the most obvious and least intrusive use of the non-rectangular device models and has seen some adoption. The problem here is of using a representative context in which to simulate the cell. Approaches have ranged from generating representative/multiple contexts [73,74] to methodologically isolating the cell from surroundings (e.g., by using auxiliary patterns [75]).
- Electrically Driven OPC. Driving resolution enhancement with design/electrical intent has been shown to have accuracy, runtime and cost benefits over traditional geometric correction [70,71]. All proposed electrically driven OPC methods (e.g., [72]) require models to convert simulated shape to current values. The models used here are likely to be simple to permit very fast evaluation and not require any interaction with actual circuit simulation.
- Design Rule Optimization. Evaluating design rules benefits from simulation followed by electrical impact analyses of rule values [69].
- Contour-based Design Analyses. Analyzing full-chip power/performance after lithography simulation will give more accurate results compared to either relying on nominal shapes or simulation contour-based cell characterization (as full-chip analysis does not ignore the long-range layout context) [67,68]. Unfortunately, without a lot of "tricks" this is impractical due to high simulation runtime as well almost complete flattening of the design (due to uniquification of all cell instances post-simulation).
- Transistor Shape Optimization. Drawing intentionally non-rectangular transistors has also been proposed using such models [77] to optimize delay-leakage tradeoffs.

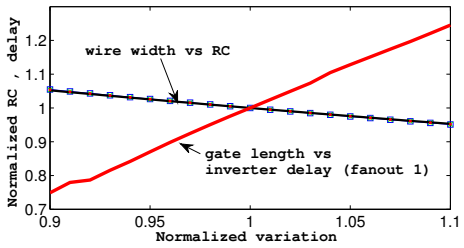

Figure 2. Sensitivities of wire RC and gate delay to patterning variation.

C. Lithography simulation methods

Lithography simulation methods can be classified according to their accuracy into two categories.

- Full-blown physical models with electromagnetic field simulation available in commercial tools(e.g., PROLITH [8] and Sentaurus-Lithography [9]) as well as academic tools (e.g, SAMPLE by UC Berkeley [10]). This type of simulation is extremely accurate but can take tens of minutes even for a few microns by few microns layout. It is used for process development, numerical aperture and illumination optimization, and process window prediction.
- Approximate imaging models [11,12] with less accuracy than full-blown models [13] but considerably faster enabling their use in full-chip optical proximity correction (OPC) (e.g., Calibre nmOPC [14]) and DFM modeling.

The need for lithography simulation in various applications has triggered research to speed it up (e.g., using compact approximate models [15,16], predictive models fitted to simulated test-patterns [17], and hardware acceleration [18]).

D. Are wires important?

An early study by Nassif [42] shows that delay variation due to gate length is about 2X larger than that due to wire width[1]. However, based on the parameters from FreePDK 45nm process [43] and capacitance model in [44], the impact of gate length variation has increased to 5X the impact of wire width as shown in Figure 2. Simulation results in Table I verify that delay and power are not sensitive to linewidth variation, which agrees with the results of [45]. It is worth noting that the impact of wire width variation is exaggerated as our experiment ignores the cancellation of power and delay variation due to averaging over long wires.

II. Non-rectangular transistor modeling

In sub-wavelength patterning, line-ends and transistors' channel are no longer rectilinear as depicted in Figure 1. There have been some commercial attempts on modeling non-rectangular gate (NRG) transistor (e.g., a shape-to-electrical engine is developed in [46] by fitting empirical equations based on transistor shapes and their corresponding electrical parameters.).

A. Polysilicon rounding

Many studies have been conducted to model MOSFET's electrical parameters (I_{on} and I_{off}) to account for channel irregularities due to polysilicon variation [47]–[57].

They account for polysilicon rounding and line-edge roughness by modeling a NRG transistor as multiple rectangular transistors

[1]Interconnect thickness variation is not considered because it is irrelevant to lithography imperfection.

Table I
LINEWIDTH-INDUCED POWER AND DELAY VARIATION FOR A DECODER IMPLEMENTED USING 45NM TECHNOLOGY [43]

Interconnect layers (variation)	Δ delay (%)	Δ Switching power (%)
M2 (+10%)	0.89	1.46
M2 (-10%)	-0.75	-0.69
M3 (+10%)	1.90	2.83
M3 (-10%)	-1.62	-1.85
M4 (+10%)	0.77	1.64
M4 (-10%)	-0.65	-0.84
M5 (+10%)	0.08	0.50
M5 (-10%)	-0.07	0.13
M6 (+10%)	0.22	0.65
M6 (-10%)	-0.19	0.00

Total gates=43K Total area=0.2mm^2

Table II
NARROW WIDTH EFFECT SOURCES AND THEIR IMPACTS.

Variation sources	$V_{th\ edge}/V_{th\ center}$[2]
Fringe capacitance	<1
Well proximity	≥ 1
Stress[3]	≤ 1

connected in parallel. To improve the accuracy of leakage current estimation, a location dependent V_{th} model is proposed in [53] and used in [55]. Many sources, modeled by narrow width effect parameters in BSIM [33], contribute to this "edge effect". The variation sources can affect V_{th} in different ways as indicated in Table II [34,65].

As illustrated in Figure 3, effective current (I_{eff}) of a NRG transistor is approximated as the sum of the currents of rectangular transistors. Subsequently, an equivalent gate length (EGL) is fitted to form a rectangular transistor, which matches the corresponding I_{eff} [47]–[53], [55]. Since the impact of irregular channel length depends on transistor working state, EGL_{on} and EGL_{off} are extracted for timing and leakage analyses, respectively. EGL approach is highly compatible with circuit simulation tools as it can be implemented easily by changing channel length. However, extracted EGL is only accurate at the bias point where I_{eff} is calculated. To account for this problem, EGL is expressed as a function of V_{gs} in [54] to yield a smooth transition between on and off states. This method enables a unified model for simulating NRG transistors under different bias points but dependency of EGL on V_{ds} is not

[2]$V_{th\ edge}/V_{th\ center}$ is the ratio of V_{th} at transistor edges to V_{th} in the middle of channel.

[3]The impact of stress varies for different devices or processes.

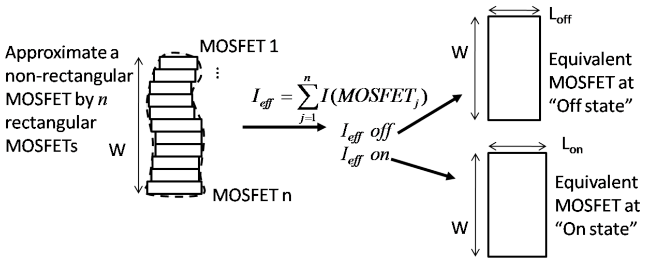

Figure 3. EGL extraction flow

Table III
COMPARISON OF LEAKAGE, DELAY, AND SETUP TIME FOR A 65NM DFFX1 BETWEEN NOMINAL AND W/ ACTIVE LAYER ROUNDING EFFECT.

		nominal	w/ active rounding	delta (%)
leakage (nW)		138.69	83.49	39.8
CLK to Q (ps)	fall	70.57	68.54	2.9
	rise	76.07	74.07	2.6
Setup time (ps)	fall	20.43	18.08	11.5
	rise	42.71	35.01	18.0

taken into account. In [57], every NRG transistor is connected in parallel to a pre-characterized voltage-dependent current source that accounts for changes in I_{ds} due to irregular channel shape. Since the pre-characterized current source is fitted for all operation regions, this approach is accurate for timing, leakage and transient analyses. Alternatively, non-rectangular transistor is represented by a limited number of transistors in [56]. Though this method improves the accuracy of EGL approach, the number of total transistors and simulation runtimes are increased.

B. Active and combined polysilicon/active rounding

As shown in Figure 1, active layer is distorted whenever transistors with different channel widths share the same active region or active routing is used to make power/ground connections [58]. This leads to a larger source or drain, which has significant impact on circuit performance as shown in Table III [60]. Active layer rounding effect is first considered in [59], whereby non-rectangular active region is approximated by an average channel width. Later, Gupta *et. al.* [60] proposed a model for NRG transistor based on empirical equations fitted to Technology Computer-Aided Design (TCAD) simulation data. The average modeling error is 0.9% for I_{on} and 3.5% for I_{off} but drain side rounding is not considered. Moreover, due to the empirical nature of the model, early evaluation of active rounding is not possible for new technologies or process setups.

Alternatively, a physically derived model is proposed in [61], which can be calibrated using circuit simulation rather than TCAD or silicon data. In [61], the channel of active-layer rounded transistor is sliced into narrower trapezoidal or rectangular transistors according to current directions. Consequently, every transistor slice has its own channel length and width[4]. The transistors associated with their respective V_{th}, channel length and width are simulated using existing tools [33] to obtain I_{eff} at a bias point. Subsequently, L_{eff}, W_{eff} and ΔV_{th} are extracted to form an equivalent rectangular transistor that matches I_{eff} and gate area (for capacitance). This method is similar to the EGL approach where two sets of parameters are required for delay and leakage analyses. Figure 4 shows that the impact of a larger source and that of a larger drain are asymmetrical. Since transistors with short channel length and narrow width are sensitive to charge sharing effect, unequal source and drain widths on trapezoidal transistor cause a change in V_{th}. Besides, transistors with rounded active layer have better I_{on}/I_{off} ratio compared to the rectangular reference transistor.

Further, Chan *et. al.* [61] extend their active rounding model to account for transistors with combined poly and active rounding by a slicing approach illustrated in Figure 5[5]. The slicing method approximates drain and source width of transistors (W_{d_i} and W_{s_i}) guided by straight lines orthogonal to the vector of channel length, $\vec{L}$. The rest of the modeling procedures are the same as the ones for

[4]An equivalent width for trapezoidal transistor is derived in [61].
[5]Middle of channel is approximated by rectangular transistors.

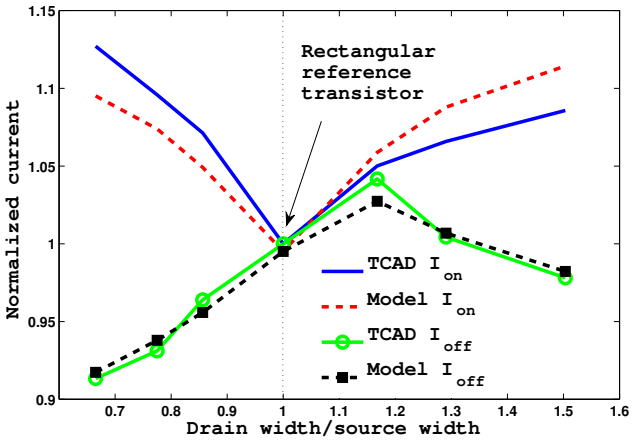

Figure 4. Model [61] vs TCAD (NMOS).

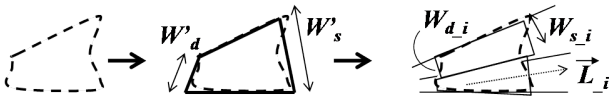

Figure 5. Edge section slicing for a transistor with combined active and poly rounding.

active layer rounding mentioned earlier. Table IV[6] shows that both TCAD and SPICE calibrated models proposed in [61] are accurate and differences between the results of the two models are small. The average error for TCAD and SPICE calibrated models proposed in [61] are 1.6% and 1.7%, respectively.

C. Line-end lithography imperfections

Line-end pull back is a patterning imperfection originating from a combination of low-k1 lithography and acid diffusion in chemically amplified resists [63]. The patterning imperfection can be alleviated by extending and shaping line-ends [62,64] or by using advanced patterning such as interference assisted lithography [5]. As illustrated in Figure 7, with misalignment the line-end is overlapped with active region and the channel length at transistor edge is affected. Moreover,

[6]Geometry parameters of NRG transistors are defined in Figure 6.

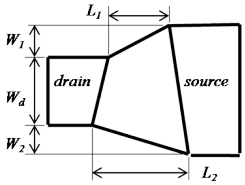

Figure 6. Description of a transistor with combined active and poly rounding.

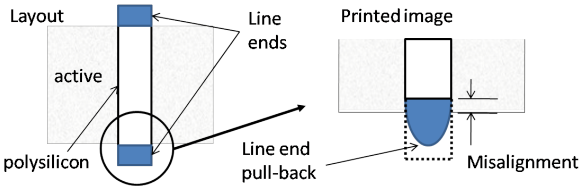

Figure 7. Lithography imperfections on line-end.

Table IV
MODELING ERRORS FOR TCAD AND SPICE CALIBRATED MODELS.

	L_1 (nm)	L_2 (nm)	W_d (nm)	W_1 (nm)	W_2 (nm)	Error (%) TCAD calibrated I_{on}	TCAD calibrated I_{off}	SPICE calibrated I_{on}	SPICE calibrated I_{off}
Source	45	45	155	26	0	-2.1	-0.8	-2.0	-0.5
side	45	45	155	45	0	-2.0	0.7	-1.9	1.1
larger	45	45	155	78	0	-2.8	0.4	-2.7	0.7
Drain	45	45	171	-26	0	0.8	-1.4	0.8	-2.3
side	45	45	200	-45	0	2.1	0.3	2.0	-0.7
larger	45	45	233	-78	0	2.6	0.4	2.5	-0.5
Polysilicon	55	45	155	0	0	NA	NA	-0.7	2.5
rounding	35	45	155	0	0	NA	NA	-0.2	7.5
Polysilicon	55	45	155	45	0	NA	NA	-1.4	3.1
and	55	45	155	0	45	NA	NA	-2.8	-2.7
active	35	45	155	45	0	NA	NA	-2.4	0.7
rounding	35	45	155	0	45	NA	NA	-0.7	7.8

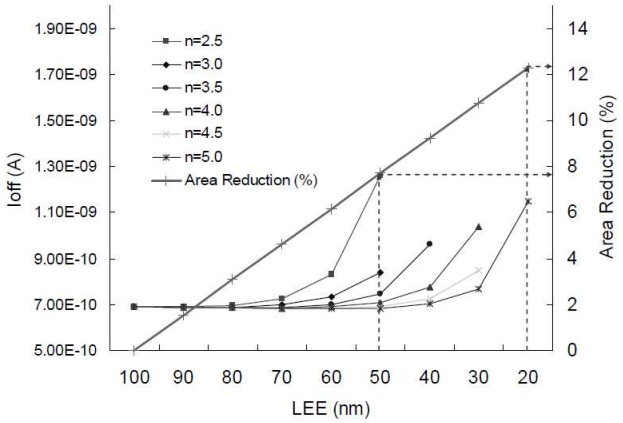

Figure 8. Area-leakage tradeoff for an 6t SRAM bitcell. Higher N implies better OPC and more rectangular line-ends.

the shape of line-end changes the fringe capacitance between line-end and transistor channel. As indicated in Table II, fringe capacitance is a source of narrow width effect [65]. Therefore, changes in line-end will lead to V_{th} and current variation. To account for line-ends imperfections, Gupta *et. al* [64] discretize line-ends to model total fringe capacitance as the sum of fringe capacitance of each line-end segment and gate edges capacitances. Subsequently, the impact of fringe-capacitance-induced narrow width effect is modeled by fringe capacitance dependent I_{on} and I_{off} equations. Meanwhile, channel irregularity due to misalignment is considered by slicing transistor channel into rectangular transistors connected in parallel. Based on the model, line-ends shapes and design rule are explored in [64] for layout area and leakage power reductions. Figure 8 shows the area-leakage tradeoff curves of a 6T SRAM bitcell at 65nm technology. If 2X leakage increment is allowed, bitcell size can be reduced by 7.69% $\sim$ 12.31%, depending on OPC aggressiveness.

Line-end shortening (LES) is the patterning imperfection when polysilicon does not completely cover active region as depicted in Figure 9. This can be caused by overlay errors or lithographic line-end pull back. The uncovered active region will form a conducting path and it is modeled as a resistor connecting source and drain terminals in [66]. A LES transistor (i.e., transistors suffering from line end shortening) and its equivalent circuit is illustrated in Figure 9. Experiment results in Figure 10 show that the maximum V_{gs} increment due to LES is 0.2V, which is too small to flip a

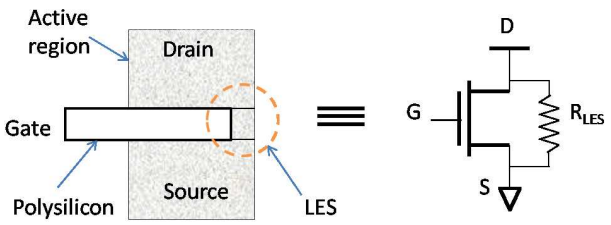

Figure 9. A transistor suffering LES and its equivalent circuit.

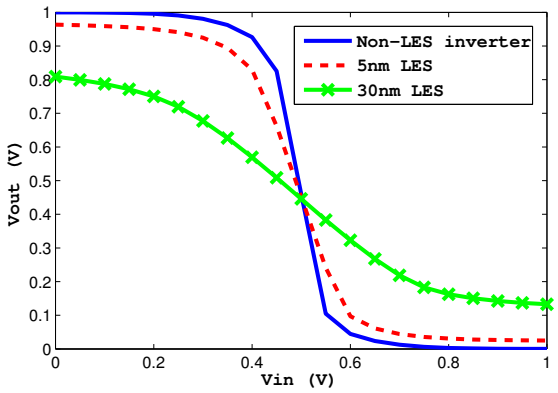

Figure 10. Voltage transfer curves for 45nm LES and nominal inverters.

CMOS logic. Therefore, LES transistors can function correctly within reasonable line-end shortening. However, LES transistor may lead to hold time failure as well as very high leakage [66].

III. Electrical Impact of DPL Imperfections

A. Overlay-induced variations

In DPL, overlay error between patterns of the same layer from different exposures translates into line-width/spacing variation[7] (depicted in Figure 11) with serious implications on devices and wires.

On the device side, the main consequence of overlay error in DPL is its impact on stress. Assuming a positive DPL process, which is preferred over a negative process for the reasons highlighted in [19][8], overlay-induced layout variations that affect stress include:

- gate spacing affecting mechanical stress from stress liner;

[7]Line-spacing variation in case of positive process, where mask-CD corresponds to printed lines on wafer, and line-width variation in case of negative process, where mask-CD corresponds to printed spaces on wafer.

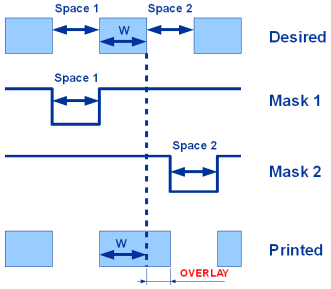

Figure 11. Example showing translation of overlay error into line-width variation in negative DPL process.

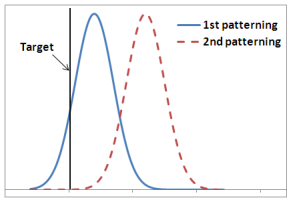

Figure 12. Bimodal distribution with different populations for first and second patterns.

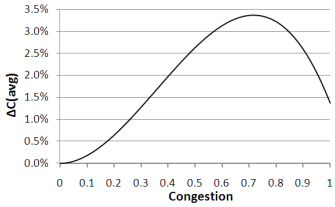

Figure 13. Average coupling capacitance variation in positive DPL process as a function of routing congestion.

- gate-to-contact spacing with impact on source/drain (S/D) resistance, gate-to-contact capacitance, and stress-liner stress;
- shallow trench isolation (STI) width, which impacts STI stress;
- S/D length influencing embedded SiGe and STI stress sources.

Stress has a significant effect on carrier mobility and V_{th} [20]–[22]. To illustrate the impact of overlay on device performance, consider 22nm process technology with 60nm minimum gate spacing and 5nm worst-case overlay. Using simulated data from [32] and extrapolating for 22nm technology, 5% I_{on} and 15mV V_{th} variation between two adjacent transistors can be observed.

Electrical impact of overlay error on wires fabricated with DPL has been studied extensively. A method for estimating delay variation due to overlay error is presented in [23]–[26]. A compact model to estimate interconnect delay variation due to overlay and focus variations in DPL is offered in [24]. A systematic method to compare the effects of overlay to that of CD variability on interconnect delay variation is proposed in [25]. In a previous work [26], we study the relative importance of different overlay sources and the interactions between overlay and design parameters. All these studies show tolerable overlay effects on coupling capacitance and wire delay variation with existing overlay budget, especially when considering congestion as Figure 13 shows (average ΔC is at most 3.4%).

B. Bimodality problem

CD and electrical parameters of transistors typically follow a normal distribution with some σ and μ, which deviates slightly from the target. Since DPL has two separate exposure and etch steps, two populations exist: one for transistors formed by the first exposure/etch step and another for transistors formed by the second exposure/etch step as depicted in Figure 12.

Furthermore, overlay error between gates of different exposure/etch steps, which induce stress and delay variation as discussed in the previous section, is another contributor to the bimodality problem.

An obvious consequence of bimodality is a larger within-die CD/delay variation. Dusa *et al.* [27] observe from CD measurements a 34% increase of 3σ CD variability in DPL compared to that of single patterning. Arnold *et al.* [19] propose the following model to describe 3σ of the pooled line CD distribution:

$$3\sigma^2_{pooled} = \frac{3\sigma^2_{p1}}{2} + \frac{3\sigma^2_{p2}}{2} + \left(\frac{3}{2}\left|\mu_{p1} - \mu_{p2}\right|\right)^2, \qquad (1)$$

where $p1$ and $p2$ correspond to lines (or lines) formed by the first and second patterning steps respectively.

Another serious consequence of the bimodality problem is the loss of spatial correlation. Effects of spatial correlation have been incorporated into statistical timing analysis [28,29] to reduce timing guardbands. Jeong and Kahng [30] examine timing problems that arise due to bimodality (53ps clock skew and 46ps additional timing slack assuming 6nm CD difference) and propose solutions to address them during timing analysis and optimization.

[8]Positive process is preferred over negative process because its larger dose-focus latitude, smaller MEEF and LER, and insensitive line-CD to overlay error.

IV. Conclusions

In sub-wavelength regime, lithography is a dominant source of layout-dependent variability; other sources, however, are also important. Layout-dependent stress variation has significant effects on circuit performance (15% Δ I_{on} from layout variation [31]). Ion scattering at well edge during implantation (well proximity effect) affects V_{th} [33]. Up to 10% delay increase in 65nm process reported in [35]. Etch process introduces CD variability with strong dependence on pattern-density within a few microns range [36,37]. Rapid thermal annealing (RTA) used in the fabrication of ultra-shallow junctions is another source of variation. RTA has a long-range dependence on pattern-density (few millimeters) [38,39] and has a significant effect on I_{on}/I_{off} ratio and V_{th}. Chemical mechanical polishing (CMP) introduces interconnect R and C variability due to dishing and erosion [40,41,76]. The amount of variability depends on line-width/spacing and pattern-density within a long-range (up to 100μm [41]).

In this paper, we did a brief overview of shape imperfections arising from lithographic patterning and electrical models thereof. Though, we did not discuss it here, a big hurdle in practical use of such models (especially when using simulated contours at perturbed lithographic process conditions) is their integration with semi-empirical device models (e.g., BSIM) at process corners. Lithographic variation (e.g., due to focus, exposure, overlay errors) is an important contributor to gate length/width variation and lithography simulation followed by non-rectangular gate modeling can remove a lot of pessimism inherent in the device models (e.g., see [49] for focus variation aware timing analysis). Unfortunately, this requires accurate partitioning and "blame assignment" of variation sources which are unavailable in most current processes (even test structure design and characterization methodologies to do this are largely an open question). Furthermore, most modern design flows limit lithography modeling to geometry (if at all), future adoption of electrical models will depend on advancements in RET or patterning (for example, interference assisted lithography [5] almost completely gets rid of line-end problems); extent of layout restrictions for manufacturability; and relative contribution of lithography to total dimensional and electrical variability.

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