Pattern-Restricted Design at 10nm and Beyond

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***Abstract*—Manufacturing has been incapable of keeping up with Moore's law without significantly increasing process variability and imposing massive geometric restrictions on design. This paper highlights the design impact of variability and geometric constraints – including traditional design rules and pattern-scale constraints – and describes our approach for evaluating and enforcing pattern-scale restrictions on design.**

I. Layout Restrictions, Variability, and their Design Impact

Small changes in layout constraints, a.k.a. design rules, can have a significant impact on design power, performance, and area metrics. Moreover, a rule change may affect different metrics in opposite directions. For example, increasing the spacing rule between n-type well and transistors active region will improve transistor performance – due to reduced well-proximity effect – but will increase layout area.

One method to examine the design impact of rules is the Design Rule Evaluator (DRE) [1]. The DRE methodology consist of quick estimation of the layout for a given set of rules followed by approximate modeling of design metrics. Layout estimation – rather than actual generation – allows the practical exploration of a wide range of rules; and, approximate models – rather than accurate models involving significant development effort (e.g., lithography/circuit simulation) – requires easy-to-extrapolate technology parameters and, hence, allows DRE use for design-technology co-optimization *at early stages of technology development*.

Manufacturing imperfections, whose magnitude depends strongly on design rules, lead to process-parameters variability [4]. Variations in process parameters translate into variation in transistors power consumption and delay with direct impact on the overall power, performance, or area of the design depending on the optimization objective. Figure 1 shows how variations in standard-cell delay translates into design area change when the objective is to meet a fixed performance target.

Chip-level DRE [3] predicts the impact of rules on delay and delay variability and models tradeoffs between performance and area that occur at the system level; it uses a static timing-analysis model to estimate cell delay and a neural network-based model to predict delay-margin dependent area penalty. Chip-level area is estimated from cell area – including the delay-margin area penalty – and a cell-area to chip-area model that is calibrated using actual synthesis, place and route data. Finally, design metrics of area, performance, variability and functional yield (and power in the future) are unified into a single design-quality metric of "good chips per wafer" (GCPW), which can be computed fast enough to allow system-level design/technology co-optimization (e.g., Figure 2).

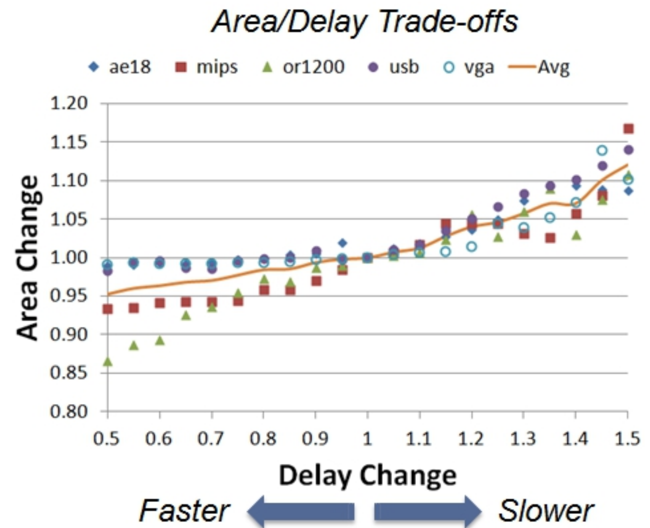

Figure 1. Design area versus standard-cell delay, where curves are generated using purely empirical synthesis/placement/routing experiments (reprinted from [2]).

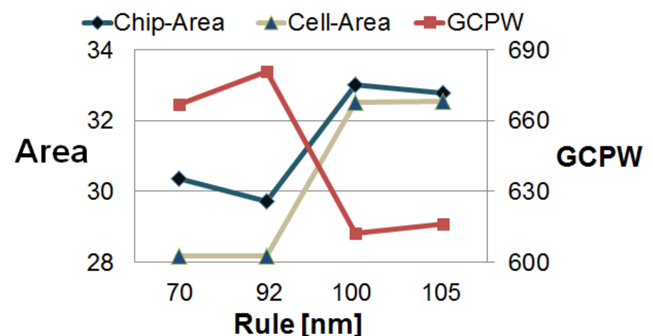

Figure 2. DRE-generated plots for chip area, overall cell area and GCPW metric for different values of n-type well-to-active spacing rule [3].

Manufacturing is becoming increasingly complex as we approach physical-scaling limits. The diameter of optical interference has been constant with scaling (and will continue to be at 10nm and possibly beyond) making features context – i.e. entire layout patterns – increasingly important. Earlier, simple dimensional constraints on layout configurations such as spacing/width design rules were enough to ensure

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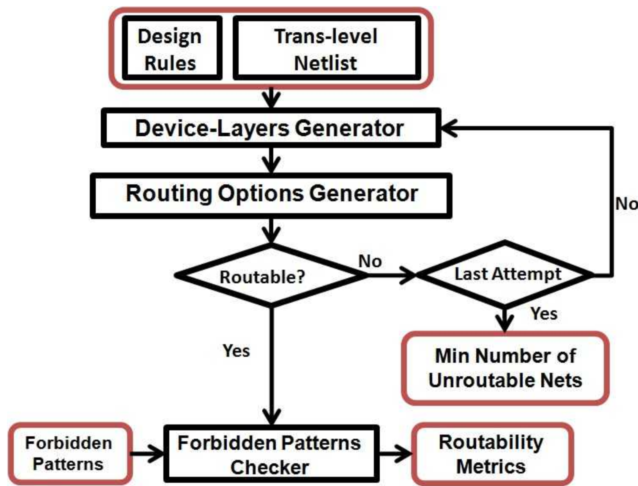

Figure 3. Flow of pattern-driven DRE.

manufacturability. In today's deep-submicron technology, constraints on layout configurations as well as their contexts (i.e. pattern-scale constraints) must be enforced to ensure manufacturability.

II. Pre-Layout Pattern Restrictions

Restricting design from comprising specific patterns can have a large impact on key design metrics including layout area. What patterns need to be prohibited depends on technological choices made when defining the process (e.g., patterning technology such as double-patterning technology). Therefore, making informed technological decisions requires methods for evaluating the cost of forbidding patterns. One such method is described in our previous works of [5,6], where the DRE methodology is extended to estimate the design impact of forbidden patterns.

The flow for pattern-driven DRE from [5] is shown in Figure 3. From a set of design rules and forbidden patterns, DRE generates a virtual standard-cell library, where metal layers are estimated using a wiring-approximation method [6]. For each cell, possible routing options are examined and only those excluding forbidden patterns are preserved. After transistors are placed, certain cells may be impossible to route. In such a situation, an alternative transistor placement solution is used and the routing is reattempted until a routing solution exists or the maximum number of attempts is reached. If the cell is unroutable after the maximum number of attempts is reached, an integer linear program is employed to determine the routing option with the minimum number of unroutable nets. The reported routability metrics include: the number of routable cells and the total number of feasible routing options. In addition, the counts of all occurring patterns are reported.

Pattern-driven DRE was used to compare litho-etch-litho-etch double patterning lithography (LELE) to extreme ultraviolet lithography (EUV). While pattern-scale constraints are needed for LELE – due to mask-assignment (a.k.a. coloring) conflicts, simple dimensional constraints suffice for EUV. To come up with a set of LELE forbidden patterns to use in our comparative experiment, $4{\times}4$ patterns are extracted from DRE-estimated standard-cell library layouts and a commercial LELE decomposer is then used to identify noncompliant patterns. The cost of forbidding those patterns is then evaluated using pattern-driven DRE: LELE leads to 6.4% less routable cells and 57.3% less routing options.

In another experiment, the routability impact of active-region placement is assessed for a Self-Aligned Double Patterning (SADP) process. Using SADP-forbidden patterns, two active-placement options are examined: (1) closest to the center of the cell at the P/N regions interface and (2) closest to the top/bottom edges of the cell. The results shows that placing active closest to the edge of the cell improves the number of routable cells by 5.1% and the routing options by 6.9%.

Simple design rules can be defined in such a way to avoid pattern/large-scale manufacturing constraint violations. A generic approach for modeling the impact of rules on large-scale violations combines DRE with machine-learning methods [6]. One example of such violations is LELE mask-assignment conflicts, whose occurrence strongly depends on spacing rules and can be correlated with certain layout aspects. Therefore, the work in [6] extracts aspects of DRE-estimated layouts such as wire congestion based upon which conflicts are predicted using a machine-learning model. High-fidelity conflict prediction with 81% accuracy is achieved and the probabilistic nature of DRE's layout estimation ensures the method is generic rather than specific to a routing approach or exact patterns.

III. Post-Layout Pattern Restrictions

Undesired manufacturing-frail patterns (a.k.a hotspots) that cannot be avoided through rules – either because layout-generation tools are not ready to handle complex rules or because avoiding them through rules leads to too large overhead – need to be eliminated before the design can be taped out. This can be achieved using pattern-based physical verification methods (e.g., DRC+ [7]). A set of hotspot patterns, verified through manufacturing simulation, is determined for the manufacturing process. Using this set of patterns, pattern matching is run on every design to identify hotspot locations. Pattern violations are then fixed by stripping out a wire and rerouting it. Hoping to converge to a legal-layout solution, the procedure is repeated iteratively.

Iterative fixing of pattern violations may converge with a handful of violations but, since pattern-scale restrictions increase with technology scaling, there will certainly be a tipping point when the number of violations becomes unmanageable.

Instead of creating the layout and then fixing it, *layout should be constructed using pre-certified patterns as building blocks*. Admittedly, forcing routers to use specific patterns is difficult and may significantly degrade solution quality. A more viable approach is to start with a layout solution from existing routers and carry out substitution with pre-certified patterns [8]. Starting with an initial pattern-oblivious layout

as guide, existing patterns are analyzed and then classified according to their connectivity and constraints with their surroundings. Performing the same "function", patterns of the same class are hence replaceable. Pattern qualification is then carried out to determine the "best" pattern in every class (e.g., best printability). By applying this process on multiple layouts, a library of best-in-class patterns and a library of imperfect patterns are constructed. Lastly, imperfect patterns are searched for in the layout, using geometric pattern-matching, and each instance is replaced with the corresponding best-in-class pattern.

Early results are promising, showing the method applicability with reasonable run-time. By analyzing only 1% of unique patterns in a relatively small 1×1mm layout, more than a hundred thousand pattern substitutions are possible. Another important result is that as much as 200 unique patterns can belong to the same class. Therefore, chances of finding high-quality best-in-class patterns are high and benefits of pattern substitution can be enormous. Additionally, because multiple unique patterns are substituted with a single pattern, the method maximizes pattern re-use making the layout more regular and facilitating silicon debug and source-mask optimization.

IV. CONCLUSION

This paper presented approaches to cope with layout design under severe pattern restrictions. First, the DRE methodology is used to optimize design rules (whether pattern-based or otherwise) such that occurrence of manufacturing-frail patterns is minimized, especially in standard cells. Second, a pattern substitution-based approach is proposed to remove residual poor patterns, especially in routing layers. Future patterning technologies at 10nm node and beyond will necessitate pattern avoidance as an integral part of the design to manufacturing flow.

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