Efficient Layout Generation and Evaluation of Vertical Channel Devices

Wei-Che Wang and Puneet Gupta
weichewang@ucla.edu, puneet@ee.ucla.edu
Department of Electrical Engineering, University of California, Los Angeles

***Abstract*—Vertical gate-all-around (VGAA) has been shown to be one of the most promising devices for the scaling beyond 10nm for its reduced delay, large driving current, and good gate control. Moreover, emerging devices such as heterojunction tunneling FETs are more amenable to vertical fabrication. However, past studies of vertical channel devices focused more on regular memory architectures and simple standard cells like inverter. Since naive migration of regular FinFET layouts to vertical FETs yields little benefits, we identify several vertical efficient layout structures and propose novel layout generation heuristics for vertical channel devices. We also compare VGAA with symmetric and asymmetric source/drain architectures. The layout efficiencies of several VGAA structures, vertical double gate (VDG), lateral gate-all-around (LGAA), and FinFET are presented in our experiments. We observe that even though most vertical channel standard cells have more diffusion gaps than lateral cells do, they still benefit from vertical architectures in area because of the elimination of diffusion contacts. For asymmetric architectures, the area is larger than symmetric architectures because of the extra diffusion gaps needed, but our experiments indicate that for both symmetric and asymmetric architectures, vertical channel devices are likely to have a density advantage over lateral channel devices assuming that current drive strengths of both are similar.**

I. Introduction

Performance and size scaling demands of modern IC chips have become the driving forces to the development of new devices [1]. Vertically fabricated transistors, such as vertical gate-all-around (VGAA) [2], vertical double-gate (VDG) [3], and vertical heterojunction tunneling FET (VHTFET) [4] are being considered to be the alternative structures in the future. The concept of vertical channel FETs was proposed for more than two decades ago [5], but it did not catch much attention due to the complex fabrication process at that time. FinFET [6], instead, has become a more practical solution for scaled semiconductor technologies [7]. However, as conventional scaling hits its barriers below the regime of 10nm, vertically fabricated transistors are reconsidered to be one of the replacements of FinFET devices [8]. Recent studies on vertical devices have demonstrated the improved fabrication process control and many appealing properties [9, 10]. Arrays of VGAA with 20nm diameter have been successfully fabricated, and good transistor characteristics such as large drive current, high I_{on}/I_{off} ratio, delay improvement [11], and better short channel effect control of VGAA have been observed [2], showing the potential opportunities provided by VGAA for the continued scaling of semiconductor devices.

Vertical heterojunction tunneling FET (VHTFET) is one of the vertical channel FETs with steep subthreshold swing and improved performance due to the decreased source-to-channel tunnel barrier height [4]. Because of the multi-junction nature, heterojunction tunneling FETs are more amenable to be fabricated vertically. The structure of VHTFET is similar to VGAA except that the source/drain terminal of VGAA is interchangeable while VHTFET has a fixed source/drain structure [12]. Vertical slit FET (VESFET) is another emerging 3D device with four vertical pillars forming a device [13]. However, VESFET is not a vertical channel FET because the current flow is parallel to the wafer plane. It is similar to planar CMOS because source and drain are on the two sides of gate control, and the layouts of standard cells can be obtained automatically using Euler path-based algorithm [14]. For vertical channel FETs, a direct migration from planar to vertical layout generation will yield little benefits. Therefore, new layout design style and strategies are introduced in this paper to optimize transistor density for vertical channel FETs.

A. Introduction to Vertical FETs

Many vertical structures have been studied and discussed [11, 12, 15]. Unlike planar transistors, the current flow of vertical channel FETs is perpendicular to the wafer plane, which brings new challenges to efficient layout generation.

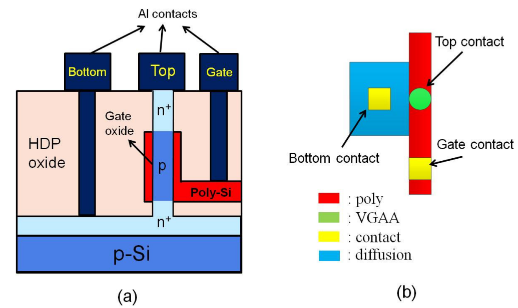

Fig. 1. VGAA device: (a)Cross section view of VGAA. (b)2D layout view.

Figure 1 shows the cross section and 2D layout view of a VGAA transistor. Two ends of the vertical pillar are doped, and the middle of the pillar is surrounded by polysilicon gate. Contacts are connected to the top, bottom, and gate of the vertical pillar. Note that the gate extension can be aligned with the bottom and top contact plane [11] as shown in Figure 1 (a), or be perpendicular to the bottom and top contact plane [12] as shown in the 2D layout in Figure 1 (b). The efficient layout generation proposed in this paper is applicable to both vertical structures. However, we focus on the structure presented in Figure 1 (b) because its layout resembles LGAA and FinFET more than the layout of Figure 1 (a) does. The top contact serves as either a source or a drain terminal, and so does the bottom contact. Interestingly, even though the source and drain terminals are interchangeable, the device behavior differs significantly between the two architectures. When the top tip of vertical pillar serves as the source, the I_{on} is about 30% larger than the case where substrate side serves as the source, which could be due to low doping on the bottom side caused by the shadowing effect [2]. However, the results in [16] show that a two-stage inverter delay is nearly 50% higher when top tip of vertical pillar serves as the source because of the increased series resistance and load capacitance. Therefore, the electrode asymmetry and parasitics are important considerations for circuit design using VGAA. In our experiments, symmetric and asymmetric VGAA structures are compared (albeit only from a layout efficiency perspective), where symmetric means that source and drain

are interchangeable, and asymmetric means that the top contact can only be served as source.

Besides the attractive characteristics of VGAA, another aspect that has impact on device performance is the crystalline orientation. Similar to FinFET, the channel of VGAA stands vertically on the wafer and can easily lie outside of the base crystallographic plane. In fact, on a (100) wafer, the surface orientation of VGAA is a mix of (110) and (100) because of the cylindrical channel shape. From the previous work on surface orientation optimization of FinFET [17], the surface orientation with the highest hole mobility and electron mobility is (110) and (100), respectively. Furthermore, since the PMOS enhancement on (110) is larger than the NMOS degradation due to velocity saturation, the overall delay can be improved by moving away from a standard (100) surface due to the enhancement of hole mobility.

The effective device performance of vertical structures compared to lateral structures is complex and beyond the scope of this work. Interested readers may refer to [11, 18] for some early studies. In this paper, we neglect the overall possible benefits of vertical channel devices by comparing the area using same effective width with lateral channel devices. Our focus is primarily to study layout efficiencies of vertical channel devices.

The VGAA fabrication process flow on 8-in bulk Si wafer has been studied and demonstrated. Figure 2 explains a common process flow [9, 10].

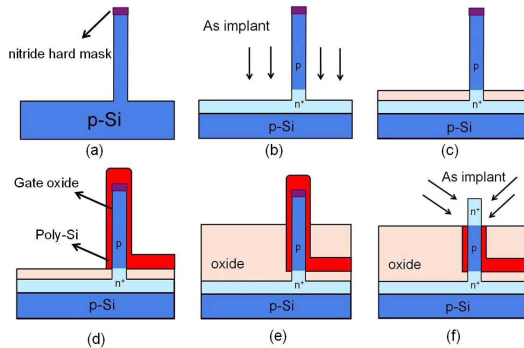

Fig. 2. Fabrication process flow of VGAA: (a)Space nitride hard mask patterning and pillar etching. (b)As implant. (c)Oxide deposition. (d)Gate oxide growth and polysilicon gate deposition. (e)Another oxide deposition. (f)Isotropic etch and pillar top implantation.

B. *Related Work*

Lot of research of VGAA application in memory devices has been done in the past because of the potential shrinking ability on both individual devices and multilevel memory structures [15, 19]. Studies on basic standard cells like inverter have also been done [11]. However, since standard cells use a large variety of layout structures, it would be difficult to evaluate the layout efficiency of a complete vertical channel standard cell library without using a systematic framework. For planar CMOS, lateral gate-all-around (LGAA) [20], and FinFET, the layout generation methodologies have been studied [21], and frameworks for an early stage design rule evaluation were also propose [22, 23]. However, these algorithms cannot be applied to VGAA given that the structure of VGAA is radically different from planar or lateral FETs. Previous study showing evident area reduction of a vertical channel inverter cell is given in [12]. The area reduction comes from the elimination of diffusion contacts between the adjacent polysilicon shapes. Replacing these diffusion contacts by top contacts as illustrated in Figure 1 (b) helps reduce area significantly.

In our experiments, we extended the concept of contact space saving and performed a fair comparison on a full standard cell library. In this paper, we propose a systematic framework that generates efficient VGAA standard cell layouts and evaluates the impact of design rules as an early technology assessment of the emerging future vertical devices.

C. *Our Contributions*

Key contributions of this work are summarized as follows:

- We develop the first systematic framework for effective layout generation for vertical channel devices.
- Layout efficiencies of several variations of VGAA, VDG, LGAA and FinFET are compared, including area and intracell wirelength. Impact of design rules on design benchmarks are also evaluated systematically.

The rest of the paper is organized as follows. In Section II, variations of VGAA devices, efficient/inefficient vertical structures, and wirelength optimizations are introduced. The cell bipartite graph representation and minimum chaining algorithm will be demonstrated in Section III. Section IV presents the design rules evaluation and experimental results on the proposed method. Finally a conclusion is drawn in Section V.

II. VGAA Layout Structures

A. *Variations of VGAA Structures*

We evaluated three kinds of VGAA structures to have a comprehensive understanding of the area impact of different VGAA cell architectures and patterning technology restrictions. The three architectures of VGAA are given below:

- *Fixed-Pitch VGAA (FVGAA):* FVGAA has regular rectangular polysilicon gate shape with fixed polysilicon pitch. The polysilicon spacing is defined as the sum of contact width and two times of contact-poly spacing. The effective transistor width is the perimeter of the VGAA. Figure 3 (a) shows an example of FVGAA 2D layout of an inverter with the bottom contact serves as source and top contacts are drain terminals. The driving strength of the PMOS is equal to four VGAA pillars and two VGAA pillars for NMOS width.
- *Contact Spacing Reduction Fixed-Pitch VGAA (RVGAA):* The polysilicon pitch of RVGAA could be one or two times of the minimum polysilicon spacing plus a polysilicon gate width, depending on whether or not a bottom contact is formed. Detail design rules are given in section IV. As shown in the Figure 3 (b), X is the minimum polysilicon spacing and Y is the polysilicon gate width. Every polysilicon is still located on grid, but the spacing becomes less than half if no bottom contact is placed between two polysilicon gate shapes. Therefore, RVGAA devices have less area than FVGAA for large drive cells with multiple polysilicon gate shapes.
- *Polygon-Poly VGAA (PVGAA):* The architecture of PVGAA is given in Figure 3 (c). The shape of the polysilicon depends on the number of VGAA needed to form the cell. Array of vertical pillars are surrounded by a huge polygon polysilicon gate shape, so the area becomes much smaller than FVGAA and RVGAA because contact spacing is smaller than polysilicon spacing. Similar VGAA array fabrication was demonstrated in [2], however, lithography patterning of the surrounding irregular polysilicon gate shape is yet another challenging task. We include PVGAA with spacing rules same as FVGAA in our comparison to give an idea of how much benefits it could have compared with FVGAA.

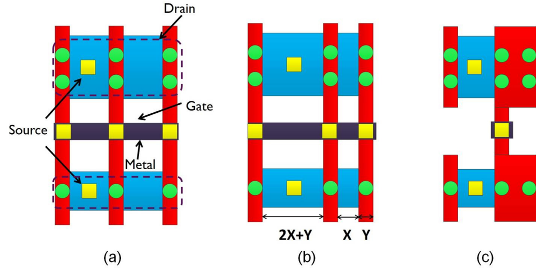

Fig. 3. VGAA structures: (a)FVGAA. (b)RVGAA. X is the minimum polysilicon spacing and Y is the polysilicon gate width. (c) PVGAA.

B. Vertical Efficient Structures

In this section, we will introduce vertical efficient structures that provide efficient layouts given the restriction of vertical channel structure, and our VGAA default structure is FVGAA. For CMOS layouts, sharing the same active/diffusion region (what we refer to as a chain in this paper) between different transistors results in fewer diffusion breaks and smaller area. The definition of chain is the same as in [22], which means pairs of P-N transistors that share a same diffusion strip. For instance in conventional lateral channel devices, two parallel connected transistors and any number of series connected transistors can share the same diffusion region or chain. Less number of chains means smaller area. Since the structure of VGAA is radically different from lateral FETs, some CMOS circuit schematics that are considered efficient in lateral FET may not be the most efficient schematics for VGAA. Figure 4 shows an example of how a 3-Parallel structure is implemented in FinFET and VGAA on a single chain. VGAA has smaller area because of the elimination of the diffusion contacts.

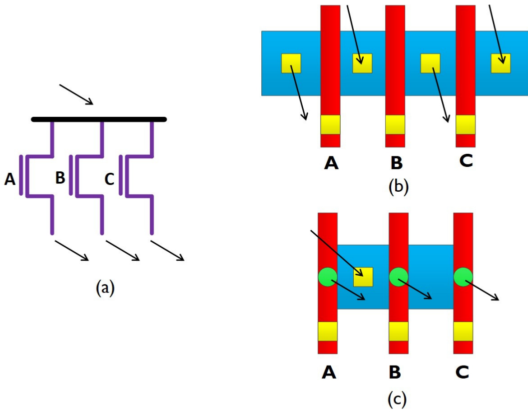

Fig. 4. 3-Parallel structure: (a)Transistor schematic. (b)FinFET. (c)VGAA.

In order to find out the best structure of VGAA layout, we categorize two types of vertical efficient layout structures.

- *n-Parallel:* The n-Parallel structure is composed of n VGAA devices with a connected source or drain terminals. The cross section view and schematic of a 3-Parallel structure is given in Figure 5. Three VGAA devices are shared on a same diffusion strip, where the shared terminal can be either a source or a drain. Three gate contacts are placed perpendicular to the bottom and top contact plane as shown in the 2D layout Figure 1 (b).
- *2-Stack n-m-Parallel:* A 2-Stack n-m-Parallel structure consists of two stacked n-Parallel structures, where the number n and m can be equal to or greater than one. Figure 6 illustrates the cross section view of a 2-Stack 3-3-Parallel structure. Note that for asymmetric structures, this is not a valid vertical structure because source and drain are not interchangeable.

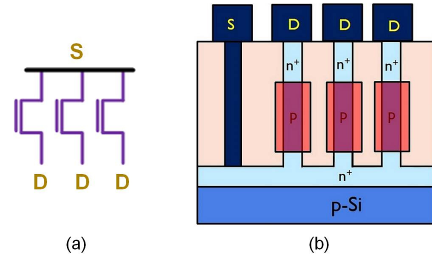

Fig. 5. n-Parallel structure: (a)Transistor schematic. (b)VGAA cross section view

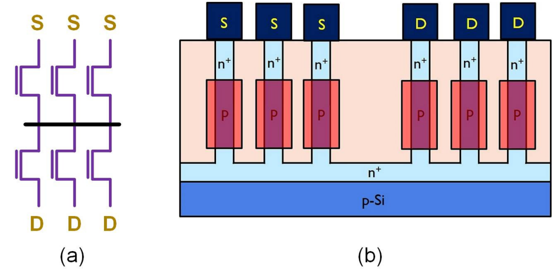

Fig. 6. 2-Stack n-m-Parallel Structure: (a)Transistor schematic. (b)VGAA cross section view

Any circuit schematic of these two forms can be realized using only one vertical channel chain, which are preferred structures in minimizing the layout area. These schematic patterns for efficient layout will be identified in a systematic way and become the input to the proposed minimum chaining algorithm for vertical channel devices.

C. Vertical Inefficient Structures

In contrast to vertical efficient structures, here are two examples of vertical inefficient structures that can be realized by lateral FETs on one chain but will require multiple chains in vertical FETs.

- *3-Stack:* A 3-Stack schematic is given in Figure 7 (a). In VGAA, the minimum number of chains to realize this structure is two. The reason is that to form a 2-stack structure in VGAA, the bottom diffusion must be shared by the stacked transistors. To cut off the shared diffusion, instead of by a polysilicon gate control like FinFET, the only way for VGAA is to introduce another chain, which explains why a 3-Stack structure cannot be implemented in VGAA with only one chain. Figure 8 shows an example of how a 3-Stack structure can be implemented in FinFET on one chain, while in VGAA the minimum number of chains is two.
- *Stack-Parallel:* A Stack-Parallel structure is similar to n-Parallel, but at least one of the paralleled structures is a stack of transistors. Figure 7 (b) gives an example of a Stack- Parallel structure. Unfortunately, this structure appears in many standard cells, making most of the vertical channel structures having more chains than lateral channel structures.

D. Intracell Wirelength Optimization

Another layout benefit of vertical channel is that for an n-Parallel chain, the bottom contact can be placed on multiple locations of the

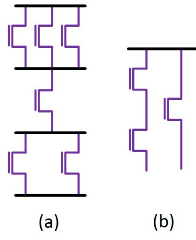

Fig. 7. Vertical inefficient structures: (a)3-Stack. The number of paralleled transistors on each stage is arbitrary. (b)Stack-Parallel.

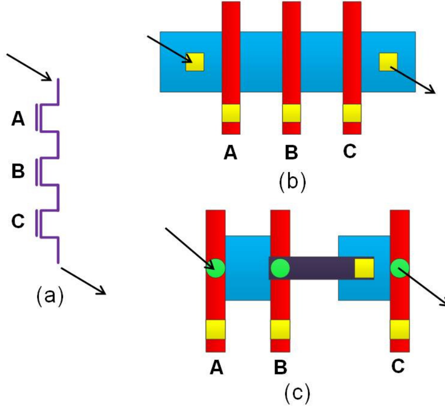

Fig. 8. 3-Stack structure: (a)Transistor schematic. (b)FinFET. Only one chain needed. (c)VGAA. Two chains needed.

diffusion strip because all parallel transistors share diffusion region. This flexibility helps to reduce the intracell wirelength of vertical channel FETs. Figure 9 shows an example of how a wirelength can be reduced by moving the bottom contact closer to each other, where the initial locations are on either the rightmost or the leftmost of the chain. A chain has at most one P/N bottom contact, and each bottom contact belongs to only one net. The total wirelength estimation is obtained by summing the half parameter wirelength (HPWL) of each net. Note that wirelength of VDD/GND is not counted in HPWL. Steps of minimizing HPWL are described below:

1) For each net, identify its leftmost and rightmost ends. If the two ends are on the same location horizontally, the HPWL cannot be reduced. Otherwise, proceed to step 2.
2) If any of the two ends is a bottom contact, move the leftmost bottom contact to right, and move the rightmost bottom contact to left.

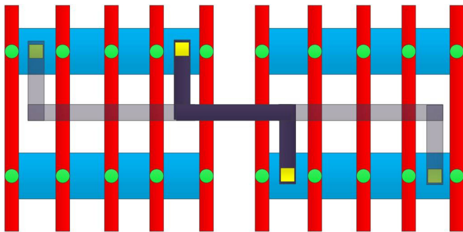

Fig. 9. Net HPWL reduced by moving bottom contacts

III. Vertical Channel Layout Generation Methodology

The proposed vertical channel layout generation methodology is divided into two steps. The first step is the development of the bipartite graph, from which the vertical efficient layout structure can be easily identified. The second step is to find the minimum number of chains by finding the minimum set of edges that cover all transistors in the bipartite graph.

A. Bipartite Graph Representation

We first define the graph notation in a similar fashion as [21]. The triple (T, D, S) represents the three attributes of a transistor t, where $T(t)$(= P or N) indicates whether t is a PMOS or NMOS, $D(t)$ and $S(t)$ represent the connecting net of the drain and the source terminal respectively. A P-N transistor pair $P(t_i, t_j)$, contains two transistors where $T(t_i) = P$ and $T(t_j) = N$. In this paper, we consider perfect pair implementation only [22], so a pair $P(t_i, t_j)$ means that t_i and t_j have the same gate input signal. To identify the vertical efficient layout structures, we represent the transistor schematic using a bipartite graph $G = (V_p \cup V_n, E)$. Each vertex in V_p or V_n corresponds to a set of PMOS or NMOS transistors that form one of the two vertical efficient layout structures. Once vertices are constructed, an edge is built between two vertices if the two vertices contain at least one P-N transistor pair. That is, each edge *covers* all the common transistor pairs between a V_p and V_n. This is different from the previous work [21] because for vertical channel devices, more than two transistors in a vertex can be formed on a chain, and each edge corresponds to a chain. Once the bipartite graph is built, we apply the proposed minimum edge covering algorithm to find out the chaining solution to the cell implementation. The formal description of E, V_p, and V_n are given:

$$E = \{E_{ij} : t_1, t_2, ..., t_k | \{t_1, t_2, ..., t_k\} = V_p i \cap V_n j\}$$
$$V_p = \{V_p i | V_p i = \{t_p | T(t_p) = P \cap (D(t_p) = i \cup S(t_p) = i)\}\}$$
$$V_n = \{V_n j | V_n j = \{t_n | T(t_n) = N \cap (D(t_n) = j \cup S(t_n) = j)\}\}$$

The description of the bipartite graph given is for symmetric structures. The representation for asymmetric structures can be easily obtained by first splitting each vertex representing a 2-Stack n-m-Parallel into two n-Parallel vertices, and then building the edges in the same fashion. It is obvious that asymmetric structure is very likely to have more chains than symmetric structures because one of the two vertical efficient structures does not exist anymore. In our benchmark experiments, both symmetric and asymmetric VGAA structures are compared.

Figure 10 gives an example of the bipartite graph representation and schematic of a symmetric VGAA AOI21 standard cell. In the bipartite graph, the node $V_p 1$, for example, contains three PMOS transistors that either their sources or drains are on net $V_p 1$ as illustrated in the schematic. $V_p 1$ itself represents a 2-Stack 1-2-Parallel vertical efficient structure, meaning that PMOS transistors A, B1, and B2 can be realized on a single chain. However, we need to consider the pairing with NMOS transistors by selecting edges in the graph. Edge E_{11} connects $V_p 1$ and $V_n 1$ and represents transistor pairs B1 and B2, so selecting edge E_{11} means that a chain is needed to realize pairs B1 and B2.

B. Minimum Edge Covering Algorithm

The goal of the algorithm is to select all P-N transistor pairs with the minimum number of edges. In the bipartite graph, each edge represents a set of P-N transistor pairs that can be realized on a chain, so a minimum edge covering algorithm is proposed to minimize the number of chains needed to implement a cell. The notation $E(P(t_i, t_j))$ is defined as the set of edges that cover the P-N transistor pair $P(t_i, t_j)$. A P-N transistor pair $P(t_i, t_j)$ is *covered* if at least one edge belonging to $E(P(t_i, t_j))$ is selected.

The algorithm is described as follows:

- For a bipartite graph, we generate a connection table for all edges and pairs. Each edge is represented by a column, and

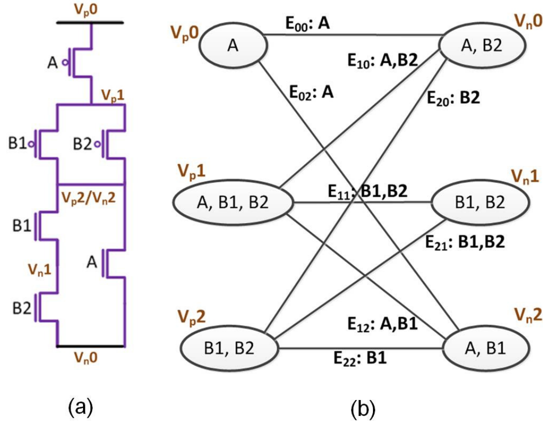

Fig. 10. AOI21 schematic and bipartite graph representation: (a)Schematic. (b)Bipartite representation.

TABLE I
CONNECTION TABLE OF AOI21

	E00	E02	E10	E11	E12	E20	E21	E22
A	1	1	1	0	1	0	0	0
B1	0	0	0	1	1	0	1	1
B2	0	0	1	1	0	1	1	0

each pair $P(t_i, t_j)$ is represented by a row. If an edge covers a pair, the value of the corresponding location is set to one, otherwise it is set to zero. The $E(P(t_i, t_j))$ of each pair is obtained after the connection table construction by finding the edges corresponding to ones in the row of $P(t_i, t_j)$.

- Identify *essential edges* by observing the connection table. If a row contains only a single 1, the corresponding edge of the column is an essential edge. Every essential edge is selected and removed from the connection table, along with all transistor pairs corresponding to the edge.
- For the remaining connection table, apply Petrickś method [24] by formulating the edges as Boolean variables and P-N transistor pairs as minterms. To cover a minterm $P(t_i, t_j)$, the sum of variables in $E(P(t_i, t_j))$ must be true. The logical function $F(G)$ is defined as the product of all minterms, and it must be true because all minterms must be covered.
- $F(G)$ is further simplified by using simple Boolean simplification technique $X + XY = X$. The product term with the least number of edges along with essential edges are returned by the algorithm as the minimum set of edges to cover all P-N transistor pairs.

Following the above procedure, the chaining solution of a vertical channel cell is then obtained. Table I gives an example of the connection table of AOI21. From the table we know that to cover P-N transistor pair of A, for example, the expression $(E_{00}+E_{02}+E_{10}+E_{12})$ must be true.

Since there are no essential edges for the AOI21 cell, we directly apply Petrickś method to form the Boolean functions given below:

$$A = E_{00} + E_{02} + E_{10} + E_{12}$$
$$B1 = E_{11} + E_{12} + E_{21} + E_{22}$$
$$B2 = E_{10} + E_{11} + E_{20} + E_{21}$$
$$F(G) = A \cdot B1 \cdot B2$$

$F(G)$ must be true to cover all the transistor pairs A, $B1$, and $B2$. After Boolean expansion and simplification of $F(G)$, there are eleven product terms with only two edges, which is the minimum set of edges needed. To make $F(G)$ true, one of these product terms is selected and set to be true, for example, $E_{00}E_{11}$. Now we know that the vertical channel cell AOI21 needs two chains to be realized, and the transistor pair on the first chain E_{00} is A, and the transistor pairs on the second chain E_{11} are $B1$ and $B2$. The final chaining result of AOI21 is shown in Figure 11.

The PMOS (upper) part of E_{11} is a 2-Parallel structure, so a bottom contact is placed as shown in Figure 4 (c), while no bottom contact is placed in the NMOS (lower part) because it is a 2-Stack 1-1-Parallel structure similar to the stacked transistors A and B shown in Figure 8 (c). Note that for asymmetric architecture, chain E_{11} will have to be split because the 2-Stack 1-1-Parallel structure of the NMOS is not valid.

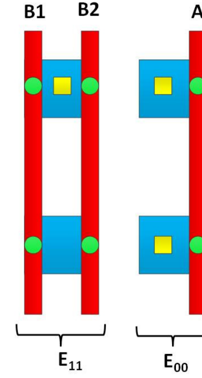

Fig. 11. AOI21 chaining result. Two chains E_{11} and E_{00} are needed.

IV. EXPERIMENTAL RESULTS

The proposed algorithm is implemented in C++ with the use of OpenAccess (OA) API [25] for GDSII file generation. We have worked with scaled version of publicly available standard cell library [26] and design rules as given in Figure 12. For RVGAA, PS_R is the polysilicon spacing when no bottom contact is placed, and PS_R2 is the polysilicon spacing when a bottom contact is placed. Note that the results of the comparison will strongly depend on the design rules chosen. The framework itself is, of course, applicable if different design rules are used.

Design Rules	nm
CW	13
DW	130
VS	15
VW	10
PW	10
PS	33
PS_R	20
PS_R2	50
FS	12
FW	4
Fin_Height	10
LGAA_D	10
LGAA_S	10

Fig. 12. Design Rules. PS_R and PS_R2 are for RVGAA polysilicon spacings.

TABLE II
PERCENTAGES OF CHANGE IN AREA IN COMPARISON TO FINFET

Cell	LGAA	FVGAA	RVGAA	PVGAA	VDG
INV_X1	0.0%	-50.0%	-30.2%	-50.0%	-50.0%
INV_X2	0.0%	-50.0%	-30.2%	-50.0%	-50.0%
INV_X4	0.0%	-50.0%	-30.2%	-50.0%	-50.0%
INV_X8	0.0%	-66.7%	-53.5%	-66.7%	-66.7%
INV_X16	-20.0%	-40.0%	-44.2%	-54.4%	-60.0%
INV_X32	-12.5%	-12.5%	-30.2%	-42.4%	-50.0%
NAND2_X1	0.0%	-66.7%	-53.5%	-66.7%	-66.7%
NAND2_X2	0.0%	-66.7%	-53.5%	-66.7%	-66.7%
NAND2_X4	0.0%	-66.7%	-53.5%	-66.7%	-66.7%
NAND2_X8	0.0%	-40.0%	-44.2%	-52.1%	-40.0%
DFF_X1	0.0%	-51.9%	-61.2%	-51.9%	-51.9%

A. Cell Area and HPWL Comparison

Table II shows the cell area comparison between LGAA, the three VGAA symmetric structures, and VDG on simple cells with different driving strengths and a complex flip-flop. The values shown are the percentages of change in cell area in comparison to FinFET.[1] For the layouts of LGAA and FinFETs, the generation is based on the framework presented in [22]. Positive percentages indicate that the device is larger than FinFET and negatives mean that the device is smaller than FinFET.

For LGAA, the area is smaller than FinFET for some cells because they are both lateral channels and LGAA has a larger effective transistor width per polysilicon than FinFET. For FinFET, the effective width of each fin is $FW + Fin_Height \times 2 = 24$, while the effective width of each LGAA is $LGAA_D \times \pi \approx 31.4$. For FinFET, each polysilicon can hold up to eight fins and the number of LGAAs that can be held per polysilicon is seven, so the effective transistor width per polysilicon for FinFET is $8 \times 24 = 192$, and for LGAA it is $7 \times 31.4 \approx 220$. Larger effective transistor width per polysilicon means less cell width and cell area.

For FVGAA, the area benefit of large driving strength inverters and NAND gates is not as significant as smaller driving cells because the number of VGAAs that can be held per polysilicon is only five according to the design rules. For small driving cells, both lateral and vertical cells need only one active polysilicon pitch, thus the contribution of removing diffusion contact becomes evident [12]. For flip-flops, the number of polysilicon gates is much larger than an inverter or a NAND gate because of its complex cell structure, but the area of the flip-flop is still much smaller than FinFET for all vertical devices. The reason is that many transistors connected to VDD and GND in flip-flops form a huge n-Parallel structure, which is a vertical efficient structure. FinFET needs more chains than VGAA to form the structure as given in Figure 4.

Compared to FVGAA, RVGAA shows more area reduction on cells with multiple shared polysilicon gates because the small PS_R when no bottom contact is placed. PVGAA also shows higher layout efficiency than FVGAA in large driving cells because VS is smaller than PS, and large driving cells require multiple polysilicon shapes. VDG shows high area efficiency because of the larger effective width per polysilicon than FinFET in addition to the diffusion contact removal.[2]

B. Comparison of Symmetric and Asymmetric Architectures

The results of area and intracell HPWL comparison on both symmetric and asymmetric FVGAA to FinFET are given in Table III.

[1]More area efficient isolation techniques for FinFET (e.g., [27]) may improve FinFET results over what is presented here.

[2]VGAA pillar diameter and pitch rules can alter this conclusion. In our current experiment, we assume pillar design rules to be same as contact rules.

TABLE III
SYMMETRIC/ASYMMETRIC FVGAA COMPARISON TO FINFET

Cell	Symmetric		Asymmetric	
	Area	HPWL	Area	HPWL
BUFFER_X1	-66.7%	-33.3%	-66.7%	-33.3%
MUX2_X1	-33.3%	-7.9%	-11.1%	26.1%
AOI21_X1	-25.0%	33.2%	25.0%	166.7%
DFF_X1	-51.9%	-47.4%	-51.9%	-47.4%
SDF_X1	-52.6%	-56.3%	-52.6%	-56.3%

TABLE IV
SYNTHESIS RESULTS OF FOUR BENCHMARKS

Benchmark	Sequential		Combinational	
	Instances	Area %	Instances	Area %
MIPS	1947	59.1	6283	40.9
FPU	656	13.9	15402	86.1
USB	1726	55.4	5291	44.6
AES	530	20.5	9871	79.5

For asymmetric structure, the area and HPWL are both worse than symmetric structure because for asymmetric structures, each chain realizing a 2-Stack n-m-Parallel must be split, which increases the number of chains.

The differences of symmetric and asymmetric architectures are also evaluated on four design benchmarks [28]. The numbers of synthesized sequential and combinational instances and area percentages of these benchmarks using a complete Nangate OpenCell library are given in Table IV.

Figure 13 gives the total design area ratio (in percentage) of FVGAA to LGAA. For all the benchmarks, the area of asymmetric architecture is much larger than symmetric architecture as expected. For RVGAA and PVGAA, the results are not shown here because the fabrication processes may still be too complicated to be practical for now. But one can expect that the area for these two structures should be smaller than FVGAA.

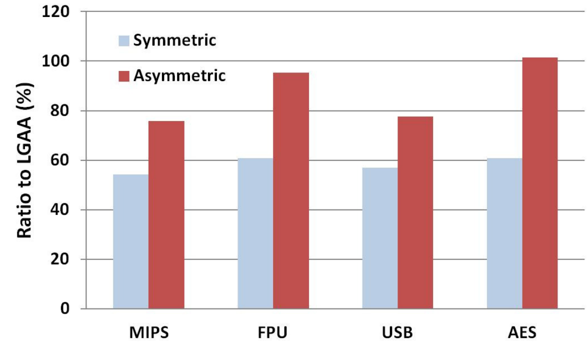

Fig. 13. Benchmark results of symmetric/asymmetric FVGAA to LGAA

C. Impact of Design Rules

Figure 14 shows the total design benchmark area ratio (in percentage) of symmetric FVGAA to LGAA where the design rule VS is evaluated at $5nm$, $15nm$, and $25nm$. As VS increases, the effective width per polysilicon reduces because the number of VGAA devices that can be held in a polysilicon reduces, thus the area increases.

All four benchmarks show that FVGAA has smaller area than LGAA. MIPS has the smallest area ratio because almost 60% of its total area is occupied by sequential cells as given in Table III. Other benchmarks have higher ratio (larger area) than MIPS because the vertical inefficient structures, as described in Section

II, are very common in many frequently used combinational cells. For example, the NMOS part of a simple AND2 cell forms a Stack-Parallel structure, and the PMOS part of an OR3 cell forms a 3-Stack structure. However, the area benefit of replacing diffusion contacts by top contacts is still the dominant factor that contributes to the area reduction in vertical channel structures.

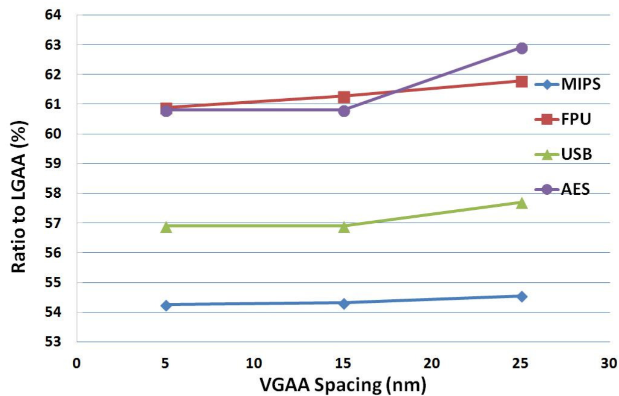

Fig. 14. Benchmark results of symmetric FVGAA to LGAA

V. Conclusion

In this paper, we develop the first framework and heuristics for efficient layout generation for standard cells using vertical channel devices (available for download at http://nanocad.ee.ucla.edu/Main/DownloadForm). Several vertical efficient and inefficient layout structures are identified to explain the difference in layout generation strategies between vertical and lateral devices. Symmetric and asymmetric vertical channel architectures are also discussed and compared. The layout efficiencies of several VGAA structures, VDG, LGAA, and FinFET are compared in our experiments. Our results show that standard cells and designs implemented by vertical channel devices are likely to have smaller area. Even though several simple standard cells are composed of vertical inefficient structures, vertical structures provide the ability of placing a top contact aligned with a vertical channel and thus still reduce the area significantly. Our future work will study in further detail the impact of design rules and alternative layout structures on VGAA layouts.

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