Comprehensive Defect Avoidance Framework for Mitigating EUV Mask Defects

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ABSTRACT

Defect avoidance methods are likely to play a key role in overcoming the challenge of mask blank defects in EUV lithography. In this work, we propose a novel EUV mask defect avoidance method. It is the first approach that allows exploring all the degrees of freedom available for defect avoidance (pattern shift, rotation and mask floorplanning). We model the defect avoidance problem as a global, non-convex optimization problem and then solve it using a combination of random walk and gradient descent. For a $8nm$ polysilicon layer of an ARM Cortex M0 layout, our method achieves 60% point better mask yield compared to prior art in defect avoidance for a 40-defect mask.

1. INTRODUCTION

Extreme ultraviolet (EUV) lithography remains the most promising next generation lithography solution to replace the current deep ultraviolet (DUV) lithography [3]. In addition to source power, mask blank defectivity is one of the key challenges facing this technology [19]. Even tiny mask blank defects can significantly alter the pattern printed on the wafer. For example, even a $3.5nm$ tall defect can cause a massive critical dimension (CD) change of $20nm$ on the wafer [7]. Moreover, these defects are hard to repair without damaging the mask itself [8].

Due to the defective and hard-to-repair nature of EUV mask blanks, the ability to tolerate some of these defects without any impact on yield is a very attractive proposition. Defect avoidance based techniques have emerged as a very effective means to tolerate mask defects. These techniques rely on inspection of mask blanks to first determine defect locations. The position of the design pattern, which needs to be written on the mask, can then be shifted relative to the mask to avoid the defects. There are essentially three degrees of freedom that can be exploited to avoid mask blank defects:

- Pattern Shift: Shifting the entire mask field pattern. Several prior approaches have looked at methods to exploit pattern shift to avoid defects [6, 22–24].
- Rotation: This involves rotating the entire mask pattern about the center of the mask. Zhang et. al. [25] proposed a method of doing small-angle rotation together with pattern shift.
- Mask Floorplanning: Move each die copy inside the mask field independently. This method can lead to gaps between die copies (scribe area), which is area wasted on the wafer. Moreover, different layers of the same design must be moved simultaneously. [11, 16] proposed methods to perform floorplanning together with pattern shift.

We have summarized the different degrees of freedom for defect avoidance in Figure 1.

Elayat et. al. [12] and Jeong et. al. [14] provided a cost-benefit assesment of different defect avoidance and reticle planning strategies, respectively. The low accuracy of mask blank inspection tools is a serious limitation for defect avoidance based mitigation. But some recent techniques have also looked at methods that can tolerate defect position inaccuracy as well [10,16]. Alternate approaches to mask defect mitigation that rely on correcting the absorber pattern after mask write have also been proposed [7, 21], but they may be less effective than defect avoidance techniques [15], especially for large defects or high defect density.

In this work, we present a global optimization based defect avoidance method to avoid EUV mask defects. To the best of our knowledge, this is the first work on EUV mask defect mitigation that allows simultaneous optimization of all the three degrees of freedom offered by defect avoidance: pattern shift, rotation and floorplanning. We formulate the problem as a non-convex optimization problem and then solve it using a combination

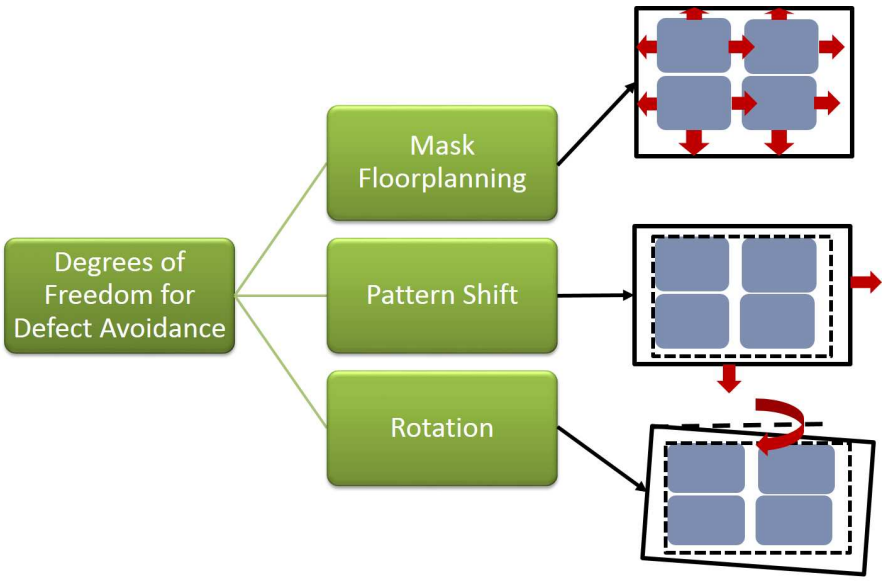

Figure 1. Summary of three degrees of freedom for avoiding EUV mask defects.

of hit-and-run based random walk and gradient descent. Some other key features of our methodology are as follows:

- Multi-layer: When multiple layers of a single design need to be patterned with EUV, the entire mask pattern corresponding to each layer can be shifted independently. The various die copies, however, must have the same relative location to ensure alignment. The floorplanning method of [16] accounts for this by using a two-step optimization strategy, where pattern shift of each layer is done first, followed by simultaneous floorplanning. This heuristic might miss several feasible solutions. Our formulation enables global optimization with pattern shift and floorplanning done together.
- Arbitrary Angle Rotation: The work on small-angle rotation in [25] assumes that $\sin\Theta \approx \Theta$ for all the defect-layout edge interactions, which limits the maximum allowed rotation angle. Our work does not make this assumption, which makes this approach viable even for larger rotation angles.
- Continuous: Our method explores the continuous solution space, instead of making discrete moves as done in the previous works on defect avoidance floorplanning [16] and small-angle rotation [25].

The remainder of this paper is organized as follows. Section 2 describes our problem formulation, which is followed by the details of our solution methodology in Section 3. Section 4 then shows some simulation results where we compare our method to a few previously proposed methods. Finally, we conclude this work in Section 5.

2. HOLISTIC DEFECT AVOIDANCE PROBLEM FORMULATION

In this work, we focus on EUV mask defect avoidance of single-project masks. This is because EUV is likely to be feasible only for high volume designs where single-project masks are used. Moreover, we shall assume that the floorplan of the die copies on the mask is gridded. Although this restricts the potential solution space, it guarantees full dicing yield. The number of die copies inside the mask is kept fixed. This contrasts with Du's approach [11], where the number of die copies on the defective mask is maximized.

Suppose each die copy inside the mask field has size $W_D \times H_D$, and suppose the usable mask area is $W_M \times H_M$. Suppose L layers of the design need to be patterned on L masks, and we want to place R rows and C columns of die copies on the mask. Since pattern shift and rotation can be done independently for each layer we define (Xp_l, Yp_l, Θ_l) as the coordinates of the center of the mask field relative to the center of the mask itself and

rotation of each layer, l. Mask floorplanning, on the other hand, must be done together for all the layers to ensure layer alignment. Hence we define the relative coordinates of the r^{th} row of dies relative to the zeroth row as Yf_r ($r \in 1, 2...(R-1)$), and the relative coordinate of the c^{th} column of dies relative to the zeroth column is Xf_c ($c \in 1, 2, ...C-1$). The goal of EUV mask defect avoidance is to determine this set of $3L + R + C - 2$ variables such that the impact of defects is minimized.

In order to ensure that the final mask is manufacturable, certain spatial constraints need to be satisfied by any defect avoidance solution. The various types of constraints are the following:

1. *Reticle boundary constraints* to ensure that the entire mask field is inside the usable area of the mask. These spatial constraint must account for rotation, and must be applied for each EUV layer of the design. In order to make these constraints linear, we make the small angle assumption ($\sin\Theta \approx \Theta, \cos\Theta \approx 1$).

$$\pm Xp_l \pm \frac{W_F}{2}\Theta_l \leq \frac{W_M - W_F}{2} \tag{1}$$

$$\pm Yp_l \pm \frac{H_F}{2}\Theta_l \leq \frac{H_M - H_F}{2} \tag{2}$$

2. *Maximum field constraints* to ensure that floorplanning does not move the die copies too far apart causing the maximum field constraints to be violated.

$$Xf_{C-1} + W_D \leq W_F \tag{3}$$

$$Yf_{R-1} + H_D \leq H_F \tag{4}$$

3. *Die overlap constraints* to ensure that the die copies do not overlap.

$$Xf_1 \geq W_D, Xf_{c+1} - Xf_c \geq W_D \quad \text{for} \quad c \in \{1, 2, ...(C-2)\} \tag{5}$$

$$Yf_1 \geq H_D, Yf_{r+1} - Yf_r \geq H_D \quad \text{for} \quad r \in \{1, 2, ...(R-2)\} \tag{6}$$

4. *Maximum allowed rotation* which restricts the maximum angle by which we can rotate the mask blank

$$-\Theta_{max} \leq \Theta_l \leq \Theta_{max} \tag{7}$$

This leads to a total of $8L + 2 + (C-1) + (R-1) + 2L$ linear constraints.

A key part of this defect avoidance methodology is to model the CD impact of defects as a function of these pattern shift, rotation and mask floorplanning variables. Suppose the mask corresponding to the l^{th} layer contains Nd_l defects and suppose the n^{th} defect has height $Hd_l(n)$ and full width half maximum width (FWHM) $Wd_l(n)$. Suppose the center coordinate of the defect is located at $(Xd_l(n), Yd_l(n))$ relative to the mask center. To account for pattern shift and rotation, the defect coordinates can be modified as shown in Equation 8 and 9.

$$\hat{Xd}_l(n) = Xd_l(n)cos(\Theta_l) - Yd_l(n)sin(\Theta_l) - Xp_l \tag{8}$$

$$\hat{Yd}_l(n) = Xd_l(n)sin(\Theta_l) + Yd_l(n)cos(\Theta_l) - Yp_l \tag{9}$$

Next let us consider one vertical edge of a layout shape e with x-coordinate $X(e)$ and y-coordinates $(Y_{low}(e), Y_{high}(e))$, relative to the die origin. Relative to the mask, a particular die shifts as a result of the floorplanning variables. Hence, for a die in the r^{th} row and c^{th} column, we can write the edge coordinates as shown below.

$$Xf(e) = X(e) + Xf_c \tag{10}$$

$$Yf_{low}(e) = Y_{low}(e) + Yf_r \tag{11}$$

$$Yf_{high}(e) = Y_{high}(e) + Yf_r \tag{12}$$

$$\tag{13}$$

We can then compute the distance of the edge from the defect using Equation 14, where $u(y)$ is the step function that is one if $y \geq 0$, else it is zero. Using this distance, we can then compute the CD impact of the defect on the layout shape using the linear model proposed by Clifford et. al., as shown in Equation 16.

$$r(e)^2 = (\hat{X}d_l(n) - Xf(e))^2 + (\hat{Y}d_l(n) - Yf_{low}(e))^2 u(Yf_{low}(e) - \hat{Y}d_l(n)) + (\hat{Y}d_l(n) - Yf_{high}(e))^2 u(\hat{Y}d_l(n) - Yf_{high}(e)) \quad (14)$$

$$DefHeight = Hd_l(n) \exp\left(\frac{-r(e)^2}{(Wd_l(n)/2)^2}\right) \quad (15)$$

$$CD_{def} = \frac{3D_A \cdot \sqrt{I_{NoDef}} \cdot (m_{def} \cdot DefHeight + b_{def})}{ImageSlope} \quad (16)$$

In order to ensure that the die works, we must ensure that the CD impact of the defect is less than the CD tolerance for every layout edge. Since the number of mask defects is significantly smaller than the number of absorber edges in the field pattern, we assume that a single absorber edge is not affected by more than one defect. Moreover, a defect only impacts a small set of layout edges around it, so for any given floorplan solution, we only need to look at the layout shapes within a certain distance of the defect. In this work, we take this distance as $3 * Wd_l(n) + A$, where A is the alignment error of the mask blank inspection tool. This significantly reduces the overhead of checking every defect-absorber edge pair of the mask pattern. The CD tolerance value for any absorber edge could be a single value assigned to all layout shapes, or design-aware, as done in [17].

3. RANDOM WALK + GRADIENT DESCENT BASED SOLUTION METHOD

The objective of EUV mask defect avoidance is to determine a feasible value of $Xp_l, Yp_l, \Theta_l, Xf_c$ and Yf_r such that all the spatial constraints and CD tolerance constraints are obeyed. The spatial constraints are simple linear constraints. However, the CD tolerance constraints are non-convex as proven below.

Theorem: For any absorber edge defect pair, the constraint $CD_{def} \leq CD_{tol}$ is non-convex.

Proof: Consider a left vertical edge of an absorber shape as shown in Figure 2 below. Let us consider the multi-variable function $f(Xp_l, Yp_l, \Theta_l, Xf_c, Yf_r) = CD_{def} - CD_{tol}$. By analytically computing the partial second derivative with respect to any of the pattern shift (Xp_l, Yp_l), rotation (Θ_l) or floorplanning variables (Xf_c, Yf_r) we find that it is not guaranteed to be positive for all possible defect-edge positions. This proves that all the CD tolerance constraints are non-convex. Geometrically, we can consider two potential defect locations relative to this edge, A and B as shown in Figure 2. Both defect locations obey the CD constraint, but the line segment connecting them contains positions such that will cause a violation. This implies that the geometric space of feasible defect locations relative to a single absorber edge is non-convex.

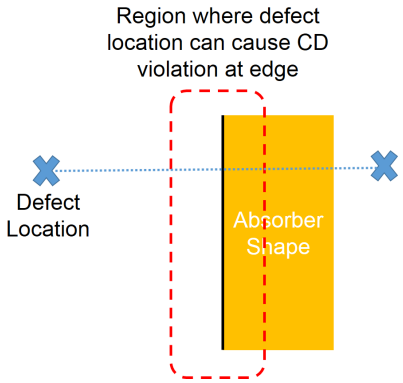

Figure 2. Illustration of non-convexity of CD constraint showing that two feasible defect locations and the segment connecting them crosses through the prohibited region for an absorber edge.

Since handling non-convex constraints is very hard in optimization, we relax the CD tolerance constraints by converting it into an objective function that we can then minimize. We use the sigmoid penalty function

to relax every CD constraint*. As a result, the cost function for our optimization problem is the sum of $sig(CD_{def} - CD_{tol})$ for all the relevant defect-edge pairs. Hence our overall optimization problem is to find the pattern shift, rotation and mask floorplanning variables to minimize this sigmoid cost function while obeying the linear spatial constraints.

To solve the non-convex optimization problem for EUV mask defect avoidance, we use a combination of random walk and gradient descent. Random walk is used to perform a coarse grained search over the n-dimensional linear polytope formed by the spatial constraints. For each of the sample points generated by random walk, we use gradient descent for local search in the vicinity of the sample. The overall method is summarized in Figure 3.

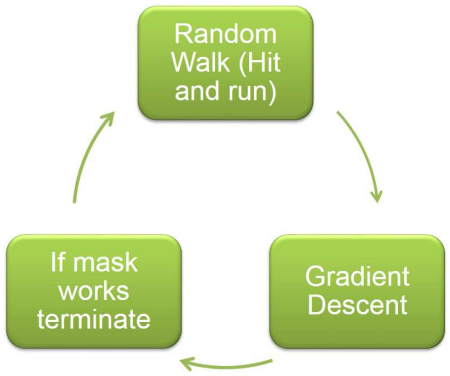

Figure 3. Illustration of the method used to solve the EUV mask defect avoidance problem.

Random walk is done using hit-and-run, which is known to be a fast mixing Markov chain random walk [20]. Hit-and-run works as follows, starting from an initial point inside the linear polytope:

1. Draw a line in a randomly chosen direction passing through the given point.
2. Find the two points where this line intersects the linear polytope.
3. Pick a random point on the line segment connecting the two points above.
4. Go back to Step 1 with this new random point.

In order to apply gradient descent to each sample point generated by random walk, we need to analytically compute the gradient of the relaxed CD tolerance objective. The analytical expression for gradient of one defect and vertical edge pair is shown in Equation 17. The value of intermediate variables Z_1, Z_2 and U_Y are shown in Equations 18, 19 and 20, respectively. Note that the discontinuity of the cost function at $Yf_{low}(e)$ and $Yf_{high}(e)$ is handled by function U_Y in Equation 20 by assuming that only one of the three conditions will hold during a round of gradient descent. Since gradient descent moves in small steps, this assumption is valid for most cases.

$$\begin{aligned}
\frac{\partial C}{\partial (Xp_l)} &= \frac{\partial C}{\partial CD_{def}} \frac{\partial CD_{def}}{\partial (r(e)^2)} \frac{\partial (r(e)^2)}{\partial (Xp_l)} &= -2Z_1Z_2 \cdot (\hat{X}d_l(n) - Xf(e)) \\
\frac{\partial C}{\partial (Yp_l)} &= \frac{\partial C}{\partial CD_{def}} \frac{\partial CD_{def}}{\partial (r(e)^2)} \frac{\partial (r(e)^2)}{\partial (Yp_l)} &= -2Z_1Z_2 \cdot U_Y \\
\frac{\partial C}{\partial (\Theta_l)} &= \frac{\partial C}{\partial CD_{def}} \frac{\partial CD_{def}}{\partial (r(e)^2)} \frac{\partial (r(e)^2)}{\partial (\Theta_l)} &= -2Z_1Z_2 \cdot (Xd_l(n)\sin\Theta_l + Xd_l(n)\cos\Theta_l) \\
\frac{\partial C}{\partial (Xf_c)} &= \frac{\partial C}{\partial CD_{def}} \frac{\partial CD_{def}}{\partial (r(e)^2)} \frac{\partial (r(e)^2)}{\partial (Xf_c)} &= -2Z_1Z_2 \cdot (\hat{X}d_l(n) - Xf(e)) \\
\frac{\partial C}{\partial (Yf_r)} &= \frac{\partial C}{\partial CD_{def}} \frac{\partial CD_{def}}{\partial (r(e)^2)} \frac{\partial (r(e)^2)}{\partial (Yf_r)} &= -2Z_1Z_2 \cdot U_Y
\end{aligned} \tag{17}$$

*$sig(x) = \frac{1}{1+e^{-\alpha x}}$, $\alpha = 4.0$ for this work

$$Z_1 = \frac{\partial C}{\partial CD_{def}} = \alpha sig(CD_{def} - CD_{tol})(1 - sig(CD_{def} - CD_{tol})) \tag{18}$$

$$Z_2 = \frac{\partial CD_{def}}{\partial (r(e)^2)} = \frac{3D_A \cdot \sqrt{I_{NoDef} m_{def}}}{ImageSlope} \cdot DefHeight \cdot \frac{-1}{(Wd_l(n)/2)^2} \tag{19}$$

$$U_Y = \begin{cases} (\hat{Yd}_l(n) - Yf_{low}(e)), & \text{if } \hat{Yd}_l(n) \leq Yf_{low}(e) \\ 0, & \text{if } Yf_{low}(e) \leq \hat{Yd}_l(n) \leq Yf_{high}(e) \\ \hat{Yd}_l(n) - Yf_{high}(e), & \text{if } \hat{Yd}_l(n) \geq Yf_{high}(e) \end{cases} \tag{20}$$

For computing the gradient and the relaxed penalty function, we need to find all the interacting defect-edge pairs, calculate the analytical expressions of Equation 17 for each such pair and then add them. Since the number of defects are typically much smaller than the number of layouts shapes, we do this by iterating over all the defects and finding all layout shapes within a certain radius $(3 * Wd_l(n))$ for each defect. We then compute the gradient for each layout edge within this radius of influence of the defect. Finding all layouts shapes within a certain radius of a defect can be done efficiently by storing the entire mask layout in a 2D region query tree data-structure [4].

The running time for computing the gradient during the iterations of local search is dominated by the process of querying the large layout repeatedly. Since only small moves are made during local search, we can avoid this overhead by upfront storing all the layout shapes that could be affected by any defect when we make small local moves. For examples, if we set the maximum number of gradient descent iterations for each random starting solution as N_G and the gradient step size is S, we can upfront store all layout shapes that are within a radius of $2N_GS + 3Wd_l(n)$ of a particular defect. At the start of gradient descent iterations, we store all such shapes for each defect. This saves the runtime of querying the large layout every time we want to compute the gradient.

4. RESULTS AND DISCUSSION

Our proposed EUV mask defect avoidance method has been implemented in C++. OpenAccess API has been used to read and access layout shapes [1]. Eigen Matrix library is used to handle vectors and matrix operations [13]. All our results are shown for an ARM Cortex M0 processor layout which was synthesized, placed and routed using Cadence Encounter with $32nm$ Synopsys Standard Cell Library. The layout is then scaled to $8nm$ technology node to show our results. The CD tolerance of every shape was set to 10% of the technology node ($0.8nm$). It is also possible to make the CD tolerance assigment design-aware, as done in [16].

For all our experiments, we assume a single size for all the defects, with peak height $Hd_l = 2nm$ and FWHM $Wd_l = 50nm$. Although our method can be applied when each defect has a different size, we chose a single size for all defects for the sake of simplicity. We show results for different number of defects on the mask so that we can highlight acceptable defect density levels for this particular defect size. Due to the lack of any industrial data on spatial distribution of buried defects, we assume that defects are uniformly distributed accross the entire usable area of the mask. 100 randomly generated spatial defect maps are considered and the percentage of these defect maps that are fixed by defect avoidance (mask yield) is the main quality metric for evaluating the efficacy of our methodology.

The number of gradient descent iterations for each random sample is set to 50 and the step size is $1nm$. We fixed the number of random walk iterations as the ratio of volume of the linear spatial polytope and the volume of the multi-dimensional ($3L + R + C - 2$ dimensions) ball that is covered by gradient descent. The rationale behind this choice is to ensure equivalent coverage of the available space when we compare different scenarios. The volume of the linear polytope was computed using the tool VINCI [5], and the volume of the gradient ball can be computed using a simple analytical expression [2].

We assume that four rows and three columns of die copies of this ARM processor can be placed inside the mask field. We allow a maximum pattern shift of $20\mu m$, small-angle rotation of 6^o and maximum allowed scribe area to be 1%. Scribe area is defined as the difference in area between the total area of all the die copies inside the

Table 1. Summary of mask yield after defect avoidance using prior methods

Defect Count	Prohibited Region		Simulated Annealing [16]	
	Pattern Shift [24]	Pattern Shift + Rotation [25]	Pattern Shift	Pattern Shift + Mask Floorplanning
10	100%	100%	100%	100%
20	81%	100%	100%	100%
30	8%	97%	0%	6%
40	1%	11%	0%	0%
50	0%	0%	0%	0%

Table 2. Summary of mask yield after our defect avoidance method with different flexibility

Defect Count	Pattern Shift	Pattern Shift + Rotation	Pattern Shift + Mask Floorplanning	Pattern Shift + Rotation + Mask Floorplanning
10	100%	100%	100%	100%
20	100%	100%	100%	100%
30	35%	91%	55%	100%
40	3%	10%	9%	74%
50	0%	1%	2%	13%

field pattern and the total field size ($W_F \times H_F$). Since the size of one ARM Cortex M0 layout is $162\mu m \times 159\mu m$, the total field size becomes $486\mu m \times 636\mu m$ and the usable area of the mask is $511\mu m \times 662\mu m$. Note that although this is much smaller than the full field size of $132mm \times 104mm$, we have analyzed smaller layouts in order to get reasonable runtimes, especially since we perform Monte Carlo analysis over 100 random defect maps. Moreover, this smaller set is sufficient to demonstrate the benefit of our proposed defect avoidance method and compare it with previous approaches.

4.1 Comparison with Other Defect Avoidance Methods

Mask yield after defect avoidance using two prior methods is shown in Table 1. Prohibited region based defect avoidance methods [24, 25] allows continuous pattern shift and small angle rotation, but cannot handle mask floorplanning. Simulated annealing based defect avoidance method [16] allows pattern shift and mask floorplanning, but arbitrary angle rotation is not possible. With our implementations of both these methods, we found that prohibited region based methods perform significantly better than simulated annealing. The reason for that is that the prohibited region based method allows continuous pattern shift instead of making discrete jumps. As a result, the solution space is explored more efficiently.

Table 2 shows mask yield using our defect avoidance method, using the different degree of freedom. Notice that even if defect avoidance is limited to pattern shift, our method performs better than both prohibited region and simulated annealing based methods. Our method performs significantly better than prohibited region based defect avoidance because prohibited rectangle construction is inherently pessimistic at corners of absorber shapes, as illustrated in Figure 4 (CD impact of defect depends to Euclidean distance from absorber edge). When pattern shift and rotation are both allowed, our method is slightly worse than prohibited region based methods because of the number of random walk iterations we set. Given enough iterations, our method can always reach the best possible solution. More importantly, by allowing mask makers to exploit all three degrees of freedom for defect avoidance, our method allows significantly better mask yield compared to these earlier approaches. For a 40-defect mask, the mask yield of prohibited region based defect avoidance with rotation is just 11%. But our method is able to improve mask yield to 74%.

4.2 Analysis for Multiple Layer Defect Avoidance

Our earlier analysis focused on just the polysilicon layer, which is typically the most critical layer. If more layers need to be patterned using EUV lithography, defect avoidance needs to be applied for each of the corresponding masks. Although pattern shift and rotation can be done independently for each of these layers, mask floorplanning must be done together to ensure alignment.

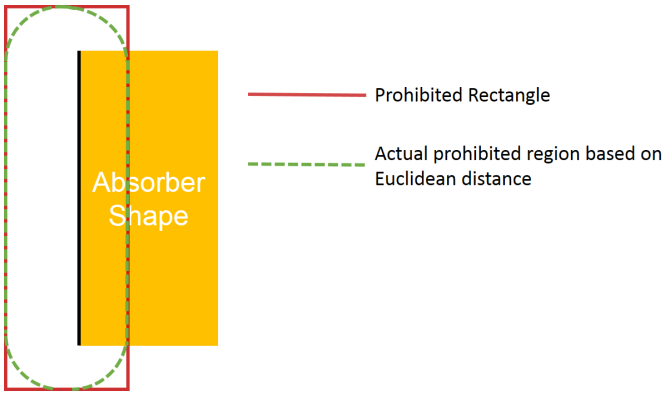

Figure 4. Pessimism of prohibited rectangle construction compared to true prohibited region based on Euclidean distance for one absorber edge.

As described in Section 2, our method can handle multiple layer defect avoidance as well. However the number of variables increases by 3 every time an additional layer is patterned using EUV. If we were to set the number of random walk iterations based on volume of the linear polytope and gradient ball as done earlier, then the number of random walk iteration would be around 10^{10}. Since this would take too much runtime, we decided to fix the number of random walk iterations as 10^7 for all cases in this sub-section. This makes the exploration of solution space less efficient for multi-layer cases.

We have summarized the results for single layer (polysilicon only), two layer (polysilicon and active) and four layer (polysilicon, active, contact and metal 1) scenarious in Figure 5. Note that mask yield here is defined as the percentage of cases where all the layers work. As a result, mask yield is lower in case of multi-layer cases. Up to 30 defects, mask yield is close to 100% for all cases. Then the mask yield for multiple layer cases reduces as we add more layers, which is expected.

In this analysis, we have ignored the problem of mask blank assignment, as done in [9], and we assigned a mask blank to a particular layer independently. Moreover, it has been shown that regular layout topologies like polysilicon layer tend to have lower mask yield than other layers [18]. Multi-layer defect avoidance methodology could utilize this fact by modifying the cost function appropriately to improve overall mask yield. This has not been explored in this work.

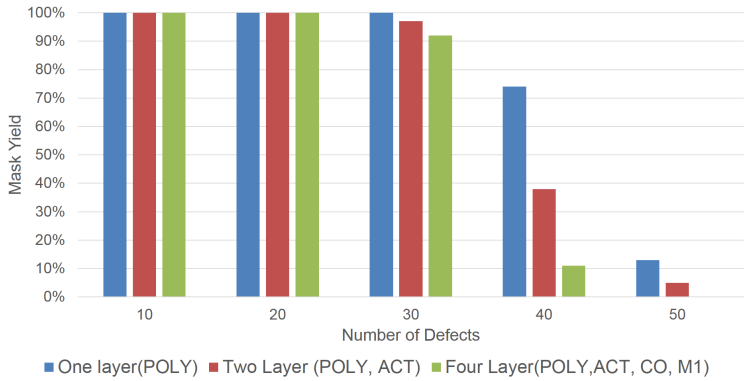

Figure 5. Comparison of mask yield after defect avoidance when multiple layers of a design is patterned using EUV lithography.

4.3 Impact of Spatial Constraints on Defect Avoidance

There are three key manufacturing constraints (corresponding to each of the three degrees of freedom) that strongly affect the potential benefit from defect avoidance:

- Maximum Pattern Shift is the difference between the size of usable area of mask and the size of pattern field ($(W_M - W_F) \times (H_M - H_F)$ in Equations 1 and 2).
- Maximum Rotation Angle is the largest angle by which the mask blank can be rotated relative to the field pattern. It is the value of Θ_{max} in Equation refeqn:angleCon.
- Maximum Scribe Area is the difference in area between the total area of all the die copies inside the field pattern and the total field size ($W_F \times H_F$), expressed as a percentage of the total field area.

These three manufacturing constraints limit the solution space availale for avoiding defects and hence can affect the mask yield strongly. We shall analyze the impact of each of these constraints in this sub-section. For the sake of brevity, we shall only analyze the single layer scenario (polysilicon layer), and we will report the mask yield for 40-defect masks.

The impact of maximum pattern shift is shown in Figure 6. Note that all our prior analysis was done assuming a maximum pattern shift of $20\mu m$. Here we look at values ranging from $10\mu m$ to $100\mu m$. For the layout we chose to analyze, mask yield for 40-defect mask was 100% for pattern shift values larger than $50\mu m$. We also computed the volume of the linear polytope formed by all the spatial constraints of the defect avoidance optimization problem because this volume is a good indicator of the potential mask yield benefit from defect avoidance.

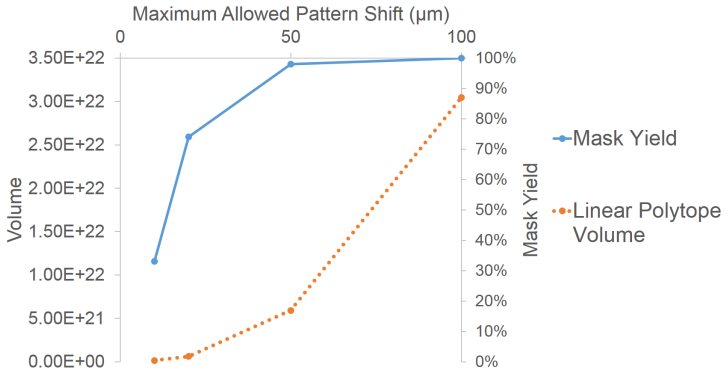

Figure 6. Volume of Linear Polytope and Mask Yield for 40 defect mask with respect to Maximum Allowed Pattern .

Similarly, the benfit of rotation is highlighted in Figure 7. Both mask yield for a 40-defect mask, and linear polytope volume is plotted for maximum rotation angle (Θ_{max}) ranging from 0 degrees to 10 degrees. The interesting thing to note here is that mask yield saturates at around 80%. The reason for this is that the overall solution space does not grow due to reticle boundary constraints.

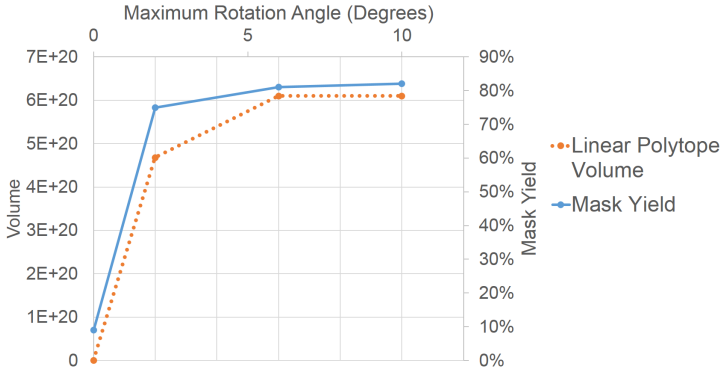

Figure 7. Volume of Linear Polytope and Mask Yield for 40 defect mask with respect to Maximum Allowed Rotation.

Lastly the impact of scribe area is shown in Figure 8. Mask yield can improve up to 100% with scribe area of 5%. Note that this improvement comes at the expense of wasted space on the wafer.

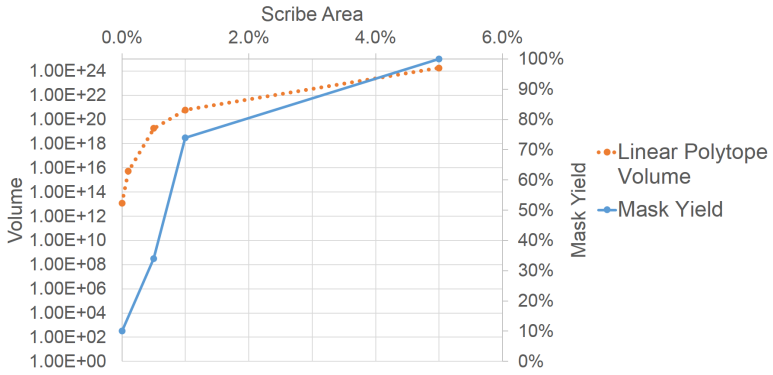

Figure 8. Volume of Linear Polytope and Mask Yield for 40 defect mask with respect to Maximum Allowed Scribe Area.

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5. CONCLUSION

In this work, we proposed a complete EUV mask defect avoidance method that can explore all the available degrees to freedom: pattern shift, rotation and mask floorplanning. Our method is generic and capable of being adapted for any mask defect model. Moreover, our method can handle multiple layers of a design and can explore the continuous solution space.

We modeled EUV mask defect avoidance as a global optimization problem with non-convex objective and linear constraints. We then solved the problem using a combinatuon of hit-and-run based random walk and gradient descent. Compared to previously proposed methods for defect avoidance, our method can fix more mask blanks and hence allow tolerance to a larger number/size of defects than possible with previous methods. For a 40-defect mask, our defect avoidance method was able to improve mask yield by more than 60%-point compared to previously proposed method for defect avoidance.

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