EUV-CDA: Pattern Shift Aware Critical Density Analysis for EUV Mask Layouts

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***Abstract*—Despite the use of mask defect avoidance and mitigation techniques, finding a usable defective mask blank remains a challenge for Extreme Ultraviolet Lithography (EUVL) at sub-10nm node due to dense layouts and low CD tolerance. In this work, we propose a pattern shift-aware metric called critical density, which can quickly evaluate the robustness of EUV layouts to mask defects ($300-1300\times$ faster than Monte Carlo, with average mask yield root mean square error (RMSE) ranging from $0.08\%-6.44\%$), thereby enabling design-level mask defect mitigation techniques. Our experimental results indicate that reducing layout regularity improves the ability of layouts to tolerate mask defects via pattern shift.**

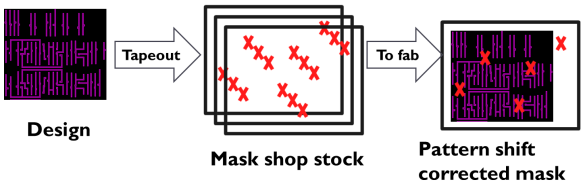


Fig. 1. Set of steps involved in a EUV mask shop involving pattern shift based mask defect mitigation.

I. Introduction

A. Background and Motivation

Extreme ultraviolet lithography is considered one of the most promising next generation lithography solutions to replace the current deep ultraviolet lithography [1]. Reflective EUV mask blanks suffer from hard-to-repair defects that can significantly alter the printed pattern on the wafer [2]. Mask blank defectivity is a key concern that could prevent the insertion of EUVL into volume manufacturing [1], [3].

Defect avoidance based techniques have emerged as an effective means to tolerate mask defects. These techniques rely on inspection of mask blanks to first determine defect locations. The position of the design pattern, which needs to be written on the mask, can be shifted relative to the mask to avoid the defects. Several approaches and results have been shown for such pattern shift based defect avoidance [4]–[7]. A similar, but more general mask floorplanning based defect avoidance has been proposed as well [8], [9]. Rotation of the mask pattern has also been explored, either small-angle [10] or 180^o/flips [8]. Recent techniques have also looked at methods that can tolerate defect position inaccuracy [8], [11]. Elayat et. al. [12] and Jeong et. al. [13] provide a cost-benefit assesment of different defect avoidance and reticle planning strategies, respectively.

A likely design to fabrication flow for EUV masks is illustrated in Figure 1. A mask shop will typically have a collection of inspected mask blanks with known defect locations. Since each critical layer of the taped out design must be patterned on a defective mask blank, the mask shop must apply defect avoidance to find a defective mask blank that works for each layer. *Given a defect density and size distribution, the probability of finding a mask blank from a large set of blanks on which the given design layout can be patterned without causing any yield loss is referred to as mask yield.*

Certain layout topologies may be more capable of tolerating mask defects, and exploiting the benefits of defect avoidance strategies. An understanding of what characteristics of a layout can make it more robust to EUV mask defects can significantly aid EUV layout design and even the formulation of design rules. In order to develop any layout or design level techniques to create robust layouts, a quantifiable metric that characterizes the robustness of layouts to such mask defects is needed. In addition to layout optimization, such a layout robustness metric can be used for mask blank assignment as well. Layouts with low mask yield can be assigned to a mask blank with lower defect density. This would save the computational effort of performing pattern shift for each layout-blank pair, as done in [14].

B. Key Contributions of this Work

In this work, we propose a new metric, *critical density*, that evaluates the robustness of EUV layouts to mask defects. To the best of our knowledge, this work is the first attempt towards developing such a metric. This metric allows us to estimate pattern shift aware mask yield for any defect density using a simple analytical expression, and enables us to distinguish between layouts that have different mask yield for any given defect density.

The need for a metric that quantifies robustness of layouts to mask defects bears resemblance to conventional critical area analysis (CAA) [15]. CAA is commonly used to check robustness of layouts to random $wafer$ defects through the use of statistical metrics that estimate chip yield for some random distribution of defects. The key features of this work that also distinguish EUV-CDA and conventional CAA are the following:

- Unlike wafer defects, a single mask defect will print on every copy of the design on the wafer. Hence, the goal of EUV-CDA is to predict mask yield, not chip yield.
- The impact of defect avoidance techniques on mask yield must be probabilistically modeled as a part of EUV-CDA since actual defect locations are not known at the design stage. Pattern shift based defect avoidance is modeled in this work since it is the most popular defect avoidance strategy [12].
- The need to account for pattern shift means that mask failure depends on the simultaneous location and size of several defects on the mask. This is in contrast to conventional CAA, where every defect can cause failure independently. This dependence complicates the analysis significantly, requiring much more computational effort and modeling.

The remainder of this paper is organized as follows. Prohibited region of a layout is described in Section II. In Section III, we propose analytical methods to estimate mask yield for two limited scenarios.

TABLE I
GLOSSARY OF TERMINOLOGY

Term	Description
s	Defect size (Height, full width half maximum pair)
PB^s	Prohibited Region for defect size s
$P(s)$	Probability of occurrence of defect size s
A_M	Mask area
D_P^s	Prohibited region density ($\frac{Area(PB^s)}{A_M}$)
D_P	Expected prohibited region density ($\sum_s P(s)D_P^s$)
K	Number of different defect sizes considered
N_d	Number of defects on mask
Δ_X	Available pattern shift in X direction
Δ_Y	Available pattern shift in Y direction
A_Δ	Total pattern shift area ($\Delta_X \times \Delta_Y$)
L_X	Design layout width
L_Y	Design layout height
A_L	Total design area ($L_X \times L_Y$)
ρ	Number of prohibited region shapes per unit area
N_X	Number of discrete X direction shifts
N_Y	Number of discrete Y direction shifts
(X_i, Y_j)	Potential pattern shift solution
E_{ij}^Δ	Event that pattern shift solution (X_i, Y_j) works
$P(E_{ij}^\Delta)$	Probability of event E_{ij}^Δ
PB_{ij}^s	Prohibited region for defect size s, shifted by (X_i, Y_j)
$Ar(PB_{ij}^s)$	Total area of all the polygons in the prohibited region
W_{pl}	Width of periodic parallel line structure
P_{pl}	Pitch of periodic parallel line structure
Y_M^{ct}	Mask Yield of periodic contact array layout
D_{cric}	Critical density
Y_M^{true}	Accurate mask yield (Monte Carlo method)
N_d^{min}	Minimum defect count considered
N_d^{max}	Maximum defect count considered
AC	Autocorrelation matrix
ACF	FFT of AC
pix	Pixel size (Sampling size) for computing AC
N_F	Number of terms from ACF used for predicting D_{cric}

We describe our critical density method in Section IV. Experimental results are then presented in Section V. We conclude this work in Section VI. All notation used in this paper is described in Table I.

II. PROHIBITED REGION

We define the prohibited region of a given layout, for a particular defect size s, as the set of polygons PB^s such that if the center of a mask defect lies inside any polygon $p \in PB^s$, the given mask layout pattern will not yield.

The method for constructing prohibited region is the same as proposed by Zhang et. al. [5] with the additional step of merging the constructed rectangles. It is similar to the process of using simple Boolean operations to compute critical area in conventional CAA [15]. *But the criteria for determining prohibited region is CD tolerance, in constrast to opens/shorts in conventional CAA.* We chose this pessimistic approach since we are dealing with mask defects. Assignment of this CD tolerance to layout shapes can be done by either setting a single pessimistic value for all the patterns (10% of the technology node, in our case), or by using some design information (timing slack, redundant/dummy patterns) to assign an appropriate CD tolerance, as done in [16]. Although EUV-CDA can be easily applied for such smart CD tolerance, for the sake of brevity we assign a single CD tolerance to all shapes in this work.

If pattern shift was not a part of EUV mask manufacturing, estimating mask yield from prohibited region would be fairly straightforward. Assuming a uniform spatial distribution of defects on the mask, mask yield could be estimated as $(1 - D_P^s)^{N_d}$ since every defect must lie outside the prohibited region[1]. This simple approach would imply that any two design layouts with the same prohibited region density will have the same mask yield. But if pattern shift is used to avoid mask defects, layout topology may also affect mask yield. To confirm this suspicion, we created four $20\mu m \times 20\mu m$ layouts such that their prohibited region is a set of parallel lines with pitch $80nm$. The width of the lines was treated as a Gaussian random variable with mean $20nm$. Different values of variance (σ) were used to construct the four layouts. We compared the mask yield of these four layouts, which is estimated using rigorous Monte Carlo simulation (described in Section III). The results, shown in Figure 2, highlight the huge difference in post pattern shift mask yield between the layouts which have very similar prohibited region density (confirmed by the pre-pattern shift mask yield of the four layouts, which are almost same).

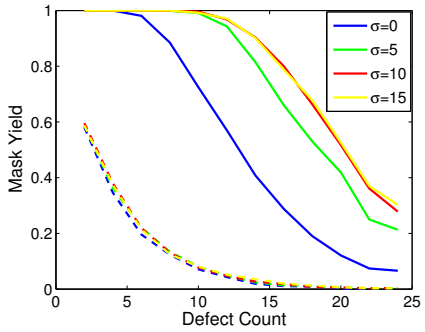


Fig. 2. Comparison of pre-pattern shift (dashed lines) and post-pattern shift (solid lines) mask yield of four parallel line layouts with same prohibited region density but different σ of Gaussian width.

III. APPROXIMATE ANALYTICAL METHODS

Monte Carlo based mask yield estimation is a simple, but computationally expensive strategy of generating random defect maps and performing pattern shift for each defect map. Mask yield can then be computing as the ratio of samples for which the final mask works, i.e. every defect on the mask is avoided. The Monte Carlo method starts off by constructing the prohibited region for different defect sizes. We then generate a defect map with N_d defects, assigning a size to each defect based on the given defect size distribution $P(s)$. Pattern shift is then applied for this defect map to determine if a feasible solution exists. Note that for each Monte Carlo iteration, N_d defects need to be generated since pattern shift makes mask failure dependent on location of several defects on the mask. This dependence necessitates a large number of Monte Carlo iterations to achieve convergence. The methodology we used for pattern shift is the same as the approach proposed by Wagner [6], which is optimal with respect to mask yield.

This naive method of estimating mask yield, although accurate, is cumbersome and slow, requiring many Monte Carlo iterations to give accurate results. Therefore this method of estimating mask yield is impractical for realistic layouts. Moreover, the method does not provide any design insights that could help improve the mask yield of a given layout. Despite these limitations, the accuracy of this method makes it appropriate for validating the faster, approximate method that we shall propose in this paper.

[1]All defects are assumed to be of size s in this example.

A. Inclusion-Exclusion Method

In this section, we propose a method to estimate the mask yield with one simplifying assumption: pattern shift picks a feasible solution from a finite set of alternatives.

Let us first discretize all the potential defect sizes, into K discrete defect sizes, $s_1, s_2, ..., s_K$ with respective probabilities of occurrence, $P(s_1), P(s_2), ..., P(s_K)$. For a uniform spatial distribution of defects, we can then calculate the probability that a particular pattern shift solution (X_i, Y_j) works using Equation 1. Note that $\frac{Ar(PB_{ij}^{s_k})}{A_M}$ is equal to the prohibited region density for defect size s_k since shifting the polygons does not change area.

$$P(E_{ij}^{\Delta}) = \left(\sum_k P(s_k) \left(1 - \frac{Ar(PB_{ij}^{s_k})}{A_M} \right) \right)^{N_d} \quad (1)$$

Pattern shift aware mask yield can be estimated as the union of all the events E_{ij}^{Δ} since the mask will yield if any of the potential solutions work (Note that a solution is picked once the defect locations are known). Calculating this union of events can be done using inclusion-exclusion principle as shown in Equation 2.

$$P(\cup_{i,j} E_{ij}^{\Delta}) = \sum P(E_{mn}^{\Delta}) - \sum P(E_{pq}^{\Delta} \cap E_{mn}^{\Delta}) \ldots \quad (2)$$

The second order intersection term $P(E_{pq}^{\Delta} \cap E_{mn}^{\Delta})$ corresponds to the event that all defects lie in the non-prohibited region of both solution E_{pq}^{Δ} and E_{mn}^{Δ}. Hence, it can be computed using a polygon Boolean OR operation as shown in Equation 3.

$$P(E_{pq}^{\Delta} \cap E_{mn}^{\Delta}) = \left(\sum_k P(s_k) \left(1 - \frac{Ar(PB_{pq}^{s_k} \cup PB_{mn}^{s_k})}{A_M} \right) \right)^{N_d} \quad (3)$$

Computation of all the inclusion exclusion terms comprising $N_X \times N_Y$ orders (only first two order are shown above), is a $\#P$-complete combinatorial enumeration problem since it requires the computation of $2^{N_X \times N_Y}$ terms [17]. This computational limitation, along with the quantization error incurred due to the assumption that the pattern shift solution space is discrete, make this method unsuitable for estimating mask yield for any realistic layouts.

Despite the impracticality of the inclusion-exclusion method, it does provide one interesting insight: *in addition to prohibited region density, mask yield depends on autocorrelation of the prohibited region of the input layout.* The second order terms in Equation 3, $Ar(PB_{pq}^{s_k} \cup PB_{mn}^{s_k})$, are linearly related to $Ar(PB_{pq}^{s_k} \cap PB_{mn}^{s_k})$, which measures the degree of overlap between the prohibited region PB^{s_k} with a shifted transform of PB^{s_k} (shifted by $(X_p - X_m, Y_q - Y_n)$). Each such overlapping area corresponds to one entry of the autocorrelation matrix of the 2D binary prohibited region signal, PB^{s_k}. Moreover, mask yield depends on the weighted sum of the prohibited region autocorrelation for different defect sizes. We will later leverage this dependence of mask yield on the weighted autocorrelation of prohibited region for critical density computation.

B. Spacings Method

In this sub-section, we will show that *if the prohibited region of a given layout is regular, the problem of finding the post-pattern shift mask yield can be mapped to the maximal spacing distribution problem, a classic geometric probability problem.* Note that pattern shift is assumed to be continuous here, unlike the previous sub-section. Also, we consider only one defect size s here, and the assumption on regularity is for the prohibited region, PB^s.

First, suppose the prohibited region of the entire layout is a periodic parallel line structure. Assuming the lines are infinitely long and parallel to Y axis, any pattern shift in Y direction will not improve mask yield. Hence, only the X coordinates of the defects is relevant, and we can map all the defects to a single line. The periodicity assumption implies that the X coordinates of all the defects can be mapped to a modulo P_{pl} space with a single line of width W_{pl}. An optimal pattern shift based defect avoidance technique can successfully avoid all the defects, if and only if there exists a gap or spacing of size W_{pl} with no defect inside it. This mapping is illustrated in Figure 3.

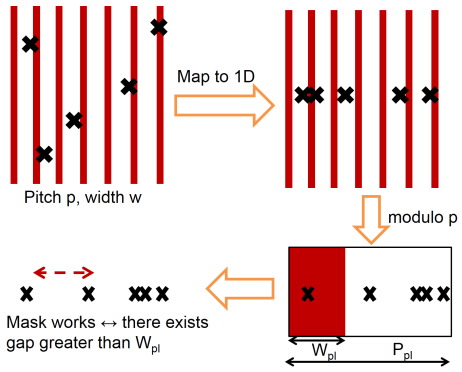


Fig. 3. Mapping mask yield estimation of parallel line to maximal spacing distribution.

This problem is equivalent to finding the probability of existence of a gap larger than $\frac{W_{pl}}{P_{pl}}$ on a unit circle with a uniform distribution of points [2]. This geometric probability, also referred to as the one dimensional maximal spacing problem [18], was first computed exactly by Stevens [19], which allows us to estimate pattern shift aware mask yield of a parallel line layout.

Similar to the parallel line case above, we can show that the the mask yield for a regular, square contact array pattern is equivalent to the two-dimensional maximal spacing distribution. Janson derived an asymptotic analytical expression for the multi-dimensional maximal spacing problem [20], that holds true as the number of random points (defects, in our case) tend to infinity. Using his expression, we can estimate pattern shift aware mask yield for an infinite contact array layout as shown in Equation 4. An additional condition is included for $N_d \leq \frac{2}{D_P}$ to correct for the anomaly that mask yield increases with increase in the number of defects. This analytical expression will be referred to as Janson's formula in the rest of this paper.

$$\begin{aligned} Y_M^{ct} &= 1 - e^{-N_d^2 D_P e^{-N_d D_P}} && if \quad N_d \geq \frac{2}{D_P} \\ &= 1 && otherwise \end{aligned} \quad (4)$$

IV. Critical Density Method

Although the periodicity assumption of parallel line and contact arrays enables us to map the yield estimation problem to a maximal spacing distribution problem, deriving such analytical expressions for random layouts is not straight-forward. In order to address the issue of estimating the yield of realisitic layout patterns, we propose a two-step model that applies principles from Section III-A and III-B.

We first define critical density of a layout as follows. *For any given input layout, critical density is the value of D_P such that Equation*

[2]Since there is no mask defect distribution data available, we assume uniform spatial distribution of defects as it usually gives more pessimistic yield estimates compared to clustering [6], [13]

4 can most accurately predict the actual mask yield of the layout for any number of defects. Mathematically, we can use the ubiquitous least squares as the criteria for accuracy and thereby define critical density as given in Equation 5.

$$D_{crit} = \underset{0 \le D_P \le 1}{\operatorname{argmin}} \sum_{N_d=N_d^{min}}^{N_d=N_d^{max}} (Y_M^{ct}(N_d, D_P) - Y_M^{true}(N_d))^2 \quad (5)$$

With this definition of critical density, our two-step model first estimates critical density of an input layout using the weighted autocorrelation matrix of the prohibited region as the predictor variables (motivated by the derivation in Section III-A). Equation 4 is then used to estimate mask yield.

The use of critical density as a part of a two-step model to estimate mask yield abstracts out defect density thereby providing a defect density-independent metric that depends solely on the prohibited region of a given layout. This metric can be used to compare the robustness of different layouts to EUV mask defects. Additionally, critical density is similar to probability of failure (ratio of critical area to chip area) in conventional CAA.

For a realistic full chip layout, using the entire autocorrelation matrix of a layout as a feature set to predict critical density is infeasible, both from the perspective of computing the autocorrelation, and fitting a model ("curse of dimensionality"). We propose the following set of steps to reduce the dimension of the autocorrelation matrix which is then used to predict the critical density:

- *Limited autocorrelation:* Based on the derivation in Section III-A, only the first $\frac{\Delta_X}{pix} \times \frac{\Delta_Y}{pix}$ entries of the autocorrelation matrix of size $\frac{L_X}{pix} \times \frac{L_Y}{pix}$ need to be considered as a part of the feature set. Moreover, we scale all the entries of the autocorrelation matrix by the reticle area, to make it independent of design size.
- *Compression:* Only the low-frequency Fourier components of the limited autocorrelation matrix are used as features for predicting critical density. This is reasonable since layouts are dominated by lower frequency components due to design rule constraints.

With this reduced autocorrelation based feature set, we apply a simple multivariate linear regression model to predict critical density of any given layout. Since the autocorrelation matrix size depends on the maximum available pattern shift and is scaled by reticle size, it is independent of the layout size. Therefore the linear regression model can be trained using small layout clips, and the trained model can then be applied to large realistic designs. This makes the training of the model manageable.

The operations involved in computing critical density, and then mask yield, of a given random layout are specified in Algorithm 1. *Note that the two-step critical density model does not assume discrete pattern shift solutions.* It actually accounts for the optimal continuous pattern shift since the linear model that estimates critical density is fitted using the Monte Carlo method that uses the optimal continuous pattern shift.

The runtime for estimating critical density is dominated by the polygon Boolean operations to compute the autocorrelation matrix. Each polygon Boolean operation takes $O(\rho A_L \log \rho A_L)$ runtime. With a sampling pixel size of pix, fast fourier transform can be performed in $O(\frac{A_\Delta}{pix^2} \log \frac{A_\Delta}{pix^2})$. Hence, the runtime order complexity to compute the critical density is $O(K \times \frac{A_\Delta}{pix^2} \times \rho A_L \log \rho A_L + \frac{A_\Delta}{pix^2} \log \frac{A_\Delta}{pix^2})$. In constrast, the order complexity of Monte Carlo is $O(N_d \times (\rho A_\Delta \log \rho A_\Delta + (\log \rho A_L)^3)))$ per iteration[3]. This method can also be easily parallelized by computing each entry of the autocorrelation matrix independently.

Algorithm 1 Steps for estimating critical density

Input: Design layout of size $L_X \times L_Y$ and total shift size permitted $\Delta_X \times \Delta_Y$. Tunable parameters: sample size for autocorrelation pix, and number of fourier order to pick N_F

Output: Critical density of layout.

1: Construct prohibited region of layout PB^s for $s \in s_1, s_2, ...s_K$
2: Define matrix AC of size $\frac{\Delta_X}{pix} \times \frac{\Delta_Y}{pix}$
3: reticleArea = $(L_X + \Delta_X) \times (L_Y + \Delta_Y)$
4: **for all** $X_i \in \{0, p, 2p, ...\Delta_X\}$ **do**
5: **for all** $Y_j \in \{0, p, 2p, ...\Delta_Y\}$ **do**
6: $AC(\frac{X_i}{pix}, \frac{Y_j}{pix}) = \sum_k P(s_k) \frac{Area(PB^{s_k} \cup PB_{ij}^{s_k})}{A_M}$
7: **end for**
8: **end for**
9: $ACF = fft(AC)$
10: Pick all terms of ACF with Fourier order less than or equal to N_F
11: Apply fitted linear model to get critical density

V. Experimental Results

Both the Monte Carlo method, and our proposed critical density method are implemented in C++. OpenAccess API [21] is used to read and query layouts. The polygon Boolean operations are performed using Boost Polygon Library [22]. Fourier transform of the autocorrelation matrix is done using FFTW library [23], and matrix operations are done using Eigen [24]. OpenMP is used to parallelize both the Monte Carlo Method[4] and the autocorrelation matrix construction step of our critical density method, with eight threads for execution. All our computation has been done on a high performance compute cluster. The reported runtime for the various testcases is the wall time on the compute nodes of the cluster.

The number of Monte Carlo iterations is kept fixed at $20,000$ for all the training clips and test layouts. For all our testcases, the Monte Carlo method is run 15 times, with defect density ranging from 10 defects to 150 defects. All of our reported average, maximum and average root mean square error (RMSE) values are across this range of defects.

All our analysis in this section is done on designs created using Synopsys $32nm$ standard cell library [26], and scaled down to $8nm$. The designs were synthesized, placed and routed using Cadence Encounter [27] with 90% cell utilization, unless otherwise stated.

All mask defects are taken as 3D Gaussian-shaped, with three discrete height values $(0.5nm, 1.0nm, 2nm)$ and three discrete full width half maximum values $(25nm, 50nm, 75nm)$. The corresponding nine discrete defect sizes are assigned probability of occurrence inversely proportional to their respective volume. The CD tolerance of all the shapes was set at $0.8nm$.

The available pattern shift $(\Delta_X \times \Delta_Y)$ is taken as $0.5\mu m \times 0.5\mu m$. Current literature on pattern shift suggest that the total available shift is around $200\mu m \times 200\mu m$ [7]. A smaller shift value is chosen to demonstrate our methodology since the runtime of the validation Monte Carlo method becomes too slow with large shift area ($\geq 5,000$ hours based on the runtime of [5]). Moreover, the shift area we have

[3]Number of Monte Carlo iterations also depends on A_L and A_Δ

[4]Thread-safe random number generation is done here [25]

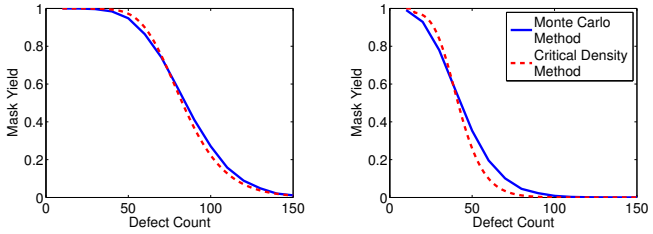
chosen is sufficient for comparing different layouts since it is large enough to cover several pitches at $8nm$ node. pix is set to $20nm$ [5], and the size of the autocorrelation based feature vector for each layout is 17. It comprises all the entries from the FFT matrix of the limited autocorrelation matrix with both row and column indices less than 4, and a constant.

The linear regression model to estimate critical density of a layout is trained using $5\mu m \times 5\mu m$ layout clips obtained from a large $32nm$ layout. We used a total of 400 layout clips from each of the four critical layers of a design as the training set: polysilicon, metal 1, contact and active. For these small layout clips, we used the Monte Carlo method to estimate the true mask yield for different number of defects. Using this data, we computed the critical density of the layout clips by solving Equation 5 in MATLAB with the interior point method. The autocorrelation based features are computed for each clip, and used to train the linear regression model for critical density in MATLAB.

A. Model Validation

The trained linear regression model is then applied on different layers of four benchmark layouts from ISCAS'89 [28], and one RISC processor layout. All these layouts are different from the training clips used to fit the model. The results are summarized in Table II [6].

Compared to the rigorous Monte Carlo method, our critical density method is able to predict critical density fairly accurately for all the test layouts with a runtime improvement ranging from $300\times$ to $1300\times$ The average RMSE in estimating mask yield ranges from $0, .08\% - 6.44\%$. Moreover, the method is able to track the general trend of how mask yield changes with defect density fairly accurately. This is illustrated in Figure 4, which plots the mask yield versus defect density of the Monte Carlo and the critical density method for the polysilicon and metal 1 layers of $s1423$.



(a) Metal 1 layer (b) Polysilicon layer

Fig. 4. Mask yield versus defect density for two layers of s1423 design

B. Impact of Layout Density and Regularity

The critical density of a layout is strongly influenced by the layout density. This is confirmed by comparing two version of s1196 in Table II with cell utilization of 90% (default) and 70%. Reducing the cell utilization reduces the layout density of all the layers, thereby reducing the critical density as well. Moreover, note that different designs constructed with the same utilization have almost equal critical density for each respective layer. This suggests that critical density depends on global layout characteristics instead of local hotspot-like regions. Hence, improving this metric may necessitate changes in design rules or physical design techniques.

[5]Pixel size only dictates the shift values for which the Boolean AND operations are performed.

[6]The validation Monte Carlo method is too slow to be run for the larger processor layout, hence the missing entries in the table.

Although layout density plays an important role in determining critical density, it is not the only factor that affects critical density. Polysilicon layer (which is a fixed pitch regular grating) has higher critical density compared to irregular metal 1 layer of each design, despite lower layout density. This indicates that random layout patterns are better suited to exploit the benefits of pattern shift due to better autocorrelation properties. To further highlight this impact of regularity, we constructed two regular layouts, parallel line and contact array, which have the same layout density as the polysilicon layer of $s1423$ and metal 1 layer of $s1196 - u70$. The results, shown in Figure 5, highlight two key aspects of layouts that affect mask yield:

- 1D layout topology (parallel line and polysilicon), are significantly worse than 2D topology (contact array and metal 1) because 2D layouts can benefit from pattern shift in both X and Y directions, whereas 1D layouts benefit only in the direction perpendicular to the parallel lines.
- An irregular 2D layout like metal 1 is much better suited to derive the benefit of pattern shift compared to a regular 2D contact array.

Most manufacturing processes, especially lithography, favor 1D regular layouts. This has led to increasing layout regularity with each technology node. But our results show that the reduced mask yield of such regular layouts can significantly increase mask cost for EUV lithography. Hence, a systematic co-optimization to balance these two competing requirements may be required for EUV layouts.

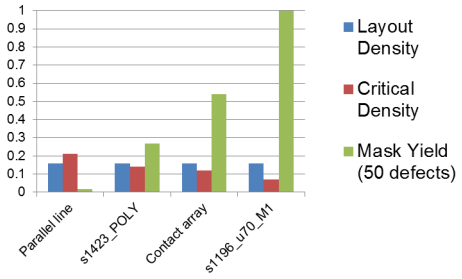


Fig. 5. Illustration of impact of regularity on critical density (and consequently, mask yield) for layouts with same density.

VI. Conclusion and Future Work

In this work, we proposed a new metric for evaluating the robustness of EUV layouts with respect to mask defects, critical density. Using critical density, layout designers and mask makers can quickly estimate the probability of finding a defective EUV mask blank on which the layout can be safely patterned for any defect density(mask yield). Our method accounts for the impact of pattern shift based defect avoidance technique on mask yield, which is the most challenging part of this methodology. We first solved the problem assuming discrete pattern shift solutions using inclusion-exclusion. Then we mapped the problem to a classic geometric probability problem, maximal spacings, for the limited case of parallel line and contact array patterns. Using principles from both these approaches, we defined our critical density metric and proposed a novel method to estimate critical density, which can then be used to estimate the pattern shift aware mask yield for any arbitrary layout. Our method was shown to be $300 - 1300\times$ faster than the rigorous Monte Carlo method for estimating mask yield and was able to predict mask yield with $0.08\% - 6.44\%$ average RMSE across a range of defect density for four critical layers (polysilicon, active, contact and metal1).

TABLE II

VALIDATION OF CRITICAL DENSITY METHOD. MASK YIELD RMSE IS AVG.RMSE BETWEEN THE MASK YIELD ESTIMATE OF MONTE CARLO AND PROPOSED METHOD ACROSS THE DEFECT RANGE. RUNTIME IS TOTAL WALL TIME REQUIRED TO COMPUTE MASK YIELD FOR THE DEFECT RANGE.

Design	Layer	Number of shape edges	Layout density	Monte Carlo method Runtime (sec.)	Critical density method		
					Critical density	Mask yield RMSE	Runtime (sec.)
s349-syn32nm Utilization 90%	POLY	4084	0.16	10742	0.14	4.15%	19
	ACT	2384	0.32	14725	0.04	4.67%	16
	CO	20132	0.03	57432	0.03	0.32%	62
	M1	9432	0.22	48382	0.08	2.84%	84
s1423-syn32nm Utilization 90%	POLY	20672	0.16	66651	0.14	4.24%	86
	ACT	11348	0.33	24895	0.04	4.54%	79
	CO	101856	0.03	239572	0.03	0.50%	349
	M1	47554	0.22	261816	0.08	1.98%	465
s1196-syn32nm Utilization 90%	POLY	11788	0.16	28201	0.14	4.28%	47
	ACT	5800	0.29	23522	0.03	3.40%	39
	CO	60448	0.03	253287	0.03	0.54%	192
	M1	26128	0.19	198613	0.07	2.91%	222
s1196-syn32nm-u70 Utilization 70%	POLY	11788	0.12	34597	0.10	6.44%	47
	ACT	6176	0.23	12797	0.03	0.94%	41
	CO	62336	0.03	255483	0.03	0.08%	233
	M1	26502	0.16	208513	0.06	4.15%	227
Cortex M0 Utilization 90%	POLY	333748	0.15	NA	0.13	NA	858
	ACT	178396	0.29	NA	0.03	NA	999
	CO	1746968	0.03	NA	0.03	NA	4743
	M1	767380	0.19	NA	0.07	NA	5852

The methodology for estimating critical density shows that mask yield is a strong function of the autocorrelation of the layout. Our analysis indicates that irregular 2D layouts have better mask yield for the same layout density, which is contrary to most manufacturing processes that demand layout regularity. By using dummy features to make irregular layouts regular with respect to printability, this problem can be addressed since defects on dummy features do not matter.

Fast estimation of critical density enabled by our method can allow us to develop techniques to improve the mask yield of EUV layouts. Our preliminary experiments to improve critical density by iteratively adjusting the whitespace after placement suggests that $3\% - 7\%$ improvement in mask yield is possible without any area penalty. Since we used a random search based whitespace optimization for each row independently. the method is too slow to be practically useful. In the future, we plan to develop a scalable layout optimization methodology to improve the robustness of EUV layouts. Our future work also includes further enhancing the critical density model to account for other defect avoidance strategies such as pattern rotation or floorplanning, and dealing with non-uniform spatial distribution of defects (if defect data necessitate so).

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