A Framework for Exploring the Interaction Between Design Rules and Overlay Control

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ABSTRACT

Overlay control is becoming increasingly more important with the scaling of technology. It has become even more critical and more challenging with the move toward multiple-patterning lithography, where overlay translates into CD variability. Design rules and overlay have strong interaction and can have a considerable impact on the design area, yield, and performance. This paper offers a framework to study this interaction and evaluate the overall design impact of rules, overlay characteristics, and overlay control options. The framework can also be used for designing informed, design-aware overlay metrology and control strategies. In this work, The framework was used to explore the design impact of LELE double-patterning rules and poly-line end extension rule defined between poly and active layer for different overlay characteristics (i.e., within-field vs. field-to-field overlay) and different overlay models at the 14nm node. Interesting conclusions can be drawn from our results. For example, one result shows that increasing the minimum mask-overlap length by 1nm would allow the use of a third-order wafer/sixth-order field-level overlay model instead of a sixth-order wafer/sixth-order field-level model with negligible impact on design.

1. INTRODUCTION

Overlay is the positional accuracy with which a pattern is formed on top of an existing pattern on the wafer [1]. As technology scaling continues, overlay control is becoming more important than ever to allow smaller and smaller feature sizes. Moreover, the introduction of multiple-patterning (MP) lithography, where overlay effectively translates into CD variability [2, 3], has made overlay control even more critical and more challenging. Meeting the requirements for overlay control is believed to be one of the biggest challenges for deploying MP technology [4].

Overlay has been traditionally modeled using a linear model with major overlay components of translation, magnification, and rotation in the wafer and field coordinate systems [5, 6]. This linear model required a simple 2-point alignment. In recent years, the industry has moved toward high-order overlay modeling and more sophisticated alignment strategies, which requires more overlay sampling and excessive alignment [7–11]. For example, the work in [11] suggests high-order process control by overlay control with one model per lot or one model for every wafer; the work in [7] proposes high-order wafer alignment, while the work in [9] proposes exposure tool characterization using off-line overlay sampling. These improvements in overlay control are capable of reducing overlay errors considerably (by up to 30% [7, 9]) when a high-order overlay model is used. On the downside, high-order modeling of overlay requires more advanced exposure scanners, more alignment measurements, and excessive off-line overlay metrology. Hence, the overlay improvement of high-order modeling comes at a huge cost in tool migration and diminished throughput capability due to the additional measuring time.

Design rules that define interactions between different layers (e.g., metal overhang on via rule) or different mask-layouts of the same layer (e.g., mask overlap) effectively serve as guard band for overlay errors. For defining these rules during process development, a prediction of the yield loss due to overlay is needed. If overlay is characterized entirely as a field-to-field error, then the probability of survival (POS) for the die is equal to the POS of the most overlay-critical spot in the layout, say k. On the other extreme, if overlay is characterized entirely as a random within-field variation, then POS

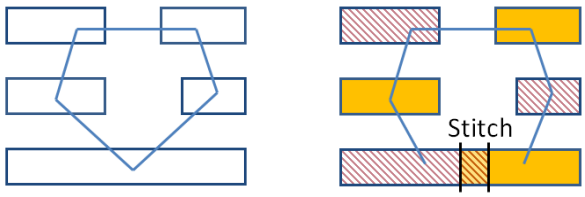
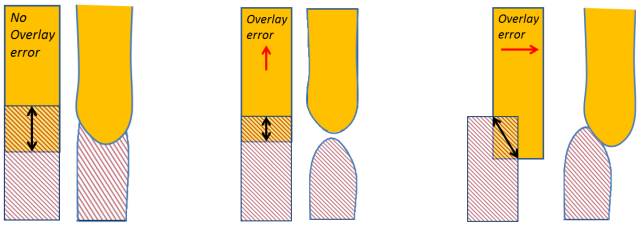


Figure 1. Example of a DP-problematic layout pattern with an odd cycle in its conflict graph (a) that was broken by introducing a stitch (b).

of the die is k^n, where n is the total number of critical spots in the design. Hence, depending on the overlay characteristics, rules can either be grown to suppress yield loss or shrank to reduce the layout area.

In this paper, we propose a general framework for exploring the interaction between design rules, overlay characteristics, and overlay-modeling options. We develop a model for yield loss from overlay that considers overlay characteristics including the residue after overlay correction and the breakdown between field-to-field and within-field overlay. The proposed framework is the first of its kind and it can be *applied during process development to better define overlay-related design rules* and *to project the overlay requirement of the process*. For demonstration purposes, the framework was used in this work to explore DP and overlay-related rules for the M1 layer as well as the polysilicon line-end extension over active rule. The framework is more general, however, and can be used to explore other inter-layer overlay rules, for different MP technologies, and at other layers.

The remaining paper is organized as follows. A background on the rules studied in this work and their interaction with overlay is given in Section 2. The proposed model for overlay-induced yield loss is described next in Section 3. Our methodology for evaluating the design impact of rules is presented in Section 4 and our findings when exploring overlay-related rules and different types of overlay models are reported in Section 5. Finally, Section 6 concludes the paper and highlights the directions of our future work.



(a) (b) (c)

Figure 2. Example of a stitch (drawn and on-wafer) in a vertical line (a), a possible failure with overlay error in Y direction that may occur after line-end pullback (b), and a possible failure with overlay error in X direction due to narrowing (c).

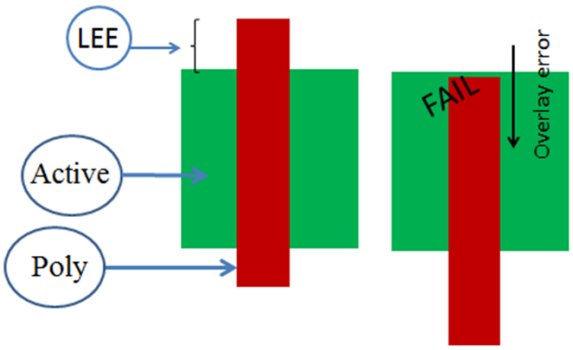


Figure 3. Poly line-end extension rule and failure criteria. The assumed process is one that does not define poly line-ends with a separate cut-exposure.

2. DESIGN RULES AND OVERLAY INTERACTION

In this paper, we focus on DP-related design rules, namely the mask-overlap length rule and the minimum line-width and spacing design rules, and poly line-end extension rule and their interaction with overlay.

The overlap-length rule is triggered whenever a stitch is introduced between the different mask layouts of the same layer. Although stitches may be a cause for yield loss, stitching is needed to conform many problematic layout patterns to DP without the need for layout modification (by breaking odd cycles in the conflict graph as in the example of Figure 1).

One of the main reasons for yield loss associated with stitches is overlay errors between the first and second exposures in DP. Therefore, the minimum overlap-length rule – a.k.a. overlap margin – has a direct impact on yield. Consider for example a stitch in the center of a vertical line as shown in Figure 2. An overlay in the Y direction may result in an insufficient mask overlap and cause an

open defect after line-end pullback; an overlay in the X direction may cause the wire to become too narrow at the stitch leading to failure. In addition, the overlap-length rule affects the DP-compatibility of the layout. The larger the overlap length is, the lesser candidate-stitch locations the layout will have. Hence, while a large and conservative overlap-length rule is likely to inhibit most yield loss of stitches caused by overlay, such overlap length may result in excessive re-design efforts and area overhead to ensure the layout conforms to DP. Another design rule that may affect the yield loss of stitches due to overlay (in x direction for the example in Figure 2) is the line-width rule. Clearly, failure from narrowing for initially narrow lines is more severe than such failure in wide lines.

The minimum line-spacing design rule impacts the delay variation of wires caused by overlay errors between the two exposures of DP [12–15]. Since overlay translates directly into line-spacing variation (with a positive dual-line process), the coupling capacitance between neighboring wires on different exposures will be affected by both overlay and the minimum line-spacing rule. The line-spacing rule has also a direct impact on the layout area. While a large line-spacing rule may confine the wire-delay variation, such spacing rule is likely to induce an area overhead.

Poly line-end extension over active rule (LEE) is subject to failure due to overlay error between the polysilicon and the active layer. Consider for example an overlay instance shown in Figure 3. An overlay error in the Y direction may lead to a low resistance path between source and drain of the transistor after line-end pullback*. Therefore, LEE has direct impact on yield since a larger poly line-end extension is likely to inhibit most yield loss caused by overlay. In addition, poly line-end extension rule also affects the design area. The larger the extension rule value is, greater is the amount of folding in poly gates which will result in a larger design area. Hence there is any interesting trade-off between yield and area(in case of LEE) or designer effort(in case of min. overlap length)

*Instead of simple geometric line-end failure model, a more complex electrical failure model [16] can be used as well

3. OVERLAY AND YIELD MODELING

The yield from overlay, $Y_{overlay}$, is equal to the probability of survival (POS) from the overlay error remaining after any overlay correction and referred to as residue[†]. Overlay-residue vector components in x and y directions are typically described by a normal distribution with zero mean and process-specific 3σ estimate. Therefore, given the fraction, p, of the overlay-residue variance breakdown between field-to-field and within-field components, the probability distribution of each type of overlay error can be calculated as follows:

$$f_{field-to-field} = \frac{1}{\sigma\sqrt{2\pi p}} e^{\frac{-u^2}{2p\sigma^2}},$$
$$f_{within-field} = \frac{1}{\sigma\sqrt{2\pi(1-p)}} e^{\frac{-v^2}{2(1-p)\sigma^2}}. \quad (1)$$

The probability for each type of overlay error to have a value between a and b is then given by

$$P_{field-to-field} = \frac{1}{\sigma\sqrt{2\pi p}} \int_a^b e^{\frac{-u^2}{2p\sigma^2}} \, \mathrm{d}u,$$
$$P_{within-field} = \frac{1}{\sigma\sqrt{2\pi(1-p)}} \int_a^b e^{\frac{-v^2}{2(1-p)\sigma^2}} \, \mathrm{d}v. \quad (2)$$

We make the assumption that overlay residue coming from *field-to-field sources* (i.e., wafer-level) is identical at all features of the same layer in the design. The overlay residue coming from *within-field sources*, however, can be different at features of the same die.

We model overlay residue (within-field and field-to-field) as partly systematic and partly random.

3.1 Yield model with purely random overlay residue

The random part of the overlay residue comes from un-modeled overlay components as well as imperfections in the correction process. In our yield model, the random component of the within-field

[†]Coupled with the lithographic line-end pullback, which we model as an offset of fixed value.

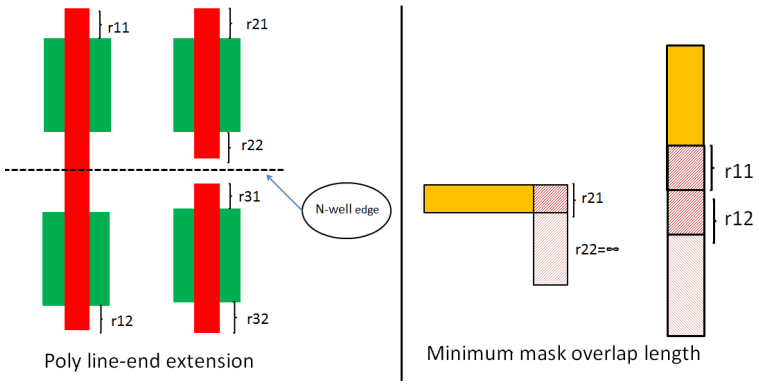


Figure 4. Example of various overlay instances scenarios for poly line-end extension and minimum mask overlap length

overlay residue is assumed to be independent from one feature to another across the design while field-to-field overlay residue is assumed to be fully correlated for all the features in the design. Hence, when the overlay residue is entirely random, the die yield caused by overlay in one direction is equivalent to the probability of all features – say n – in the design surviving such overlay error and it is calculated as follows:

single instance:

$$POS_{within-field} = \frac{1}{\sigma\sqrt{2\pi(1-p)}} \int_{-r_{12}}^{r_{11}} e^{\frac{-v^2}{2(1-p)\sigma^2}} \, \mathrm{d}v; \tag{3}$$

where r_{11} and r_{12} are the extension rule values for the overlap instance (e.g. Figure 4)

all instances n in the design:

$$POS_{within-field} = \prod_{i=1}^{n} \left[\frac{1}{\sigma\sqrt{2(1-p)\pi}} \int_{-r_{i2}}^{r_{i1}} e^{\frac{-v^2}{2(1-p)\sigma^2}} \, \mathrm{d}v \right]; \tag{4}$$

Now taking into account the wafer-level random component, say u, Die yield is given by

$$Y_{x|y} = \frac{1}{\sigma\sqrt{2p\pi}} \int_{u_{min}}^{r_{max}} \prod_{i=1}^{n} \left[\int_{-r_{i1}-u}^{r_{i2}-u} \frac{e^{\frac{-v^2}{2(1-p)\sigma^2}}}{\sigma\sqrt{2(1-p)\pi}} \mathrm{d}v \right] e^{\frac{-u^2}{2p\sigma^2}} \, \mathrm{d}u, \tag{5}$$

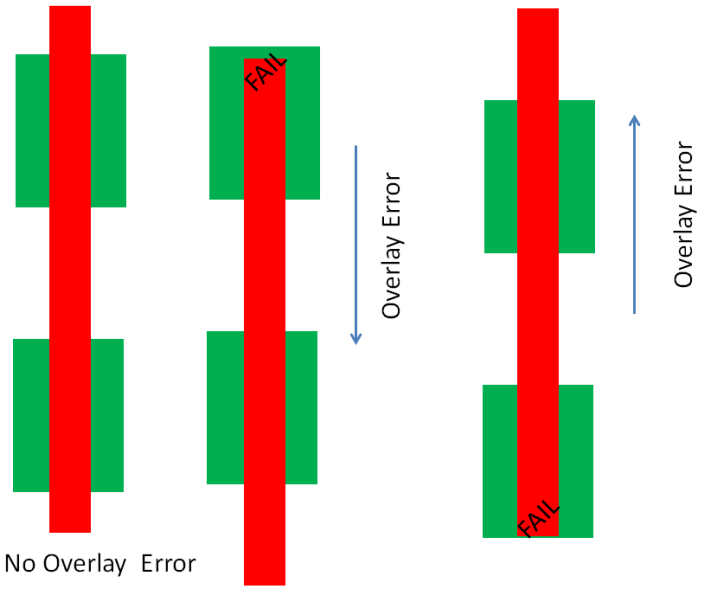


Figure 5. Example of overlay instance scenarios for which failure can occur because of overlay error in both direction

where r_{max} is the value of the maximum of all given extension rule in the design. For yield calculation purpose, maximum value of wafer-level random error u is taken as r_{max} since any overlay error beyond this limit will cause all features to fail and hence yield will be zero. Minimum value of u , say u_{min}, can either be -r_{max}, when overlay error causes failure in both direction (for e.g. +/- y direction in Figure 5) or $-\infty$, when the overlay in a particular direction effectively increases the overlap at the feature (for e.g. Figure 6(c)). r_{i1} and r_{i2} represents the values of the i^{th} instance of layer-overlap in the design (e.g. Figure 4).

3.2 Yield model in presence of systematic overlay residue

The systematic part of the overlay residue comes from un-corrected high-order overlay components (up to the sixth-order components in our experiments). The reason for not correcting for those high-order terms is because scanner tools have limited correction capability (e.g., previous-generation tools could not correct terms beyond the third order) and sophisticated alignment and overlay measurement strategies needed for high-order terms correction reduces the manufacturing throughput [8]. For yield computation, we divide the design into grids (see Figure 7). While we assume the field-to-field system-

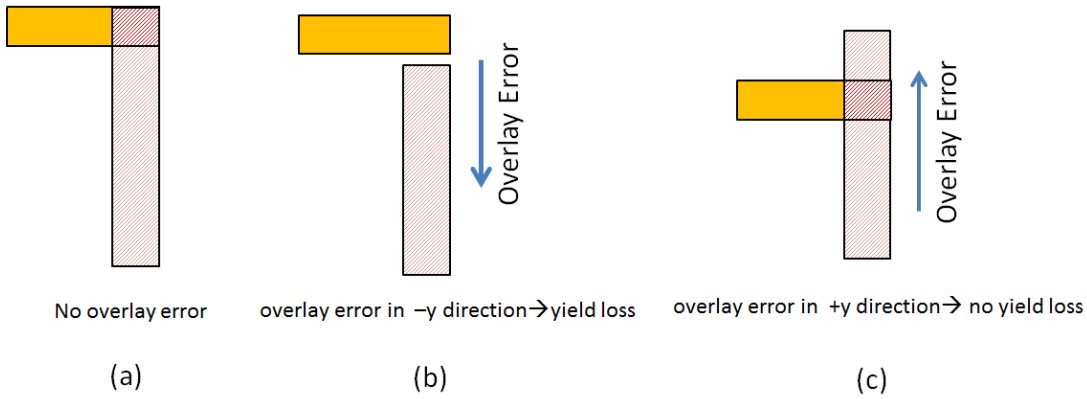


Figure 6. Example of an overlay instance causing failure only in one direction (a) stitch in a L-shaped wire segment (b) for no failure, overlay error should be less than mask overlap length in the given direction (c)no failure in this direction for any value of overlay error

atic overlay residue is identical at all features in the field, we assume the within-field systematic overlay residue is identical for features of the same grid only but different from one grid to another. Therefore, the total systematic overlay residue at an overlap-instance is the sum of the systematic within-field overlay residue in the grid containing the instance and the systematic field-to-field overlay residue of the field containing the instance. Unmodeled overlay error is assumed to be purely random. This random residue is further broken down into wafer-level component and field-level component. Therefore, given the fraction, p, of the random overlay-residue variance (σ^2) breakdown between field-to-field and within-field and systematic overlay residue as described earlier , the probability of survival from within-field overlay for a single instance, all instances in a grid, and the entire die is as follows:

single instance with systematic overlay s:

$$POS_{within-field} = \frac{1}{\sigma\sqrt{2\pi(1-p)}} \int_{-r_{12}-s}^{r_{11}-s} e^{\frac{-v^2}{2(1-p)\sigma^2}} \, \mathrm{d}v; \tag{6}$$

where r_{11} and r_{12} are shown in Figure 4

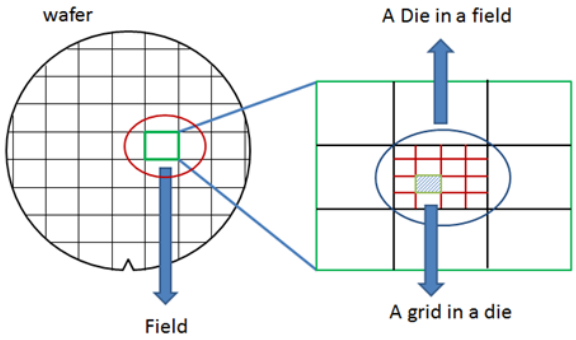


Figure 7. Pictorial representation of wafer, exposure fields, dies and the grid structure on each die.

all instances (n/g) of same grid of design with g grids:

$$POS_{within-field} = \prod_{j=1}^{n/g} \left[\frac{1}{\sigma\sqrt{2(1-p)\pi}} \int_{-r_{j2}-s}^{r_{j1}-s} e^{\frac{-v^2}{2(1-p)\sigma^2}} \, \mathrm{d}v \right]; \tag{7}$$

all instances in the die:

$$POS_{within-field} = \prod_{i=1}^{g} \prod_{j=1}^{n/g} \left[\frac{1}{\sigma\sqrt{2\pi(1-p)}} \int_{-r_{ij1}-s_i}^{r_{ij2}-s_i} e^{\frac{-v^2}{2(1-p)\sigma^2}} \, \mathrm{d}v. \right], \tag{8}$$

where s_i is the systematic overlay residue at the center of the i^{th} grid, which includes field-to-field and within-field sources. A model to estimate s_i will be presented in the next section.

Now taking into account the wafer-level random component,say u, Die yield is given by

$$Y_{x|y} = \frac{1}{\sigma\sqrt{2\pi p}} \int_{u_{min}}^{r_{max}+s_{max}} \prod_{i=1}^{g} \prod_{j=1}^{n/g} \left[\int_{-r_{ij2}-u-s_i}^{r_{ij1}-u-s_i} \left(\frac{e^{\frac{-v^2}{2(1-p)\sigma^2}}}{\sigma\sqrt{2\pi(1-p)}} \mathrm{d}v \right) \right] e^{\frac{-u^2}{2p\sigma^2}} \mathrm{d}u, \tag{9}$$

where r_{ij1} and r_{ij2} are the values of the j^{th} overlay instance in the i^{th} grid, u is the random component of the field-to-field overlay residue and s_{max} is the maximum systematic overlay error in the die.

Table 1. Summary of all assumptions made in the derivation of the yield model of Equation 9.

Overlay Component	**Assumption**
Random field-to-field	Identical for all feature within the same field
Systematic field-to-field	Identical for all feature in the same field
Random within-field	Independent for all feature in the same field
Systematic within-field	Identical for all feature within the same grid

The maximum value of u is chosen to be (r_{max}+s_{max}) because beyond this limits all features will definitely fail and POS will be zero. The minimum value of u, say u_{min}, can either be $-(s_{max}+r_{max})$ when overlay error causes failure in both direction or $-\infty$, when the overlay in particular direction effectively increases the overlap at the feature. Table 1 summarizes all the assumptions made in the derivation of the yield model of Equation 9.

Finally, the overall yield from overlay in any direction is approximated as the product of the yield in the x and y directions[‡]:

$$(Y)_{overlay} = (Y)_x \times (Y)_y. \tag{10}$$

3.3 Modeling the systematic overlay residue

In this section, we describe our method for estimating the systematic overlay residue at the center of each grid (s_i in Equation 9).

Systematic overlay error is typically described using a polynomial model function of wafer and field levels coordinates as in [17]. When the maximum polynomial order of the model is m but correction is performed for up to the k^{th} order only, then the polynomial model can be used to describe the uncorrected systematic overlay error s_x in x direction and s_y in y direction as follows:

[‡]This equation slightly underestimates the yield loss as, in reality, yield loss from overlay is defined by the area of the overlap region, which is influenced by overlay in both x and y directions.

Table 2. σ^2 values in nm^2 for second to sixth polynomial order of field-to-field and within-field overlay sources using overlay characterization data reported in [8].

Order	**Field-to-field (X)**	**Within-field (X)**	**Field-to-field (Y)**	**Within-field (Y)**
2^{nd},3^{rd}	$0.14nm^2$	$0.17nm^2$	$0.22nm^2$	$0.055nm^2$
4^{th},5^{th}, 6^{th}	$0.045nm^2$	$0.028nm^2$	$0.037nm^2$	$0.037nm^2$
Random	$0.07nm^2$	$0.07nm^2$	$0.028nm^2$	$0.028nm^2$

$$s_x = \sum_{q=k+1}^{m} \sum_{t=0}^{q} a_{qt} * x^t * y^{q-t} + \sum_{q=k+1}^{m} \sum_{t=0}^{q} b_{qt} * X^t * Y^{q-t} \tag{11}$$
$$s_y = \sum_{q=k+1}^{m} \sum_{t=0}^{q} c_{qt} * x^t * y^{q-t} + \sum_{q=k+1}^{m} \sum_{t=0}^{q} d_{qt} * X^t * Y^{q-t}$$

where x, y are the field level coordinates and X, Y are the wafer level coordinates. a and c are the coefficients for field-level and b and d are the coefficients for wafer-level terms.

The coefficients of the model of Equation 11 can be estimated from overlay measurement data. For our experiments, we estimate these coefficients as follows. We use overlay variance values for each polynomial order reported in [8], where a source of variance analysis has been conducted to characterize overlay error at 32nm node up to the sixth order wafer and sixth order field components. Since our experiments were performed for the 14nm node, we scaled the variances by a factor of 2 to account for possible improvements of scanner tools correction accuracy. We also assume that the source of variance coming from the random component is split equally between field-to-field and within-field overlay sources. Table 2 shows the σ^2 values used in this work for each order. To simplify the estimation of the model's coefficients using variance values, coefficients for all components of a given order are assumed to be same (i.e., for a given q, all a_{qt}, b_{qt}, c_{qt} and d_{qt} coefficients of Equation 11 are the same). Using the coordinates at a number of points in the wafer and field, the coefficient values of each polynomial order are then inferred from Equation 11 and the estimated

Table 3. Coefficients for the systematic overlay residue model of Equation 11 using a field size of 33x26mm and assuming 63 fields per wafer.

Within-field		**Field-to-field**	
a_{20}, a_{21}, a_{22}	0.5203	b_{20}, b_{21}, b_{22}	0.0090
$a_{30}, a_{31}, a_{32}, a_{33}$	0.2681	$b_{30}, b_{31}, b_{32}, b_{33}$	4.8183×10^{-4}
$a_{40}, a_{41}, a_{42}, a_{43}, a_{44}$	0.0811	$b_{40}, b_{41}, b_{42}, b_{43}, b_{44}$	3.4968×10^{-5}
$a_{50}, a_{51}, a_{52}, a_{53}, a_{54}, a_{55}$	0.0491	$b_{50}, b_{51}, b_{52}, b_{53}, b_{54}, b_{55}$	2.272×10^{-6}
$a_{60}, a_{61}, a_{62}, a_{63}, a_{64}, a_{65}, a_{66}$	0.0338	$b_{60}, b_{61}, b_{62}, b_{63}, b_{64}, b_{65}, b_{66}$	2.592×10^{-7}
c_{20}, c_{21}, c_{22}	0.3025	d_{20}, d_{21}, d_{22}	0.0114
$c_{30}, c_{31}, c_{32}, c_{33}$	0.1543	$d_{30}, d_{31}, d_{32}, d_{33}$	6.0713×10^{-4}
$c_{40}, c_{41}, c_{42}, c_{43}, c_{44}$	0.0933	$d_{40}, d_{41}, d_{42}, d_{43}, d_{44}$	3.1309×10^{-5}
$c_{50}, c_{51}, c_{52}, c_{53}, c_{54}, c_{55}$	0.0565	$d_{50}, d_{51}, d_{52}, d_{53}, d_{54}, d_{55}$	2.0141×10^{-6}
$c_{60}, c_{61}, c_{62}, c_{63}, c_{64}, c_{65}, c_{66}$	0.0389	$d_{60}, d_{61}, d_{62}, d_{63}, d_{64}, d_{65}, d_{66}$	2.2976×10^{-7}

variance values. For example, the coefficient of the within-field second polynomial order, a_2, can be calculated as follows:

$$s_x(2nd\ order\ within-field) = a_2 * (x^2 + y^2 + xy) \tag{12}$$
$$a_2 = \frac{\sigma_{2^{nd}order field}}{\sigma(x^2 + xy + y^2)}.$$

Table 3 shows all coefficient values that we use in our experiments.

4. EVALUATION OF RULES IMPACT ON DESIGN

This section presents the methods we used for evaluating the design impact of overlay-related rules.

4.1 Evaluation of Design Area

Our evaluation for the design area associated with poly line-end extension rule is achieved using the Design Rules Evaluator (UCLA_DRE[§]) from [18]. To evaluate area, DRE essentially creates a virtual standard-cell layouts from a set of DRs and transistor-level netlists of standard-cells. Using estimated

[§]UCLA_DRE is available for public use and can be downloaded at nanocad.ee.ucla.edu/Main/DownloadForm

area of the virtual layouts as well as instance-counts of cells in the design, the total cell-area in the design is evaluated.

4.2 Evaluation of DP-Compatibility

A layout is said to be DP-compatible, if its features can be assigned to the first and second masks without any spacing violations in each mask-layout. Hence, we choose the number of spacing violations as our metric for DP-compatibility. We use the mask-assignment algorithm of [19], which guarantees to a mask-assignment solution if one exists. To further reduce the number of spacing violations in DP-incompatible layouts, we modify the algorithm to flip the mask-assignment of violating features if the flipping reduces the number of violations.

4.3 Evaluation of Overlay-Induced Delay Variation

We use the method described in [12] to evaluate the electrical variation of wires formed with DP. In essence, the method consists modeling the wire resistance and capacitance, which are the main elements of wire delay, as a function of overlay and its different components. Since the method in [12] assumes a linear overlay model, we limit our experiments on the minimum line-spacing rules to the case of overlay control with a linear model.

5. EXPERIMENTAL RESULTS

In this section, we explore DP related design rules and poly line-end extension rule and their interaction with overlay at the 14nm technology node.

5.1 Testing setup

Our experiments were performed using AE18 design from [20], synthesized using Nangate Open Cell-Library [21], and FreePDK open-source process [22]. Since the PDK and standard cell-library are for a 45nm process, all rules and layouts were scaled by $2\times\sqrt{2}$ to run the experiments for the 14nm node

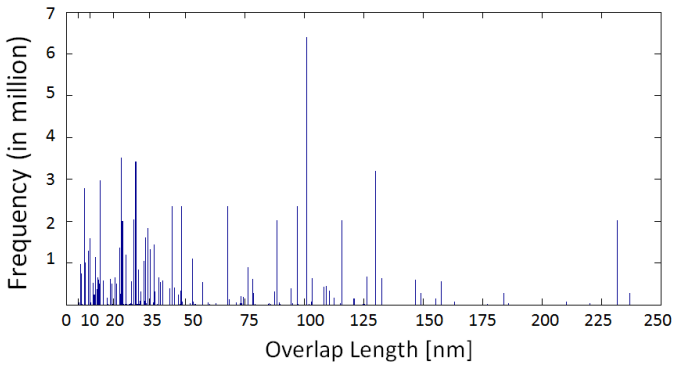


Figure 8. Histogram of overlap-length values in the design.

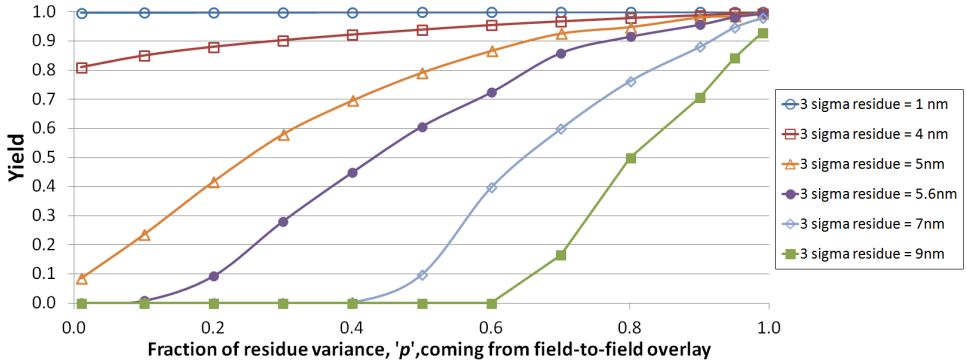


Figure 9. Plots showing the effects of the breakdown of overlay among field-to-field and within-field overlay components for different overlay-residue values.

(M1 half-pitch becomes 23nm). In all experiments, we assume a line-end pullback of 5nm. We use a field size of $33 \times 26mm$ and a design grid size for yield computation of $2.5 \times 2.5mm$.

Since the area of the benchmark design is relatively small (10K-cell instances), we normalize the yield results to a $100mm^2$ die area to have a realistic number of structures that are susceptible to yield loss (e.g, number of stitches in our experiments). We determine for the base case in each experiment the number of design copies that can fit in $10 \times 10mm$ chip size and find the corresponding number of stitches as well as the overlap length and direction of stitches in the design[¶]. Figure 8 depicts a histogram of overlap-length values for all stitches in the design.

[¶]Note that, for corner stitches, we assume that half are in vertical lines and the other half are in horizontal lines to estimate the yield loss for the open-circuit failure shown in Figure 2(b). Layout context effects for more accurate modeling is part of ongoing work.

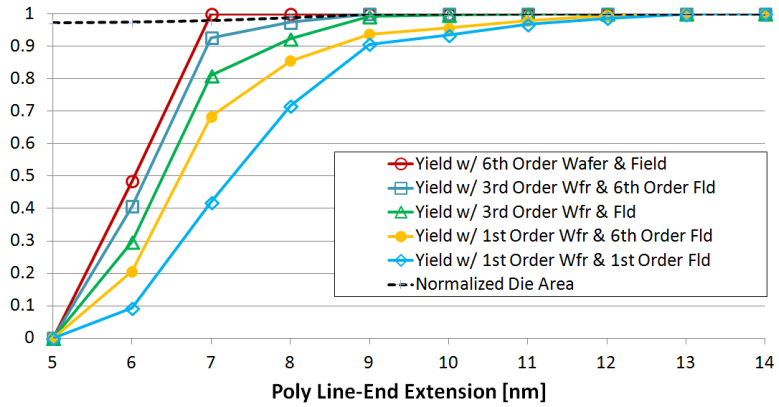


Figure 10. Plots showing the interaction between the polysilicon line-end extension rule and overlay control and their impact on yield and die area.

5.2 Projecting the overlay capability of the process

In the first experiment, the framework is used to analyze the yield loss for various values of variance of unmodeled residue and breakdown p of the residue between field-to-field and within-field components. This experiment has been done for Poly line-end extension rule value of 13nm and for first order wafer/first order field correction model. Figure 9 plots the yield of LEE for different cases. The results show that the larger the fraction of within-field overlay component, the larger the yield loss. The plots also identify the value of the residue for which a close to 100% yield can be achieved for a given overlay breakdown between field-to-field and within-field components. Such result can project the overlay capability of the process and serve as early hint for design-rules development.

5.3 Poly Line-end extension rule

The framework was also used to evaluate poly line-end extension rule (LEE) . Figure 10 shows yield and design area curves as minimum poly line-end extension rule is varied for various overlay control options. Impressively, increasing the rule value by just a few nanometer can allow the use of less complex overlay control while keeping yield and die area virtually unaffected. For example, increasing the rule from 8nm to 9nm would allow the use of third-order wafer and field-level model instead of sixth-order wafer and field-level model with negligible impact on area and yield (less than 1% area increase while yield drops from 100% to 99.3%). This can have important implications such

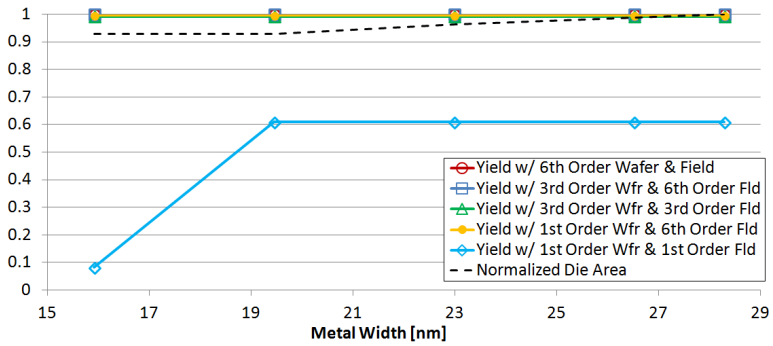


Figure 11. Plots showing the interaction between the minimum line-width rule and overlay control and their impact on yield and layout area of the design with minimum overlap-length rule of 14nm.

as increased throughput and extending the lifespan of current scanner tools that are not capable of high-order overlay correction.

5.4 Interaction between DP-related rules and overlay control

We also use the framework to study the effects of DP rules on stitch failure and the area and DP-compatibility of the design. In one experiment, we vary the line-width by few nanometers from the nominal value at 23nm and report the yield loss and the normalized design area for the different overlay-modeling options. The results, depicted in Figure 11, show that the line-width has almost no impact on stitch failure. The reason is that the nominal rule value is large enough to avoid stitches failure from overlay in the direction perpendicular to lines. Hence, stitches yield loss may be neglected when deciding on the minimum line-width rule. It can also be clearly seen from Figure 11 that the first-order wafer/first-order field-level overlay model, i.e., the linear model, is insufficient for controlling overlay at the 14nm node.

In another experiment, we vary the minimum mask-overlap length and report the yield loss and number of DP-spacing violations in the design for the different overlay-modeling options. The results, depicted in Figure 12[‖], show the strong interaction between the rule value and overlay-control options as well as the overall impact on yield and DP-compatibility. Interestingly, few nanometer changes

[‖]The number of DP-spacing violations are normalized with respect to the case with the largest number and DP mask-assignment of the layouts was performed using a minimum same-color spacing of 1.5× the half-pitch.

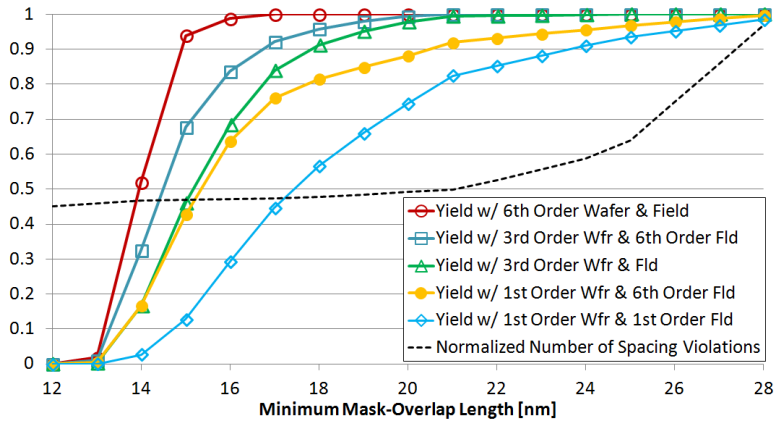


Figure 12. Plots showing the interaction between the overlap-length rule and overlay control and their impact on yield and DP-compatibility of the design at the nominal line-width of 23nm.

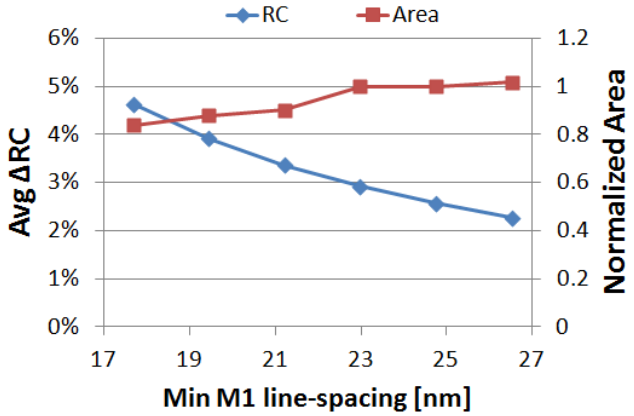


Figure 13. Plot for the average ΔRC and the normalized design area for different values of the minimum line-spacing rule.

in the rule value may allow the use of a less stringent overlay control without significant impact on DP-compatibility. For example, increasing the minimum mask-overlap length from 19nm to 20nm would allow the use of third-order wafer/sixth-order field-level overlay model instead of sixth-order wafer/sixth-order field-level model while yield remains at 100% and DP-spacing violations increase by just 1%.

Our last experiment is about studying the effects of the line-spacing rule on wire-delay variation and layout area. We vary the line-spacing rule from the nominal value at 23nm by few nanometers. The results, given in Figure 13**, indicates that the impact of this rule on the average RC variation is minor, while its impact on area is considerable. Hence, tweaking the line-spacing rule with the

**Note that there is always some electrical variation due to overlay errors with any realistic line-spacing rule.

intention of reducing the electrical variation is ineffective.

6. CONCLUSIONS AND FUTURE WORKS

We propose a general framework to explore the interactions between design rules, overlay characteristics, and overlay modeling options. Yield loss due to overlay is modeled as a function of design-rule values and the overlay characteristics. The proposed framework is the first of its kind and it can be used during process development to better define overlay-related design rules and project overlay requirements for the process. For demonstration purposes, the framework was used in this work to explore DP and overlay-related rules for the M1 layer as well as the polysilicon line-end extension over active rule at the 14nm node. Important conclusions could be drawn from our experimental results. One result shows that increasing the minimum mask-overlap length by 1nm would allow the use of a third-order wafer/sixth-order field-level overlay model instead of a sixth-order wafer/sixth-order field-level model with negligible impact on design. Another result shows that the minimum line-width and spacing rules have an insignificant impact yield and electrical variation. Although our studies were performed for a few rules at the M1 and poly layers, the framework is more general and can be used to explore other inter-layer overlay rules, for different MP technologies, and for different layers. In future work, we will extend our yield and design-impact analysis to a chip-level analysis across all layers in the design and explore other overlay-related rules especially rules related to cut-masks.

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