On Electrical Modeling of Imperfect Diffusion Patterning

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***Abstract*—Imperfect lithographic patterning leads to non-rectangular polysilicon and diffusion layers. Though electrical modeling of polysilicon rounding has received much attention, same is not true for diffusion. In this work, we propose the first *physically derived* electrical model for diffusion rounding. We show that channel length, effective device width and V_{th} of the device are affected. The model shows that effect of rounding is not symmetric with respect to source and drain. Further, we extend the model to handle polysilicon and diffusion patterning imperfections together. The model can be calibrated using circuit simulation instead of silicon/TCAD. The average errors (as verified with TCAD simulation) of the model are 1.6% and 1.7% for TCAD and SPICE based calibration respectively. The average error for the combined poly and diffusion rounding model is 2.7%. As a simple circuit application, we show that poly-to-diffusion spacing rule can be shrunk to reduce cell area by 5% without any delay or leakage penalty.**

I. Introduction

Due to aggressive scaling in CMOS technology, critical dimension of integrated circuit has shrunk to sub-wavelength lithography regime. Even with various resolution enhancement techniques and design for manufacturability methodology, significant lithography pattern distortion is observed on polysilicon and diffusion layers [1,2].

Many studies have been carried out to model MOSFET's electrical metrics (I_{on} and I_{off}) to account for channel irregularities [3]–[14]. Most of these works attempt to model polysilicon rounding or line-edge-roughness by a number of narrower rectangular MOSFETs connected in parallel. Then, the current of sliced rectangular MOSFETs is summed to obtain effective current. With the information of effective current, the non-rectangular gate (NRG) transistor is represented by two rectangular devices with equivalent gate lengths (EGL) depending on its working state [3]–[11]. Instead of using different gate lengths for a single transistor, [12,13] replace a NRG transistor by a limited number of transistors. Alternatively, a unified transistor model card that accounts for all operation regions is proposed in [14]. A recent study reveals that active layer is increasingly distorted with the shrinking polysilicon pitch whenever several transistors with different channel widths are located close to each other [2]. For example, Fig. 1 shows poly and diffusion layers printed by state-of-art 193nm steppers (with OPC) which has significant corner rounding with radii of the order of 60nm (indicated by red circles). A recent work proposed a simple model to capture diffusion rounding effects [15]. This model is based on empirical equations that are fitted to Technology Computer-Aided Design (TCAD) simulation data. Due to the empirical nature of the model, early evaluation of diffusion rounding is not possible for new technologies or process setups. Moreover, this method only handles source side rounding but in reality, diffusion rounding can happen on both sides.

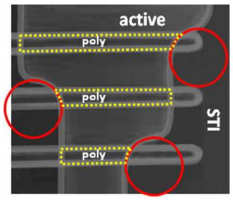

Fig. 1. Diffusion and poly layers by state-of-art 193nm steppers [2]

In this paper, we propose a MOSFET model that accounts for poly and diffusion rounding effects. The major contributions of this paper are as follows:

- We derive I_{on} and I_{off} equations for diffusion rounded device based on gradual channel approximation and charge sharing models. Unlike empirical equations in [15] our model captures the difference between source and drain sides rounding, with physical insights.
- Our model can be calibrated using circuit simulation rather than TCAD or silicon.
- A model that handles both polysilicon and diffusion patterning imperfection is proposed and verified.

The rest of this paper is organized as follows. Section II describes our modeling for diffusion rounded device and model verification. Section III shows parameter extraction using SPICE data. Section IV explains and verifies our general model that covers both diffusion and poly rounding. Circuit examples are included in section V. Finally, section VI concludes this paper.

II. Modeling a diffusion rounded MOSFET

Given a diffusion rounded MOSFET, it is convenient to model it as a trapezoidal gate device, as it introduces little mismatch with original shape and simplifies overall calculation complexity. An early study of trapezoidal MOSFET is addressed in [18] where I-V equations are derived. However, only I_{on} is discussed and the derived equation is computationally expensive.

In this work, a diffusion rounded transistor is decomposed into narrower trapezoid and rectangular transistors connected in parallel. Since trapezoidal transistor cannot be simulated

directly using BSIM [16], it is approximated by a rectangular transistor with equivalent channel width derived from first order expressions. Meanwhile, equivalent channel lengths and V_{th} of these transistors are evaluated to account for the impacts of diffusion rounding. After that, all transistors (with their respective channel, width and V_{th}) are approximated as rectangular transistors using BSIM model and simulated using SPICE to obtain total the I_{on} and I_{off} for the diffusion rounded transistor. Second order effects such as DIBL, velocity saturation, and etc, are modeled in BSIM.

Finally, based on the simulated I_{on} and I_{off}, we can find an equivalent device with L_{eff}, W_{eff} and ΔV_{th} that matches the total current and gate area (for capacitance). This method is similar to the EGL approach where 2 sets of parameters are required for delay and leakage analysis. Our model can be implemented differently to obtain a unified model for leakage and delay analysis. E.g., a multiple transistors model proposed in [12,13] can be used. Alternatively, our model can be used to generate a post-litho module that estimates ΔI for a diffusion rounded MOSFET based on geometry information and bias conditions as in [14].

The rest of this section describe our slicing strategy, the derivations for equivalent channel length, width and V_{th} and model verification.

A. Channel length

One of the key differences between trapezoidal and normal MOSFET is electrostatic potential distribution. Fig. 2 shows the electrostatic potential contours of a trapezoidal MOSFET spread from drain to source junction and curved around the edges. This shows that electrical field ($\vec{E}$) for trapezoidal gate MOSFET has vertical and horizontal components in contrast to unidirectional field for normal MOSFET. Capturing two-dimensional $\vec{E}$ is crucial as it defines the current direction and therefore channel length. As shown in Fig. 3, we approximate $\vec{E}$ in trapezoidal device according to its location in channel. I.e. $\vec{E}$ in middle section has only horizontal component while the ones in edge sections have both horizontal and vertical components. Then, we assume directions of $\vec{E}$ in edge sections change linearly from purely horizontal to parallel to channel's edge. We divide source/drain's width into a number of slices equivalently, in which the middle point from source to drain for a sliced channel is in the same direction as $\vec{E}$.

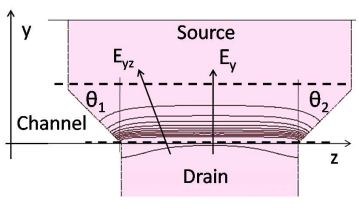

Fig. 2. Simulated potential contour on silicon surface.

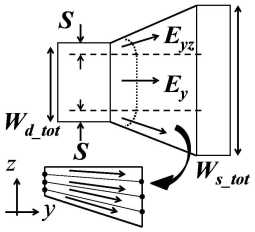

Fig. 3. Slicing approach.

In this work, we estimate the slicing location, S (border between middle and edge section) by

$$S \; \alpha \; \vec{E_z}/\vec{E_y} = \frac{f(\theta) * L_{eff}}{L_{eff-ref}}, \tag{1}$$

which models S as a ratio of vertical field to horizontal field. Based on TCAD simulation results, we found that S can be modeled as a linear function of θ, $f(\theta) = (a + b\theta) * L_{eff}/L_{eff-ref}$. [1] Parameters a and b are obtained from TCAD simulation results and their values are 8nm and 0.089nm/degree, respectively. Since horizontal field changes linearly with channel length, it is modeled by a multiplier, $L_{eff}/L_{eff-ref}$, which is the ratio of effective channel length to a reference value ($L_{eff-ref}$ = 25nm)[2]. In this work, L_{eff} of our MOSFET model is 25nm at 45nm drawn gate length. After decomposing trapezoidal channel as mentioned, diffusion rounded device is represented by transistors connected in parallel, each with its channel length, width and V_{th}.

B. Threshold voltage

For every sliced transistor, V_{th} varies due to narrow width effect (ΔV_{th-ed}) [9,16,19] and asymmetry between drain/source terminals (ΔV_{th-cs}). The effective V_{th} for a given slice is

$$V_{th-eff} = V_{th-m} + \Delta V_{th-ed} + \Delta V_{th-cs}, \tag{2}$$

where V_{th-m} is nominal V_{th} in the middle of device.

1) ΔV_{th-ed}: Due to narrow width effect, variation of V_{th} for different slices can be approximated using the model in [9], with ΔV_{th-ed}(z)=

$$\begin{cases} K_b(W-z-w) - K_a(W-z-w)^2, & W-w \le z \le W \\ K_b(z-w) - K_a(z-w)^2, & 0 \le z \le w \\ 0, & w \le z \le (W-w). \end{cases}$$

K_b and K_a are fitted parameters;w is the maximum width from both sides that experience narrow width effect; and W is device's average width[3].

2) ΔV_{th-cs}: Figure 4 shows the top view and cross section of a sliced transistor in edge section with asymmetry source and drain widths. The general threshold voltage equation for any transistor is given as follows

$$\begin{aligned} V_{th} &= V_{fb} + 2\phi_b + [\frac{Q_{Beff}}{Cox.W_{avr}L}], \\ W_{avr} &= (W_d + W_s)/2. \end{aligned} \tag{3}$$

V_{fb}, ϕ_b, Q_{Beff},Cox, W_{avr} and L are flat band voltage, built-in potential, effective bulk charge, capacitance per-unit area, average gate width and gate length, respectively. The threshold voltage deviation in short channel device can be modeled by depletion charge sharing between gate and source/drain junctions [17]. Therefore, effective bulk charge in device's channel can be modeled as $Q_{Beff} = Q_{total} - Q_{sd}$, where Q_{sd} is defined as the total charge shared by both drain and source junctions with the gate.

[1] When θ increases, increased source/drain width leads to stronger vertical field component and a larger S. Meanwhile, increased source/drain portion is further away from channel, causing the effective vertical field and S to be weakly dependent on θ.

[2] Based on our simulation results, we found that same parameters (a, b and $L_{eff-ref}$) can be used for NMOS and PMOS devices with reasonable accuracy despite of differences in dopant concentration.

[3] w,K_b and K_a can be extracted using rectangular devices as reported in [9]. The location of each slices, z is estimated by its centroid.

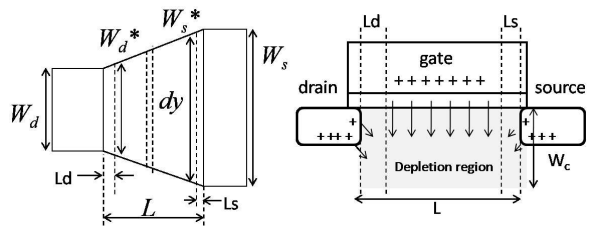

Fig. 4. Description of a sliced trapezoidal gate device.

In this paper, we assume that charge sharing region for drain and source sides are extended by L_d and L_s into channel, and depletion depth (W_c) is constant along device's channel. The total shared charge and total charge without sharing effect are therefore given by

$$\begin{aligned} Q_{sd} &= qN_a(\frac{W_c}{2})(L_dW_d + L_sW_s), \\ Q_{total} &= qN_aW_cLW_{avr}. \end{aligned} \tag{4}$$

It should be noted that the effective width for L_s and L_d region are slightly different from W_s and W_d. This error can be reduced by replacing $W_{s,d}$ with $W^*_{s,d}$ [4] For rectangular device, W_s = W_d = W^*_s = W^*_d.

$$\begin{aligned} W^*_d &= W_d + (W_s - W_d)L_d/2L, \\ W^*_s &= W_s - (W_s - W_d)L_d/2L. \end{aligned}$$

Combining (3)-(4), yield

$$\begin{aligned} V_{th} &= V_{fb} + 2\phi_b + \frac{qN_aW_c}{Cox}F \\ F &= 1 - \frac{L_dW_d + L_sW_s}{2LW_{avr}}. \end{aligned}$$

The deviation of V_{th} due to charge sharing is only a function of gate length for rectangular device. However, as soon as device's source and drain sides are different, charge sharing term F and V_{th} will change accordingly. For a sliced transistor of which the source side width changes from W_d to W_s as in Fig. 4, the threshold voltage is given as,

$$\Delta V_{th} = \frac{qN_aW_c}{2LCox}[\frac{2(L_dW_d + L_sW_s)}{W_d + W_s} - (L_d + L_s)]. \tag{5}$$

C. Equivalent width

In order to figure out its effective channel width, the I-V equations for saturation and cut-off regions are derived.

1) I_{on}: In the following derivation, gradual channel approximation [19] is used and it defines the channel width as the length of equipotential arcs. For rectangular slices, the channel width is simply its geometrical width. For transistors that have unequal width at drain and source sides, it is modeled as in Fig. 4. We define the channel width,W along channel by

$$W(y) = W_d + (W_s - W_d)y/L. \tag{6}$$

In strong inversion region, I_{on} of a MOSFET is given as [19]

$$I_D = Q_{tot}(y)v(y).$$

Since V_{th} is constant across channel width (for a slice).

[4]In this work, TCAD based calibration uses (II-B2) while SPICE (circuit simulation) based calibration uses (4). By using 4, our model can be calibrated without knowing the exact values of L_d and L_s.

$$\begin{aligned} I_D &= W(y)Q_n(y)v(y), \\ v(y) &= \mu.dV(y)/d(y). \end{aligned} \tag{7}$$

$Q_n(y)$ is the inversion charge per unit area; $v(y)$ is the velocity of carriers; and $V(y)$ is electrostatic potential, at position y along the channel. In this derivation, drift velocity (μ) is taken as a constant instead of field dependent velocity term as in [18] to give the first order result of equivalent width. This simplification leads to an analytical closed form equation. Moreover, derived equivalent width is easy to use in BSIM SPICE model with good accuracy. Based on sheet charge and gradual channel approximation,

$$Q_n(y) = Cox[V_G - V_{th} - V(y)]. \tag{8}$$

Substitute (6),(8) into (7),

$$I_D = (W_d + (W_s - W_d)\frac{y}{L})\mu Cox[V_G - V_{th} - V(y)]\frac{dV(y)}{d(y)},$$

Then we integrate from drain to source, yielding

$$\begin{aligned} \int_0^L \frac{I_D.dy}{(W_d + (W_s - W_d)y/L)} &= \int_{V_s}^{V_d} \mu Cox[V_G - V_{th} - V]dV \\ I_D &= \frac{1}{L}\frac{(W_s - W_d)}{ln(W_s/W_d)}\mu Cox[V_G - V_{th} - \frac{V_{ds}}{2}]V_{ds}. \end{aligned} \tag{9}$$

It is observed that (9) is the same as classical long channel MOSFET I-V equation except for the equivalent width term,

$$W_{eff} = \frac{(W_s - W_d)}{ln(W_s/W_d)}. \tag{10}$$

Based on this information, we can translate a trapezoidal gate device to a rectangular gate device with equivalent width given in (10) and ΔV_{th-eff}.

2) I_{off}: Throughout this paper, we assume that the leakage current is dominated by sub-threshold current. In order to figure out the equivalent width for I_{off} we start with the general form of diffusion current [19],

$$I_{off} = w(y)D\frac{dQ_{inv}}{dy}. \tag{11}$$

We integrate (11) from source to drain, yielding

$$I_{off} = \frac{1}{L}\frac{(W_s - W_d)}{ln(W_s/W_d)}D.(Q_{inv}(l) - Q_{inv}(0)). \tag{12}$$

where $Q_{inv}(.)$ is location dependent inversion charge and D is a constant which includes channel width, mobility factor and thermal voltage. Equation (12) shows that equivalent width for I_{off} is same as the one derived for I_{on} while the remaining terms are same as in the current equation for rectangular device. Through the derivation, we have shown that for a trapezoidal device, its effective channel widths are same for saturation and cut-off regions. The effective channel width is given by (10).

D. Model verification

In order to verify our model, we compare I_{on} and I_{off} of our model (simulated using SPICE) to the ones obtained from the TCAD tool [20]. In this experiment, our TCAD model is generated based on Synopsys's Sentaurus 3D 45nm reference flow and its parameters are shown in Table I.

TABLE I
TCAD MODEL PARAMETERS

Parameters	Value
Drawn gate length	45 nm
Effective channel length	25 nm
Width (NMOS)	110-300 nm
Width (PMOS)	255-500 nm
Vdd	1 V
Tox	1.5 nm
Channel doping (Nmos)	3e20 cm^{-3}
Channel doping (Pmos)	2e20 cm^{-3}
NSUB (Nmos)	2.5e18 cm^{-3}
NSUB (Pmos)	2.5e18 cm^{-3}
Junction depth	20 nm
Line-end extension	20 nm
Spacer width	30 nm
STI width	100 nm
STI depth	300 nm

TABLE II
NMOS TCAD VS MODEL RESULTS

	Drain (nm)	Source (nm)	θ (^{o})	TCAD I_{on} (uA)	Model I_{on} (uA)	Error (%)	TCAD I_{off} (nA)	Model I_{off} (nA)	Error (%)
Rectangular	155	155	0	162.09	161.32	-0.5	73.80	73.44	-0.5
	200	200	0	208.01	208.03	0.0	92.50	94.08	1.7
Source	155	181	30	173.65	170.06	-2.1	71.14	70.54	-0.8
larger	155	200	45	177.63	174.07	-2.0	68.72	69.22	0.7
1 side	155	233	60	182.69	177.51	-2.8	67.41	67.70	0.4
	200	245	45	225.06	220.77	-2.5	90.17	89.86	-0.3
Source	155	207	30	183.75	179.29	-2.3	67.76	67.98	0.3
larger	155	245	45	194.01	186.80	-3.4	63.94	65.00	1.7
2 sides	155	311	60	204.01	194.42	-4.2	62.67	62.37	-0.5
Drain	181	155	30	170.21	171.62	0.8	76.88	75.82	-1.4
larger	200	155	45	172.76	176.34	2.1	74.12	74.31	0.3
1 side	233	155	60	175.99	180.63	2.6	72.19	72.49	0.4

TABLE III
PMOS TCAD VS MODEL RESULTS

	Drain (nm)	Source (nm)	θ (^{o})	TCAD I_{on} (uA)	Model I_{on} (uA)	Error (%)	TCAD I_{off} (nA)	Model I_{off} (nA)	Error (%)
Rectangular	300	300	0	184.34	184.33	0.0	68.09	67.64	-0.7
	345	345	0	211.56	211.98	0.0	76.14	77.47	1.7
Source	300	326	30	191.64	189.08	-1.3	66.48	66.67	0.3
larger	300	345	45	194.39	190.92	-1.8	64.86	66.08	1.9
1 side	300	378	60	197.38	191.88	-2.8	64.93	65.36	0.7
	345	390	45	222.16	218.57	-1.6	76.08	76.24	0.2
Source	300	352	30	199.98	194.13	-2.9	66.45	65.76	-1.0
larger	300	390	45	204.66	197.50	-3.5	63.12	64.40	2.0
2 sides	300	456	60	210.83	199.89	-5.2	61.54	63.17	2.6
drain	326	300	30	190.13	190.37	0.1	71.18	69.57	-2.3
larger	345	300	45	192.55	192.76	0.2	69.31	68.95	-0.5
1 side	378	300	60	194.75	194.24	-0.3	68.29	68.07	-0.3

After simulating rectangular MOSFETs of different widths using TCAD, its I_{on} and I_{off} values are taken for fitting the parameters of a BSIM model card. Fig. 5 shows that our SPICE model is fitted closely to TCAD simulation results for normal rectangular MOSFETs. Then, trapezoidal MOSFETs as described in Fig. 2 and 3 are simulated using TCAD with different angles, θ. Consequently, TCAD experiment results from 30° and 45° trapezoidal devices (source diffusion rounded on one side) are used for fitting the values of L_d and L_s in (5). From the fitted parameters L_d and L_s, we estimate the I_{on} and I_{off} of other diffusion rounded devices excluding those used for fitting. After obtaining equivalent channel length, width and ΔV_{th-eff}, current of transistors are estimated, summed and compared to TCAD as shown in Table II-III.

Table II and III show that I_{off} of source side diffusion rounded device is less but I_{off} of drain side diffusion rounded device is higher (for small θ) compared to rectangular devices. The experiment results indicate that the errors between our model and TCAD simulation results are within 5.2% for all devices [5]. Based on our model, the changes in I_{off} are due to changes in V_{th} as a result of charge sharing. I.e., V_{th} increases when the device is source side rounded and the other way around for drain side rounded device. When θ is large, the effective channel length around edges increases. As a result, V_{th} on edges increases and leakage current is reduced. Since channel edges are usually more leaky compared to the inner region due to narrow width effects, such increment in V_{th} may lead to reduction in total current, even when effective channel width increases due to rounding.

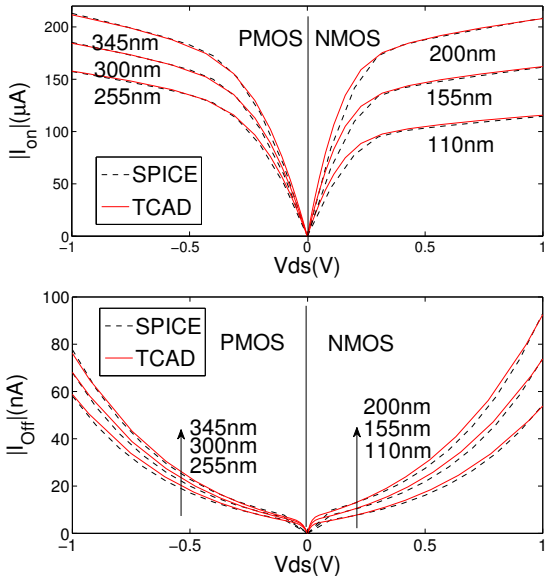

Fig. 5. TCAD vs SPICE model for rectangular devices

[5]In saturation region, channel length modulation (CLM) happens and effective L reduces. While CLM effect is modeled in BSIM the drain side width of trapezoidal gate MOSFET is not (the width for trapezoidal channel is a function of channel length). Therefore, higher I_{on} errors are observed for trapezoidal devices compared to rectangular ones. This error can be corrected by refining drain side width based on effective channel length, which is a function CLM factor and V_{ds}.

III. Parameter Extraction Using SPICE

In previous section, it is shown that given process parameters and device's geometry, I_{on} and I_{off} of our model match TCAD simulation results with high accuracy for fitted L_d and L_s. Fitting these parameters would require reference data either from simulation or silicon. The SPICE-based extraction for ΔV_{th-ed} can be done by the method proposed in [9]. In this work, we propose an approximation approach that uses only BSIM model to extract required parameters for diffusion rounding model. For a rectangular device,

$$V_{th} = V_{fb} + 2\phi_b + \frac{qN_aW_c}{Cox}(1 - \frac{L_d + L_s}{2L}).$$

The (L_d + L_s) term can be extracted from the difference of V_{th} values between two rectangular devices with different channel lengths.

$$K_1 = V_{th,L_1} - V_{th,L_2} = \frac{qN_aW_c}{2Cox}(L_d + L_s)(\frac{1}{L_2} - \frac{1}{L_1}).$$

Also, when V_{ds} is small, $L_d \approx L_s$. By comparing the V_{th} values at different V_{ds}, we can obtain another set of equation which has the desired terms, L_d and L_s :

$$K_2 = V_{th}|_{V_{ds}=1V} - V_{th}|_{V_{ds}=0V} = \frac{qN_aW_c}{Cox}(\frac{L_s - L_d}{L}).$$

Using K_1 and K_2, we can solve for L_d and L_s :

$$\begin{aligned} K_1(\frac{L_1L_2}{L1 - L2}) - \frac{K_2L}{2} &= \frac{qN_aW_c}{Cox}(L_d) \text{ and} \\ K_1(\frac{L_1L_2}{L1 - L2}) + \frac{K_2L}{2} &= \frac{qN_aW_c}{Cox}(L_s). \end{aligned} \quad (13)$$

Note that, we do not extract L_d and L_s from $\frac{qN_aW_c}{Cox}$ terms, as they can be substituted into (5) directly [6]. As mentioned earlier, parameters a, b and $L_{eff-ref}$ in (1) are insensitive to junction/channel doping. Therefore, we assume that they are technology independent and can be used for SPICE-based extraction. In Table III, we compare the accuracy of this approach to previous fitting solution as well as method in [15]. As shown in Table III, the errors for SPICE-based extraction are within 5% for all devices. The sources of errors including mismatch between SPICE model vs TCAD, our model vs TCAD and errors from extracted parameters. Also, it is shown that both extraction methods based on our model are more accurate compared to [15]. It is shown that SPICE-based extraction method introduced little additional error compared to TCAD-based extraction. Thus, we can use it for early evaluation of diffusion rounding effects without TCAD/silicon data.

IV. Combined Poly and diffusion rounding model

The modeling and slicing approaches described in section II can be applied for diffusion and poly rounded device with minor refinement in edge sections slicing. For irregular channel channel's edge, it is approximated as a trapezium for slicing as shown in Fig. 6. Note that, W'_d and W'_s are only used to determine slicing angle but not the width of sliced channel. Drain and source width of transistors (W_{d_i} and W_{s_i}) are obtained by approximating edges with straight lines that are orthogonal to the vector of channel length, $\vec{L}$.

[6]In this experiment, $\frac{qN_aW_c}{Cox}L_s$ and $\frac{qN_aW_c}{Cox}L_d$ terms are extracted at large channel width (500nm) and length (90nm) to decouple narrow width and DIBL effects.

TABLE IV
Percentage error for different calibration methods (NMOS)

	Drain (nm)	Source (nm)	TCAD extraction		SPICE extraction		Method [a] [15]	
			I_{on} (%)	I_{off} (%)	I_{on} (%)	I_{off} (%)	I_{on} (%)	I_{off} (%)
rectangular	155	155	1.7	-0.5	1.7	-0.5	NA	NA
Source	155	181	-2.1	-0.8	-2.0	-0.5	0.7	6.2
larger	155	200	-2.0	0.7	-1.9	1.1	4.0	-0.5
1 side	155	233	-2.8	0.4	-2.7	0.7	10.5	-9.2
Source	155	207	-2.3	0.3	-1.2	1.0	2.5	15.6
larger	155	245	-3.4	1.7	-3.2	2.4	7.3	6.9
2 sides	155	311	-4.2	-0.5	-4.0	0.2	18.9	-2.3
Drain	181	155	0.8	-1.4	0.8	-2.3	NA	NA
larger	200	155	2.1	0.3	2.0	-0.7	NA	NA
1 side	233	155	2.6	0.4	2.5	-0.5	NA	NA

[a]Drain-side rounding is not modeled in [15]

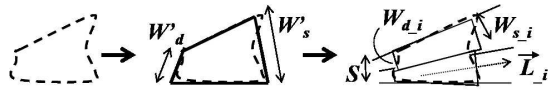

Fig. 6. Edge section slicing for poly+diffusion rounding device.

A. Model verification

To verify our model, we generate poly and diffusion rounding device on a 3D TCAD simulator [20] with process parameters given in Table I and the description of test pattern is shown in Fig. 7. These patterns include +/- 10nm gate length variation (nominal gate length = 45nm) due to poly rounding and also diffusion rounding on different edges at different values.

Based on the experiment results in Table V, we can see that I_{on} increases and I_{off} decreases when a poly rounded device has diffusion rounding [7]. These experiment results also show that when diffusion rounding happens on the edge with shorter channel length, reduction in I_{off} is more significant as expected. When diffusion rounding occurs at that edge, the effective length around there is increased. As a result, a higher reduction in I_{off} is observed. The results also show that our model is able to estimate I_{off} and I_{on} accurately. The average error is 2.7% but larger errors ($\sim$ 7%) are observed for certain devices, which stem mostly from the previously published poly-rounding model [9,11].

V. A Circuit example : Implication to design rules

With the knowledge of diffusion rounding model, we can relax design rule that limits poly-diffusion corner spacing. A case study is carried out for NOR and NAND gates with diffusion straps connected to power/ground, whereby the spacing rule is reduced by 30% (original value=50nm, shrunk value=35nm) and performance metrics are compared

[7]For brevity, only the results for NMOS source-side rounding are shown.

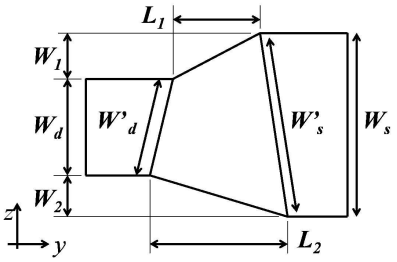

Fig. 7. Device's channel with diffusion and poly rounding.

TABLE V
TCAD VS POLY + DIFFUSION MODEL (NMOS)

	L_1 (nm)	L_2 (nm)	w_1 (nm)	w_2 (nm)	TCAD I_{on} (uA)	Model I_{on} (uA)	error (%)
rectangular	35	35	0	0	211.47	211.28	-0.0
	45	45	0	0	162.09	161.33	-0.5
	55	55	0	0	132.38	131.12	-1.0
poly rounding	55	45	0	0	146.10	145.06	-0.7
	35	45	0	0	184.39	183.97	-0.2
Diffusion and poly rounding	55	45	26	0	155.13	152.81	-1.5
	55	45	45	0	158.63	156.48	-1.4
	55	45	0	26	157.46	153.78	-2.3
	55	45	0	45	162.34	157.82	-2.8
	35	45	26	0	198.52	194.06	-2.2
	35	45	45	0	202.49	197.65	-2.4
	35	45	0	26	195.04	192.90	-1.1
	35	45	0	45	198.44	196.99	-0.7

	L_1 (nm)	L_2 (nm)	w_1 (nm)	w_2 (nm)	TCAD I_{off} (nA)	Model I_{off} (nA)	error (%)
rectangular	35	35	0	0	5763.3	5874.6	1.9
	45	45	0	0	73.80	73.44	-0.5
	55	55	0	0	2.93	2.81	-4.1
poly rounding	55	45	0	0	19.52	20.00	2.5
	35	45	0	0	1270.8	1366.7	7.5
Diffusion and poly rounding	55	45	26	0	19.640	19.93	1.5
	55	45	45	0	19.244	18.84	3.1
	55	45	0	26	18.24	17.31	-5.1
	55	45	0	45	16.596	16.14	-2.7
	35	45	26	0	1225.2	1235.7	0.9
	35	45	45	0	1154.6	1163.1	0.7
	35	45	0	26	1268.5	1363.8	7.5
	35	45	0	45	1263.2	1362.3	7.8

in Table VI[8]. The worst case corner is defined by printing diffusion layer at 100nm defocus. By relaxing the design rule, total width of both NAND and NOR gates are reduced by 30nm (5.2%) while other performance metrics are negligibly changed.

TABLE VI
DESIGN RULE ANALYSIS FOR NAND AND NOR GATES
(ALL VALUES ARE NORMALIZED)

		NAND_X1		NOR_X1	
		Original	Spacing Reduced	Original	Spacing Reduced
Delay	nominal (no defocus)	1.00	1.00	1.00	0.99
	worst (100nm defocus)	1.05	1.04	1.05	1.05
Leakage	nominal (no defocus)	1.00	1.00	1.00	1.01
	worst (100nm defocus)	0.91	0.91	0.90	0.90
area		1.00	0.95	1.00	0.95

VI. CONCLUSIONS AND FUTURE WORK

In this work, we have presented a MOSFET model to account for diffusion rounding. From our study, the effect of diffusion rounding on a device can be represented by changes in V_{th}, channel length and effective width. The accuracy of our model is verified by TCAD simulation results and average errors are 1.6% (I_{on} error=2.2%, I_{off} error=0.9%) and 1.7% (I_{on} error=2.3%, I_{off} error=1.0%) for TCAD and circuit simulation based calibrations, respectively. In this work, we extended our model to account for polysilicon and diffusion rounding simultaneously. The average error for our combined polysilicon and diffusion rounding model is 2.7% (I_{on} error=1.8%, I_{off} error=3.7%). Finally, our experiments show that cell area can be reduced by relaxing design rules without penalty in performance. Extending our model for large angle drain side diffusion rounding, and experiment on more complex gates/circuits and proof-of-concept silicon are part of our on-going work.

[8]This experiment uses SPICE-based calibrated model in section III.

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