# Single-Mask Double-Patterning Lithography

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## ABSTRACT

This paper proposes shift-trim double patterning lithography (ST-DPL), a cost-effective method for achieving 2× pitch-relaxation with a single photomask (especially at polysilicon layer). The mask is re-used for the second exposure by applying a translational mask-shift. Extra printed features are then removed using a non-critical trim exposure. The viability of ST-DPL is demonstrated. The proposed method has many advantages with virtually no area overhead ($< 0.3\%$ standard-cell area): (1) cuts mask-cost to nearly half that of standard-DPL, (2) reduces overlay errors between the two patterns and can virtually eliminate it in some process implementations, (3) alleviates the bimodal problem in double-patterning, and (4) enhances throughput of first-rate scanners. We implement a small 45nm standard-cell library and small benchmark designs with ST-DPL to illustrate its viability.

**Keywords:** Double patterning, shift-trim, photomask, trim exposure, overlay, bimodal CD distribution, scanner throughput.

## 1. INTRODUCTION

Double-patterning lithography (DPL) is one of the most likely short-term solutions for keeping the pace of scaling beyond 32nm node [6]. It is one of the many resolution enhancement techniques (RET) that have been introduced to push the limit of optical lithography. DPL can be implemented with different manufacturing processes: litho-etch-litho-etch (LELE), litho-litho-etch (LLE), and spacer double-patterning (SDP). In SDP, features are defined by sidewall spacer making it more suitable for well-structured memory cells rather than random logic layout [6]. This paper focuses on LELE and LLE processes referred to as standard-DPL processes hereafter.

DPL has three major impediments:

1. high mask-cost compared to standard single patterning because of its use of two critical photomasks to pattern a single layer;
2. reduced fabrication throughput due to additional processing steps needed for the second pattern;
3. tight overlay budget because overlay of second to first pattern translates directly into CD variability [7] (which has a budget three times tighter than inter-layer overlay according to ITRS [8]).

An attempt to use DPL with a single photomask and, consequently, reduce its cost, is reported in [9]. It consists of splitting the mask area into two regions, each corresponding to a different pattern (similar to a multi-layer reticle). As reported in [9], this approach renders fabrication throughput even worse than that of standard-DPL and does not address DPL technical challenges.

In this paper we propose shift-trim DPL (ST-DPL), an effective method to use a single mask to achieve 2× pitch-relaxation (especially at polysilicon layer). Essentially, the method consists of applying a translational mask-shift to re-use the same photomask for both exposures of DPL. Extra printed features are then removed using a non-critical trim exposure. ST-DPL manufacturing process and design requirements are discussed in Section 2. In Section 3, the feasibility of this technology is demonstrated by creating an ST-DPL compatible standard-cell library by layout migration of Nangate open cell-library [1] and ST-DPL compatible real designs. Results show virtually no area overhead associated with ST-DPL implementation and a non-critical and easy to fabricate trim-mask. Benefits of the proposed method in terms of cost, overlay control, CD performance, and throughput are discussed in Section 4 while Section 5 concludes.

## 2. SHIFT-TRIM DPL

### 2.1 Manufacturing Process

ST-DPL involves the following steps:

1. print the first pattern as in standard DPL processes;
2. shift the photomask of step 1 by minimum gate pitch $X$ and print the second pattern;
3. apply a non-critical trim (a.k.a. block) exposure to get rid of unnecessary features.

ST-DPL can be implemented using LELE and LLE positive dual-line and negative dual-trench with little modifications to the processes as demonstrated in Figure 1*. Here, the processes are presented in order of popularity with the first process on the left being the most favorable. We only show the case of positive resist since it is standard for todays lithography. Negative resist can also be used with little modifications to the manufacturing process. In this paper, we assume a LELE positive dual-line process in ST-DPL demonstration. However, ST-DPL application with the other less popular processes is possible with slight modifications to the implementation.

The only extra step that ST-DPL requires on top of standard-DPL is an inexpensive and non-critical trim-exposure cycle (resist coat-expose-develop) and removal of hardmask corresponding to extra printed features before final etch. Trim-exposure is a mature and well-known method used in many patterning techniques such as double-patterning with spacer [14, 15], alternating phase-shift mask [13], and subtractive-litho patterning [17, 18]. It was recently employed to trim-away printing assist features (PrAF) introduced to enhance the resolution of conventional single patterning [16]. A second hardmask layer is necessary in case of positive LELE process. However, this does not represent an extra requirement since many standard DPL implementations favors the use of a second hardmask [7, 10]. Requirements on trim-exposure are easy. Trim-mask CD is much larger than that of critical-mask (at least twice as big) and the pitch is relaxed to a great extent. We show later in the paper more details on trim-exposure simplicity, which allows this step to be carried out on second-tier scanners with little impact on the overall throughput.

### 2.2 Layout Restrictions and Challenges

Basic layout restrictions are imposed for implementing ST-DPL. $X$ being the amount of mask-shift and $X_0$ being the minimum gate pitch of single patterning†, restrictions follow.

1. Gate-pitch is restricted: every other gate, pitch is either $X$ or $\geq X_0$. This is illustrated by the example of three gate-poly lines shown in Figure 2.
2. In light of (1), minimum gate spacing is equal to contacted-gate spacing (equal to $X$ minus poly-line width).
3. Poly routing is restricted to top and bottom routing channels of the cell (i.e. poly-routing in the center of the cell is not allowed).

In addition, some design rule restrictions (especially line-end to field-poly spacing and line-end gap) may be necessary to guarantee a simple trim-mask as we show later in this paper.

ST-DPL implementation for poly fixed pitch grating is straightforward and requires no redesign effort. In this case, ST-DPL critical mask still consists of fixed-pitch grating but with a perfect $2\times$ pitch relaxation. ST-DPL for unidirectional-poly designs with non-fixed pitch requires small redesign effort. In particular, adjustment of the pitch between some lines might be necessary to enforce restriction (1). Nevertheless, this restriction is easily met in real designs because majority of the gates are at contacted-pitch (equal to $X$) from at least one of its two neighbors. The critical mask for this type of designs consists of simple unidirectional lines with twice the minimum pitch of single patterning. The most challenging type of designs is conventional logic and sequential circuits that involve bidirectional-poly. To handle such designs, two lines in

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*BARC layers are not shown for brevity.

†$X_0$ is typically $2X$.

the opposite direction are added at the top/bottom of the critical mask of the cell leading to ladder-like shapes as illustrated in Figure 3[‡]. This permits the use of "wrong-way" poly to connect gates internally within the cell in the top/bottom routing channels. Both critical-mask options of Figure 3 are possible without any effects on the complexity of the trim-mask. Option (a) has wrong-way lines whether they are needed or not. On the other hand, option (b) has these lines only when needed. As a results, option (b) leads to less corner-rounding than option (a). Nevertheless, we preferred option (a) in our implementation because it is very regular making it more favorable for lithography [19, 20]. In these structures, gate-pitch is twice the minimum pitch of single patterning, i.e. ensuring pitch doubling, and small notches that appear on vertical lines correspond to contact-landing pads, which are not necessary in processes permitting trench contacts [18].

For all types of designs, layout decomposition into critical and shifted exposures is trivial as we show in Section 3.

[‡]The shape shown in this figure is for illustration purposes and do not include RET-related features.

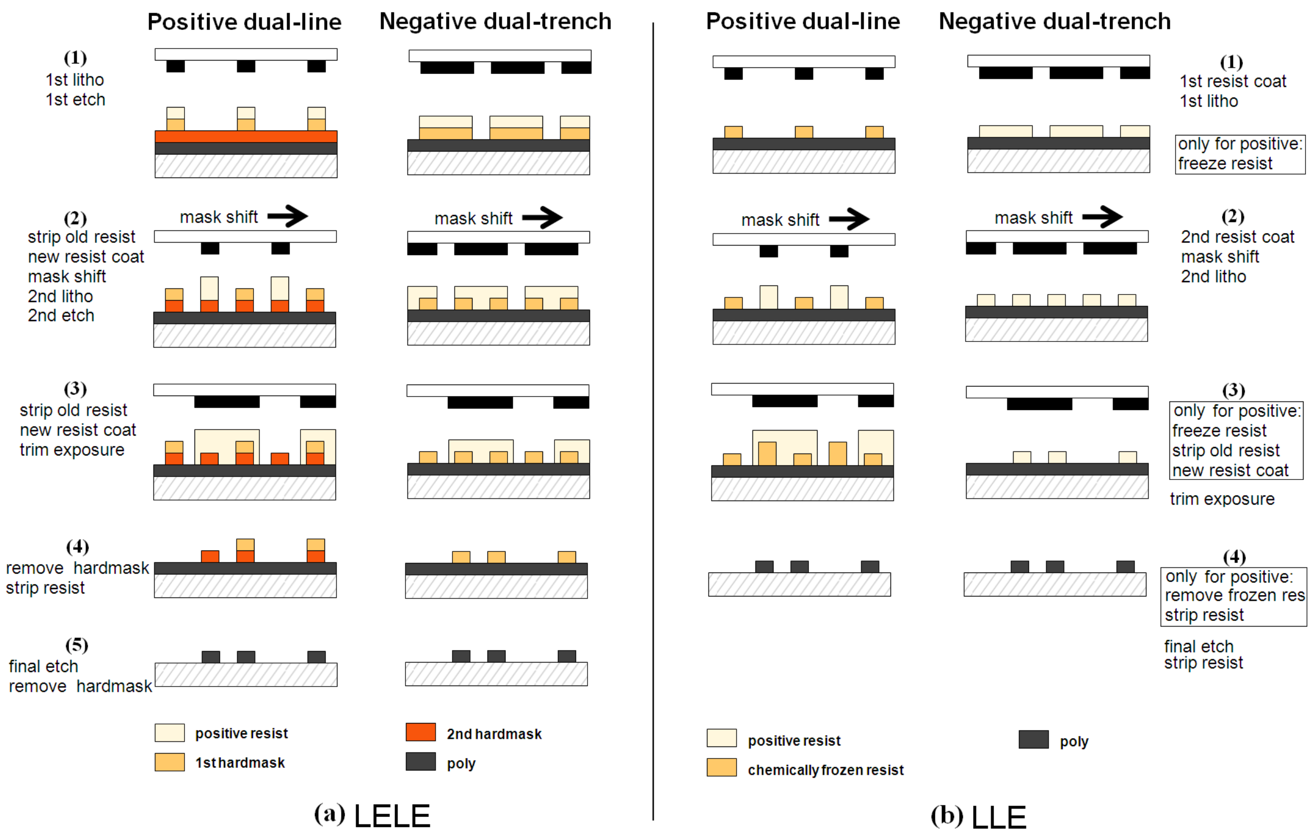



Figure 1: Proposed manufacturing processes for ST-DPL: (a) LELE and (b) LLE positive dual-line and negative dual-trench processes.

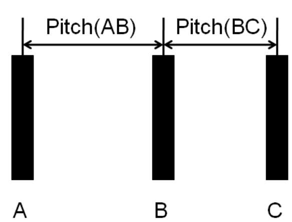



Figure 2: Example illustrating gate-pitch restriction. In case $Pitch(AB)$ is $< X_0$ but different than $X$, then $Pitch(BC)$ is restricted to either $X$ or $\geq X_0$. The same restriction applies to $Pitch(AB)$ if $Pitch(BC)$ is unrestricted.

ST-DPL steps applied to 4-input OAI standard-cell from Nangate 45nm open library [1] are illustrated in Figure 4. In this example, the cell-layout was made compatible with ST-DPL without any area overhead. ST-DPL application for most standard-cells is straightforward and introduces no or little area overhead as we show in the next section.

Even though the same features with exactly same surrounding are in the first and second exposures, printed images of the first and second patterns are different because of process-differences (e.g. resist thickness, hardmask characteristics, etch-interference, etc...). One way to compensate for this difference consists of using different OPC features for the different patterns [12]. In ST-DPL, this method is no longer possible since the same mask is used for the first and second exposures. As a result, other means to correct for processing differences between the two patterns must be employed (e.g. dose-mapping).

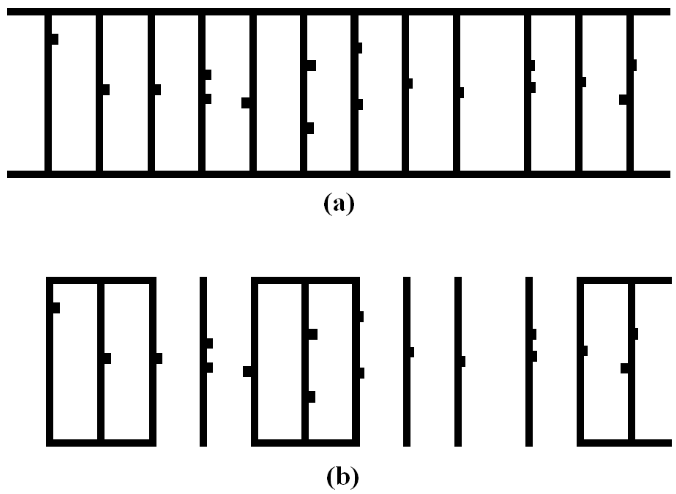



Figure 3: ST-DPL critical mask snippet corresponding to a flip-flop cell with two structure-options (a) and (b).

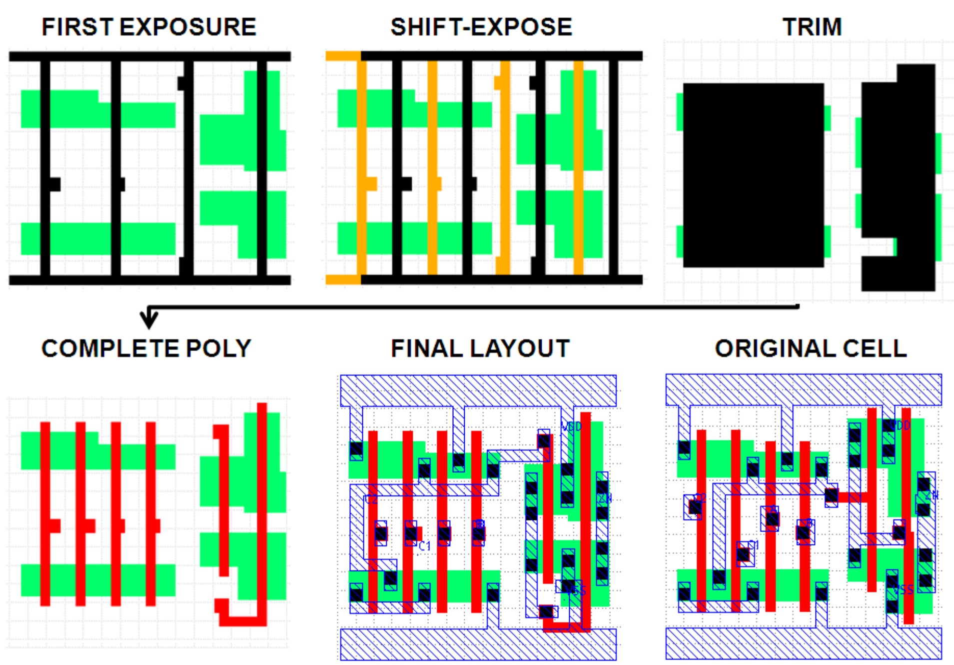



Figure 4: Example of 4-input OAI cell layout migrated for the application of ST-DPL.

Table 1: ST-DPL compatible standard-cell library and associated area. Note that the area overhead is quantized due to cell-pitch restrictions from place and route.

| **Cell-type** | **Original Area [$um^2$]** | **ST-DPL Area [$um^2$]** | **Area overhead [$um^2$]** |
|---|---|---|---|
| AND2 { X2, X4} | 1.064/1.064 | 1.064/1.064 | 0 |
| AND3 { X1} | 1.33 | 1.33 | 0 |
| AOI211 { X1} | 1.33 | 1.33 | 0 |
| AOI21 { X1} | 1.064 | 1.064 | 0 |
| AOI221 { X2} | 1.596 | 1.596 | 0 |
| AOI222 { X2} | 2.128 | 2.128 | 0 |
| AOI22 { X1, X2} | 1.33/1.33 | 1.33/1.33 | 0 |
| BUF { X1, X2} | 0.798/0.798 | 0.798/0.798 | 0 |
| CLKBUF { X1, X2, X3} | 0.798/1.064/1.33 | 0.798/1.064/1.33 | 0 |
| INV {X1, X2} | 0.532/0.532 | 0.532/0.532 | 0 |
| INV {X4} | 0.532 | 0.798 | 0.266 |
| INV {X8} | 0.798 | 1.064 | 0.266 |
| INV {X16} | 1.33 | 1.596 | 0.266 |
| NAND2 { X1, X2, X4} | 0.798/0.798/1.33 | 0.798/0.798/1.33 | 0 |
| NAND3 { X1} | 1.064 | 1.064 | 0 |
| NAND4 { X2} | 1.33 | 1.33 | 0 |
| NOR2 { X1, X2} | 0.798/0.798 | 0.798/0.798 | 0 |
| NOR4 { X2} | 1.33 | 1.33 | 0 |
| OR2 { X1, X2} | 1.064/1.064 | 1.064/1.064 | 0 |
| OR3 { X2} | 1.33 | 1.33 | 0 |
| OR4 { X2} | 1.596 | 1.596 | 0 |
| OAI21 { X1, X2} | 1.064/1.064 | 1.064/1.064 | 0 |
| OAI22 { X1} | 1.33 | 1.33 | 0 |
| OAI33 { X1} | 1.862 | 1.862 | 0 |
| OAI211 { X1, X2, X4} | 1.33/1.33/2.128 | 1.33/1.33/2.128 | 0 |
| XOR2 { X1, X2} | 1.596/1.596 | 1.596/1.596 | 0 |
| DFF {X1} | 5.054 | 5.054 | 0 |
| SDFF {X2} | 6.916 | 6.916 | 0 |

## 3. IMPLEMENTATION

In this section, we demonstrate the application of ST-DPL for standard cell-based designs.

### 3.1 ST-DPL Standard-Cell Library and Mask Layout Generation

We develop ST-DPL compatible standard-cell library by manual layout migration of Nangate open cell library [1] using FreePDK [23] 45nm process design rules. Details on ST-DPL cell library are presented in Table 1. Most standard-cells have fairly simple layouts and are made compliant to ST-DPL technology with little or no redesign effort. However, layout migration of large cells that use poly to route gate signals require more time and effort. The primary reason for this complication comes from contact landing pads being printed in the shifted exposure whether they are needed or not. So unless the part of the line containing the landing pad is trimmed away in the shifted version, enough room must be available so that poly-to-active spacing design rule is not violated. This requires location adjustment of active regions in some cases. For a process enabling trench contacts (e.g. Intel's 45nm process [18]), this complication is eliminated and layout migration can be easily automated.

Layout decomposition into first and second exposures is automated (C++ program based on OpenAccess 2.2 API [22]). Since wrong-way poly (horizontal lines of Figure 3(a)) is printed in both exposures, the decomposition problem is reduced to assigning gate-poly lines (vertical lines of Figure 3(a)) to the two exposures. Traversing each cell in the library from left to right, the following decomposition rules applies:

- if the pitch with the previous line is $X$, the line is assigned to the shifted-exposure (i.e. second exposure) and the previous line is assigned to the first exposure;

- if the pitch with the previous line is $< X_0$ and different than $X$, the line is assigned to the first exposure and the previous line is assigned to the second exposure;
- if the pitch with the previous line is $> X_0$, the line can be assigned to either of the two exposures.

Since the trim-mask covers the entire poly-layer in our ST-DPL proposed process, we start by the poly-layer as the base structure of the trim-mask and apply a series of expansions to simplify the mask. Trim-mask structures of two successive gates with pitch $< X_0$ are joined. For gates with larger pitch and gates at the cell-edge, trim-mask structures of each gate are expanded by $S_{min}/2$, where $S_{min}$ is the minimum separation between gates (i.e. $X$ minus gate line-width). This large trim-mask coverage of gates is to have a large resist thickness at sidewalls after development preventing etch interference with gate features under imperfect overlay and etch control (see process details in Figure 1). Trim-mask coverage of field-poly is limited to 20nm on all sides to maximize spacing between trim-mask features. Here, sidewall resist thickness requirement is much smaller than in the case of gate-poly because CD control is much less important. Since poly line-ends are formed by printing a long line in one exposure and cutting its ends in another exposure (i.e. trim-exposure), line-end tapering [21] and pull-back (a.k.a. shortening) are substantially reduced [17]. Hence, we assume line-end extension rule, which only addresses trim-to-STI overlay error and possible damage of line-end by etch in ST-DPL, can be reduced from 55nm to 35nm. With this setup, the overall margin of trim-mask overlay error is at least 20nm in $X$ as well as $Y$ directions.

To guarantee trim-mask easy fabrication and quality trimming, we enforce few design rule restrictions.

1. Poly line tip-to-side and tip-to-tip within-cell spacing rules are increased from 75nm to 140nm.
2. Top/bottom "wrong-way" poly lines used for routing are pushed 35nm toward the center of the cell.
3. Line-ends are extended at most up to the starting location of "wrong-way" lines.

Rule (1) is to ensure reasonable dimensions of the holes in the trim-mask (at least 100nm wide) that can occur in such situations within a cell as illustrated in Figure 5. Rule (2) and (3) are introduced to avoid small holes in the trim-mask that might occur at cell boundaries, as illustrated in Figure 6, resulting in a relaxed separation of at least 100nm between trim-mask features of different cells.

All these rules are specific to FreePDK 45nm process that the cell library is based on and might not be needed for other process technologies. For example, rules (2) and (3) are very likely to be unnecessary (or at least smaller) for commercial processes where line-end gap is considerably larger than the minimum field-poly spacing to meet manufacturability requirements unlike in the case of FreePDK where line-end gap rule is equal to the minimum field-poly spacing. In addition,

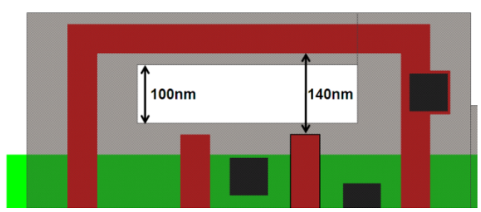
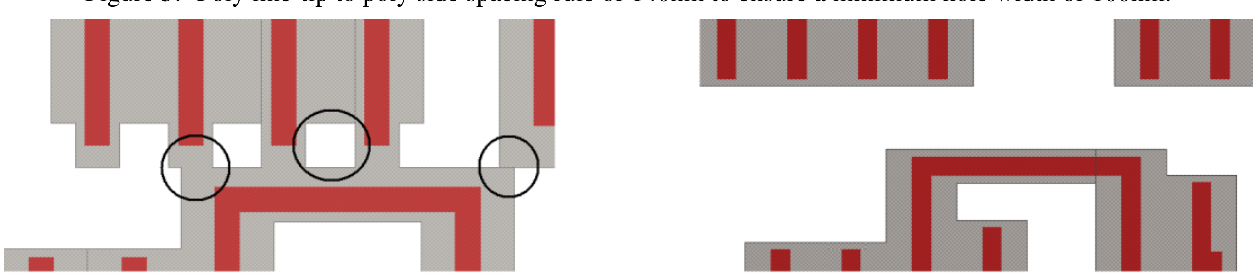



Figure 5: Poly line-tip to poly side spacing rule of 140nm to ensure a minimum hole width of 100nm.



**(a)** **(b)**

Figure 6: Trim-mask complexity at cell-boundaries before (a) and after (b) including rules (2) and (3).

Table 2: Details of ST-DPL compatible designs showing negligible area overhead.

| | Description | Cell instances | Cell-types | Flip-flops | INV/BUF | Cell-area $[um^2]$ | Area overhead |
|---|---|---|---|---|---|---|---|
| mips789 | processor core | 10529 | 35 | 2011 | 1465 | 22867.5 | 0.02% |
| or1200 | combinational logic | 3070 | 35 | 0 | 890 | 3014.8 | 0.34% |
| usb | com. controller | 478 | 31 | 93 | 52 | 880.2 | 0% |

rules (2) and (3) might be avoided for a cell-library designed for ST-DPL technology rather than migrated from an existing library. In particular, the trim-mask simplification at cell-boundaries are better handled during optimization of cell-height and line-end gap rules.

A final step of trim-mask simplification is performed to avoid notches wherever possible as illustrated in Figure 7. In Figure 7(a), notch-filling is performed by extending the trim-mask coverage of field-poly. This is not possible if the neighboring gate in the direction of the extension and within close proximity uses the same "wrong-way" poly track to connect to another signal. In this case, the trim-mask extension violates the minimum separation of trim-mask features and might create a bridge-defect. In Figure 7(b), notch-filling is performed by leveling line-ends of neighboring gates (by extension of the shorter line-end).

After generating the different masks for all cells in the library and all possible cell-orientations, mask generation for ST-DPL compatible designs is a simple step. For each cell-instance, cell-type and orientation are determined and mask-features are copied from the corresponding cell in the library to the instance location in the design. The generated mask layout is free of errors at cell-boundaries because critical-mask features outside the cell (or close to the cell-edge) are trimmed away and enough spacing between trim-mask features of different cells is guaranteed by construction.

### 3.2 Results

ST-DPL standard-cell library was implemented without area overhead compared to the original Nangate library layouts except for three cells as shown in Table 1. This overhead is caused by layout restrictions imposed to simplify the trim-mask. In case these restrictions are avoided for the reasons discussed earlier, ST-DPL does not have any area overhead in all cells. Moreover, if option(b) of Figure 3 is used instead of option(a), i.e. having "wrong-way" poly tracks only when needed, ST-DPL implementation of these three inverter-cells results in no area overhead because rule (2) can be avoided.

Three designs from [24] are synthesized in Cadence RTL Compiler ™v6.2 using the developed ST-DPL standard-cell library. Designs are placed and routed using Cadence SOC Encounter ™v6.2. Details on the designs and associated *cell-area* overhead are presented in Table 2. *Cell-area* overhead for all three designs is negligible (at most 0.34%). The reason is attributed to low utilization of the cells where area overhead occurs (low utilization of large-size inverters is typical).

Mask layouts are automatically generated for all three designs. A snippet of trim-mask layout for the "usb" design is shown in Figure 8. In this figure, simple blocks with few vertices correspond to cells with unidirectional poly and more complex shapes correspond to flip-flops involving bidirectional poly-routing. Hence, the trim for purely unidirectional poly designs consists of extremely simple features (large rectangles mostly). Trim-mask complexity is further analyzed. In Table 3, we report minimum line-width, notch size, hole dimensions, and number of fractures of the trim-mask. These minimum dimensions are fairly large compared to the minimum feature size of the process (i.e. 50nm) resulting in simple trim-mask for all designs. The dimensions listed in the table are not to be compared directly to dimensions of the critical-mask because trim-mask features do not define patterns but rather protect existing patterns by larger coverage. The number

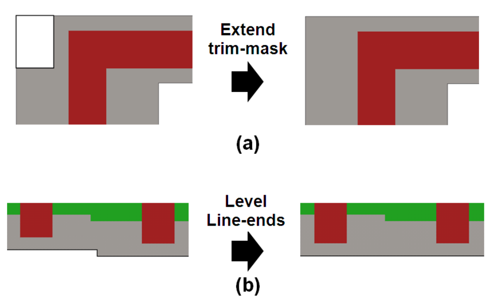



Figure 7: Trim-mask notch-fill by (a) trim-mask extension and (b) poly line-end leveling.

Table 3: Details on trim-mask for the design of Figure 2 showing very basic fabrication requirements.

| | Line-width $[nm]$ | Notch **Size** $[nm]$ | Hole **dimensions** $[nm]$ | Overlay margin $[nm]$ | Trim-mask **poly fractures** | **Post-OPC mask fractures** |
|---|---|---|---|---|---|---|
| mips789 | $\geq 90$ | $\geq 70$ | $\geq$ 190 x 145 | 20 | 78597 | 367633 |
| or1200 | $\geq 90$ | $\geq 70$ | $\geq$ 380 x 100 | 20 | 5189 | 43150 |
| usb | $\geq 90$ | $\geq 70$ | $\geq$ 190 x 145 | 20 | 2770 | 14404 |

of fractures of the trim-mask (determined using Calibre MDP™v2008), which affects mask-cost, is 5 to 8 times smaller than the number of feature for post-OPC poly-layer (OPC generated using Calibre OPC™v2008). In addition, the trim-mask does not require expensive RET features such as OPC and SRAF which substantially increase mask-complexity and cost.

## 4. ST-DPL BENEFITS

In addition to cutting mask-cost to nearly half that of standard DPL because of critical-mask reuse for both exposures and a cheap trim-mask as shown in Section 3, ST-DPL has benefits in terms of overlay, CD control, and throughput.

### 4.1 Overlay and Throughput Benefits

Negative LLE process which does not require wafer removal from the exposure tool chuck between the two exposures (as illustrated in Figure 1)was shown to be viable [5] and has good chances of being adopted because of its throughput benefits. In case such process is used in combination with ST-DPL, the second exposure can be performed after a blind translational shift without any alignment of the second exposure. This practically eliminates any overlay error between the two patterns and, also, saves alignment time.

An important source of overlay is reticle metrology errors [4], which is caused by reticle mounting and heating as well as particle contamination of the reticle alignment marks. Since mask loading and unloading between both exposures is not necessary in ST-DPL, this source of overlay error is virtually eliminated in all ST-DPL process implementations. Moreover, reticle alignment, which is another source of overlay, is again eliminated in all ST-DPL processes for the same reason. The time spent on mask loading/unloading as well as reticle alignment is saved.

A major source of overlay is registration error ($\approx 25\%$) [11]. In DPL, registration error of the two exposures is observed to be correlated which greatly reduces its impact on overlay. This correlation is mainly attributed to mask-layout similarity [11,25]. In ST-DPL, registration error is expected to have a higher correlation factor than in the case of standard DPL since mask-layout is exactly the same for both exposures.

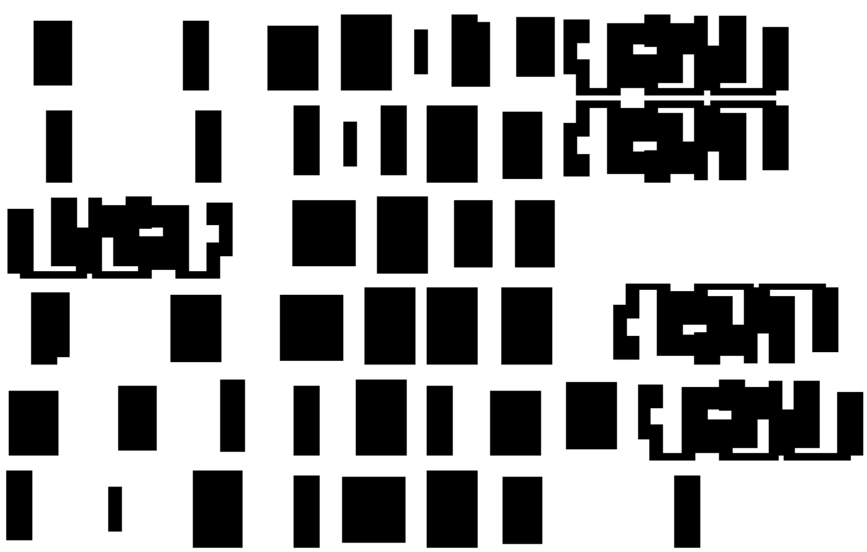


Figure 8: Trim-mask layout snippet where simple large blocks correspond to cells with unidirectional poly and more complex shapes correspond to flip-flops with bidirectional poly-routing.

Table 4: Summary of ST-DPL overlay benefits.

| Source | Overlay contribution | Benefit |
|---|---|---|
| All sources | 100% | almost eliminated in case of negative dual-trench LLE process |
| Reticle metrology | n/a | eliminated for all ST-DPL processes |
| Reticle alignment | n/a | eliminated for all ST-DPL processes |
| Registration | 25% | reduced for all ST-DPL processes |

### 4.2 Alleviating CD Bimodality Problem

Whenever two patterns are formed in different exposure and etch steps, lines and spaces have bimodal CD distributions [2] that can have severe implications for the digital design flow [26]. Since in ST-DPL the same mask is used for both exposures, mask CDU, which is the second most important contributor to the overall CD variation as reported in [2, 3], no longer affects the difference between the two distribution and the bimodal problem is alleviated.

Considering CD of the first ($CD_a$) and second ($CD_b$) patterns as random variables, then

$$\begin{aligned} CD_a &= \mu_a + m_a + nm_a, \\ CD_b &= \mu_b + m_b + nm_b, \end{aligned} \tag{1}$$

where $\mu_a$ and $\mu_b$ are the mean of $CD_a$ and $CD_b$ respectively, $m$ is mask CDU random variable and $nm$ (short for non-mask) is a random variable corresponding to all other contributors to line CDU. Assuming $CD_a$, $CD_b$, and all other random variables of Equation 2 have independent normal distributions in standard-DPL, the covariance of the two CD distributions is zero and CD difference has a normal distribution with $\mu_{diff} = \mu_a - \mu_b$ and $\sigma_{diff} = \sqrt{\sigma_a^2 + \sigma_b^2}$, where $\sigma_a$ and $\sigma_b$ are the standard deviations of $CD_a$ and $CD_b$ distributions respectively. In case of ST-DPL, $m_a = m_b = m$ and, consequently, the covariance is

$$\begin{aligned} Cov(a,b) &= E(a.b) - \mu_a \times \mu_b \\ &= \mu_a \times \mu_b + \mu_a(m + nm_b) + \mu_b(m + nm_a) + m(nm_a + nm_b) + nm_a \times nm_b + m^2 - \mu_a \times \mu_b \\ &= \mu_a(m + nm_b) + \mu_b(m + nm_a) + m(nm_a + nm_b) + nm_a \times nm_b + m^2. \end{aligned} \tag{2}$$

Since $m$, $nm_a$, and $nm_b$ have zero mean, Equation 3 simplifies to

$$Cov(a,b) = \sigma_m^2, \tag{3}$$

where $\sigma_m$ is the standard deviation of mask CDU normal distribution. The distribution of CD difference has $\mu_{diff} = \mu_a - \mu_b$ and $\sigma_{diff} = \sqrt{\sigma_a^2 + \sigma_b^2 - 2Cov(a,b)} = \sqrt{\sigma_a^2 + \sigma_b^2 - 2\sigma_m^2}$ (from Equation 3).

Using line-CDU breakdown values for LELE positive dual-line 32nm process from [2] (i.e. 2.7nm $3\sigma$ from etch, 1.4nm $3\sigma$ from mask-CDU, 0.7nm $3\sigma$ from dose, and 0.5nm $3\sigma$ from focus), $\sigma_{diff}$ is 1.49nm in the case of standard-DPL and 1.34nm in the case of ST-DPL which corresponds to a 10.3% reduction in standard deviation.

### 4.3 Comparison with Popular Patterning Techniques

In this section, ST-DPL technology is compared to other popular patterning techniques including standard-DPL and subtractive-litho of [18]. Essentially, subtractive-litho consists of printing a grating and removing dummy-poly with a trim-exposure. A summary of attributes is presented in Table 5. Subtractive-litho can suffer from a large area overhead when fixed-gate pitch is imposed as reported in [27]. Even though this technique has good printability due to its imposed regular layout, it does not achieve pitch-doubling which might be necessary to enable scaling to future technology nodes. Clearly, ST-DPL has many advantages over standard-DPL as discussed earlier. The only drawbacks of ST-DPL in this comparison is higher redesign effort and the use of a trim-exposure. ST-DPL designs are compatible with spacer double-patterning (SDP) technology enabling poly-routing with almost no mask-assignment effort. Hence, cell/block reuse from one technology to the other is possible. Trim-exposure non-criticality allows its processing on second-rate fabrication-lines and its use permits the reduction of line-end extension rule as discussed earlier in this paper.

Table 5: Summary of comparison between subtractive-litho, standard-DPL, and ST-DPL methods.

| | **Subtractive-litho [18]** | **Standard-DPL** | **ST-DPL** |
|---|---|---|---|
| Mask-cost | best | worst | intermediate |
| Trim | yes | no | yes |
| Pitch doubling | no | yes | yes |
| Area overhead | worst | best | best |
| Designing effort | worst | none | intermediate |
| Layout decomposition | none | tough | trivial |
| Variability | best | worst | intermediate |
| CD bimodality | no | yes | reduced |
| Same-layer Overlay | no | yes | reduced |
| Throughput | best | worst | intermediate |

## 5. CONCLUSION

ST-DPL is a viable and promising technique to achieve 2× pitch relaxation. It allays major DPL impediments: cost, overlay control, CD performance, and throughput. In case of LEE negative dual-trench process, ST-DPL virtually eliminates overlay error between the two patterns of the same layer extending the lifetime of scanners to future nodes. On the down side, layout design effort and ST-DPL aware CAD tools are necessary for this technique to deploy. Another overhead is trim exposure and its associated processing steps, but this may not be a concern for many DPL implementations that already employ a trimming step. ST-DPL benefits are believed to be worthwhile especially for fairly regular layouts, where little layout-modification is needed, and low-volume manufacturing, where mask cost is a big concern. Implementation of ST-DPL for metal layers, contacts, and vias as well as ST-DPL aware layout solutions are part of ongoing work.

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## REFERENCES

[1] Nangate Open Cell Library v1.2. Available: http://www.si2.org/openeda.si2.org/projects/nangatelib.

[2] J. Finders *et al.*, "Double patterning for 32nm and below: an update," *Proc. of SPIE Double Masking*, p. 692408-1, 2008.

[3] M. Dusa *et al.*, "Pitch doubling through dual patterning lithography challenges in integration and litho budgets," *Proc. SPIE Conference on Optical Microlithography*, p. 65200G-1, 2007.

[4] K. Suzuki and B. W. Smith, *Microlithography: science and technology*, Second Edition, Boca Raton: CRC Press, 2007.

[5] S. Lee, *et al.*, "An analysis of double exposure lithography options," *Proc. SPIE Optical Microlithography*, p. 69242A-1, 2008.

[6] C. A. Mack, "Seeing double" *IEEE Spectrum*, pp. 46-51, Nov. 2008.

[7] W. Arnold, M. Dusa, and J. Finders, "Manufacturing challenges in double patterning lithography," *IEEE Intl. Symp. Semiconductor Manufacturing* , pp.283-286, 25-27 Sept. 2006.

[8] International Technology Roadmap for Semiconductors, report, 2007.

[9] Y. Yamamoto, R. Rigby, and J. Sweis, "Multi-layer reticle (MLR) strategy application to double-patterning/double-exposure for better overlay error control and mask cost reduction," *Proc. of SPIE Photomask Technology*, p. 67302X, 2007.

[10] C. F. Tseng, C. C. Yang, E. Yang, T. H. Yang, K. C. Chen, and C. Y. Lu, "A comprehensive comparison between double patterning and double patterning with spacer on sub-50nm product implementation," *Proc. of SPIE*, p. 69241Y-3, 2008.

[11] D. Lee *et al.*, "Impact of registration error of reticle on total overlay error budget," *J. Vac. Sci. Technol.*, B24(6), 2006.

[12] M. de Beeck *et al.*, “Manufacturability issues with double patterning for 50-nm half-pitch single damascene applications using RELACS shrink and corresponding OPC,” in textitProc. of SPIE, vol. 6520, p. 65200I, 2007.

[13] L. Liebmann, “Enabling alternating phase shifted mask designs for a full logic gate level: design rules and design rule checking,” *Proc. of Design Automation Conference, DAC’01*, 2001.

[14] W. Shiu *et al.*, “Spacer double patterning technique for sub-40nm DRAM manufacturing process development,” *Proc. of SPIE Lithography Asia*, p. 71403Y, 2008.

[15] T. Chiou *et al.*, “Full-chip pitch/pattern splitting for lithography and spacer double patterning technologies,” *Proc. of SPIE Lithography Asia*, p. 71401Z, 2008.

[16] H. Haffner, J. Meiring, Z. Baum, S. Halle, “Paving the way to a full chip gate level double patterning application,” *SPIE/BACUS Photomask Technology*, p. 67302C, 2007.

[17] E. Vreugdenhil, H. Benten, L. Reijnen, G. Dicker, J. Gemmink, F. Bornebroek, “Yield Aware Design of gate layer for 45 nm CMOS-ASIC using a high-NA dry KrF systems,” *Proc. of SPIE*, 69250D, 2008.

[18] K. Mistry *et al.*, “A 45nm logic technology with high-k+metal Gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging,” *IEEE Int. Electron Devices Meeting*, pp. 247-250, 2007.

[19] M. C. Smayling, H. Liu, and L. Cai, “Low k1 logic design using gridded design rules,” in *Proc. SPIE*, vol. 6925, 2008, p. 69250B.

[20] L. Pileggi, H. Schmit, A. Strojwas, P. Gopalakrishnan, V. Kheterpal, A. Koorapaty, C. Patel, V. Rovner, and K. Tong, Exploring regular fabrics to optimize the performance-cost trade-off, in *Proc. IEEE/ACM Design Automation Conference DAC03*, 2003.

[21] P. Gupta, K. Jeong, A. B. Kahng, and C. Park, “Electrical metrics for lithographic line-end tapering,” in *Proc. SPIE*, vol. 7028, p. 70283A, 2008.

[22] http://openeda.org

[23] FreePDK. [Online]. Available: http://www.eda.ncsu.edu/wiki/FreePDK

[24] [Online]. Available: http://www.opencores.org/

[25] K. Bubke, R. de Kruif, J. H. Peters, M. Dusa, and B. Connolly, “Mask characterization for double patterning lithography,” *J. Micro/Nanolith. MEMS MOEMS* 8(1), p. 011004, 2009.

[26] K. Jeong and A. B. Kahng, “Timing analysis and optimization implications of bimodal CD distribution in double patterning lithography,” *Proc. Asia and South Pacific Design Automation Conf.*, pp. 486-491, 2009.

[27] R. S. Ghaida and P. Gupta, “A framework for early and systematic evaluation of design rules,” to appear in *Intl. Conf. on Computer-Aided Design, ICCAD’09*, 2009.