Design-Overlay Interactions in Metal Double Patterning

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ABSTRACT

In double patterning lithography (DPL), overlay error between two patterning steps at the same layer translates into CD variability. Since CD uniformity budget is very tight, overlay control becomes a tough challenge for DPL. In this paper, we electrically evaluate overlay error for BEOL DPL with the goal of studying relative effects of different overlay sources and interactions of overlay control with design parameters. Experimental results show the following: (a) overlay electrical impact is not significant in case of positive-tone DPL ($<$ 3.4% average capacitance variation) and should be the base for determining overlay budget requirement; (b) when considering congestion, overlay electrical impact reduces in positive-tone DPL; (c) Design For Manufacturability (DFM) techniques like wire spreading can have a large effect on overlay electrical impact (20% increase of spacing can reduce capacitance variation by 22%); (d) translation overlay has the largest electrical impact compared to other overlay sources; and (e) overlay in y direction (x for horizontal metallization) has negligible electrical impact and, therefore, preferred routing direction should be taken into account for overlay sampling and alignment strategies.

Keywords: Double patterning, overlay, overlay control, alignment strategy, overlay budget, DFM, wire spreading, wire widening, congestion.

1. INTRODUCTION

Double patterning lithography (DPL) is expected to be used for volume manufacturing at 32nm technology node [2]. DPL has a serious technical challenge of meeting overlay requirements [3]. Single-patterning overlay budget is estimated by ITRS [1] to be 20% of the design rule. On the other hand, CD budget is much tighter and is approximated by ITRS to be 7% of the design rule. In DPL, overlay error contributes to CD variability, which has a very tight budget even for single-patterning [8,9]. Overlay error between different patterns in the same metal layer can affect (a) metal spacing, which translates into interconnect capacitance variability; or (b) metal width, which translates into interconnect resistance as well as capacitance variability (illustrated in Figure 1).

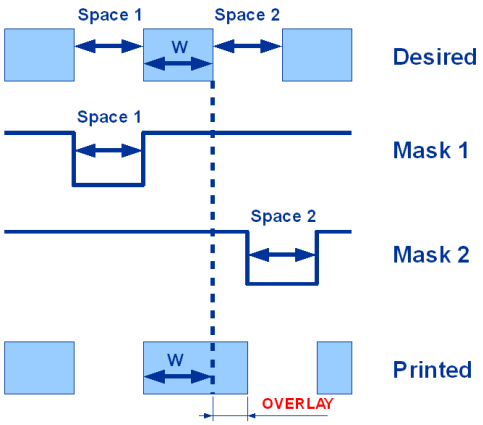

Figure 1. Example showing translation of overlay error into CD variation in negative-tone DPL.

In this paper, we electrically evaluate overlay errors for BEOL DPL with the goal of studying relative importance of different overlay sources and interactions of overlay control with design parameters and, consequently, trying to alleviate the overlay problem in DPL.

The next section describes overlay error and its impact on electrical characteristics of wires. In Section 2, experimental methodology and results are presented and observations are discussed. Finally, Section 3 concludes with a summary and directions for future work.

2. ELECTRICAL IMPACT OF OVERLAY

In BEOL process implemented with DPL, overlay error between two patterning steps at the same layer affects electrical characteristics of wires. This section exhibits models for overlay and its electrical impact that are used in our experiments.

2.1 Overlay Modeling

Overlay error between different-exposure patterns is described by an overlay model that is used for overlay control and correction. Major overlay components are translation, magnification, and rotation in the wafer and field [5, 7] and are considered in a linear-type overlay model. High-order models are also used with some scanners to enhance overlay accuracy, but such models requires more overlay sampling and alignments [10–12]. In our study, we adopt the following widely used linear model [7]:

$$\begin{aligned} \delta_x &= T_x + M_{wx} \times X_w - R_{wx} \times Y_w + M_{fx} \times X_f - R_{fx} \times Y_f + Res_x, \\ \delta_y &= T_y + M_{wy} \times Y_w + R_{wy} \times X_w + M_{fy} \times Y_f + R_{fy} \times X_f + Res_y, \end{aligned} \tag{1}$$

where δ_x (δ_y) is the total overlay error in the X (Y) direction. T, M, and R refer to translation, magnification, and rotation overlay parameters respectively. Res is the residual parameter and accounts for un-modeled secondary overlay components such as skewness and trapezoidal overlay. w and f stand for wafer and field respectively. (X_w, Y_w) and (X_f, X_f) refer to Cartesian coordinates in the wafer and field respectively.

Even though the model's parameters are refined continuously during processing, the model still does not correct for overlay error totally. This imperfect correction has many reasons: field to field and wafer to wafer overlay variations, limited overlay sampling that does not cover entire wafer and lot, and un-modeled secondary overlay components.

2.2 Electrical Impact in Positive-Tone DPL

DPL can be implemented in a positive-tone process, which prints lines, or negative-tone process, which prints spaces [4,6]. If positive-tone process is implemented for BEOL, interconnect spacing (s), between the two patterns is affected leading to the change of interconnect line-to-line capacitance (C_{LL}).

We derive a closed form equation for C_{LL} between two parallel vertical lines of length L where one line is printed perfectly and the other is printed with overlay error. Using the parallel plate capacitance model, C_{LL} can be expressed as follows:

$$C_{LL} = \epsilon t \int_0^L \frac{1}{s^\star} dl, \tag{2}$$

where ϵ is the dielectric constant, t is the interconnect thickness, and $s^\star$ is interconnect spacing with overlay error. Using the overlay model of Equation (1) and converting from wafer and field coordinate system to design coordinate system, $s^\star$ is determined by:

$$\begin{gathered} s^\star = s - (T_x + M_{wx}X_o + M_x X_Q - R_{wx}Y_o - R_x Y_Q + Res_x) - M_x x + R_x y + sM_x + R_x L, \\ where \;\; R_x = R_{wx} + R_{fx}, \;\; M_x = M_{wx} + M_{fx}, \end{gathered} \tag{3}$$

(X_o, Y_o) and (X_Q, X_Q) refer to the coordinates of field origin in the wafer plane and die origin in the field plane respectively, and (x, y) are the coordinates the bottom left corner of the line of interest in the design plane. Consequently, the closed form equation of C_{LL} as a function of structure coordinates in the design is:

$$\begin{gathered} C_{LL} = \frac{\epsilon t}{R_x} \ln \frac{s - b - M_x x + R_x y + sM_x + R_x L}{s - b - M_x x + R_x y + sM_x}, \\ where \;\; b = T_x + M_{wx}X_o + M_x X_Q - R_{wx}Y_o - R_x Y_Q + Res_x. \end{gathered} \tag{4}$$

Similar derivation is performed for a structure of three parallel vertical lines of length L where lines at the edge are printed perfectly and the middle line is printed with overlay error. The closed form equation of C_{LL} in this case becomes

$$C_{LL} = \frac{\epsilon t}{R_x} \left[\ln \frac{s - b - M_x x + R_x y + sM_x + R_x L}{s - b - M_x x + R_x y + sM_x} + \ln \frac{s + b + M_x x - R_x y + (s+w)M_x}{s + b + M_x x - R_x y + (s+w)M_x - R_x L} \right]. \tag{5}$$

2.3 Electrical Impact in Negative-Tone DPL

In case of negative-tone process, interconnect width (w) is affected leading to the change of interconnect resistance (R) as well as interconnect capacitance (C).

Using the parallel plate capacitance model and overlay model of Equation (1), closed form equations for R and C are derived in a similar manner to the derivation of C_{LL} in case of positive-tone DPL. Considering a structure of two parallel vertical lines where the line of interest is formed by printing one space perfectly and the other with overlay error, R of the line of interest is described by:

$$R = \frac{\rho}{tR_x} \ln \frac{w - b - M_x x + R_x y - wM_x + R_x L}{w - b - M_x x + R_x y - wM_x}; \tag{6}$$

C_{LL} between the two lines is determined by:

$$C_{LL} = \frac{\epsilon t}{R_x} \ln \frac{s + M_{wx}X_o + M_x X_Q - R_{wx}Y_o - R_x Y_Q + M_x(x + w) - R_x y}{s + M_{wx}X_o + M_x X_Q - R_{wx}Y_o - R_x Y_Q + M_x(x + w) - R_x y - R_x L}; \tag{7}$$

and C_{LG} between the line of interest and plane of layer below is modeled by:

$$C_{LG} = \frac{\epsilon L}{2H}[2(w - b - M_x x - M_x w + R_x y) + R_x L]. \tag{8}$$

In Equations (6, 7, 8), b, R_x, and M_x are the same as in Equations (3, 4), ρ is the wire resistivity, and H is the height of inter-level metal insulator.

For a structure of three parallel vertical lines, R and C_{LG} are calculated using the same equations as for two-line structure, i.e. Equations (6, 8), but a new equation is needed for calculating C_{LL}. Assuming the space between first and second lines is printed perfectly while the space between second and third lines is printed with overlay error, C_{LL} is determined as follows:

$$C_{LL} = \frac{\epsilon t}{R_x} \ln \frac{s + M_{wx}X_o + M_x X_Q - R_{wx}Y_o - R_x Y_Q + M_x(x + w) - R_x y}{s + M_{wx}X_o + M_x X_Q - R_{wx}Y_o - R_x Y_Q + M_x(x + w) - R_x y - R_x L} + \frac{\epsilon t L}{s}. \tag{9}$$

3. EXPERIMENTS AND OBSERVATIONS

A series of experiments are performed to evaluate electrical impact of overlay in BEOL DPL. This section describes experimental setup and methodology and presents results and their interpretations.

3.1 Experimental Setup

We conduct experiments for evaluating overlay electrical impact in positive and negative-tone DPL. A 300mm wafer with 63 33x26mm fields each containing 4 copies of the same design is considered. The study is performed for BEOL 32nm technology node (i.e. metal 1 half pitch) at local interconnect levels with design rules adopted from ITRS [1]. Interconnect length (L) is set to 100μm, which is close to maximum wire length for local interconnect levels where DPL is likely to be implemented.

The test structures used in the experiments are the 2-line and 3-line structures depicted in Figure 2. In both structures, overlap capacitance (C_{LG}) is assumed to be between the line of interest and a single grounded plane at the layer below. Also, lines of the first pattern are labeled with "DP1" and are assumed to be formed perfectly, while lines of the second pattern are labeled with "DP2" and are printed with overlay error. For 2-line structure, total capacitance (C) of "DP2" wire is given by:

$$C = C_{LL} + C_{LG}; \tag{10}$$

as for 3-line structure, total capacitance (C) of "DP2" wire is given by:

$$C = C_{LL} + C'_{LL} + C_{LG}, \tag{11}$$

where C_{LL} and C'_{LL} are line-to-line coupling capacitance between line of interest and left and right lines respectively.

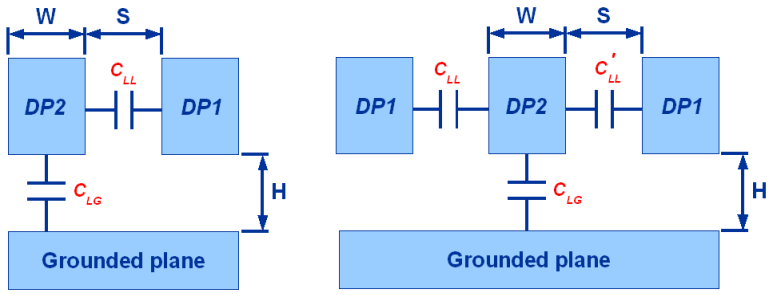

Figure 2. Test structures used in the experiments: (a) 2-line structure, and (b) 3-line structure with single grounded plane at the layer below.

Table 1. Overlay breakdown for reference experiment of estimated overlay components.

	% of imperfect correction	**Exact value [nm]**
Translation	5.32%	0.34
Wafer magnification	14.18%	0.91
Field magnification	2.48%	0.16
Wafer rotation	25.53%	1.63
Field rotation	2.48%	0.16
Residual	50%	3.2

Worst case overlay is assumed to be equal to ITRS 3σ overlay for single-patterning lithography in x and y directions, which is 20% of design rule (i.e. 6.4nm). 50% of the total overlay error is assumed to originate from un-modeled terms and random errors and are lumped into Res term; remaining 50% is assumed to originate from imperfect correction of the six primary overlay components, i.e. translation, magnification, and rotation in field and wafer. This assumption conforms well to experimental results reported in [13] where, after correction with a linear overlay model and excessive overlay sampling, 58% of overlay is non-systematic error and 42% of overlay is from imperfect correction of systematic error. Experiments with different decomposition cases of the overlay from imperfect correction among these components were performed to study their relative importance. A set of experiments involves extreme cases where all error caused by imperfect overlay correction is from a single source: translation, magnification, rotation, field overlay, or wafer overlay. For field and wafer extreme cases, overlay from imperfect correction is split equally among translation, magnification, and rotation overlay components. In addition, we run a reference experiment where decomposition is based on estimated required precision for overlay measurement offered in [14]. Table 1 shows overlay breakdown of this last decomposition.

Overlay parameters in Equations (6, 7, 8) can be inferred from the contributions of overlay components. T is equivalent to total translation and Res is equivalent to total residual because these two components are independent of location; whereas M_w, M_f, R_w, and R_f are inferred by considering worst case location that happens to be at the edge of wafer and field. Res is assumed to be in worst-case direction across the entire wafer, which is the same direction as T.

All parameters used in the experiments and corresponding values are summarized in Table 2.

Table 2. Parameters and corresponding values used in the experiments.

Parameter	**Value**
Wafer diameter	300mm
Number of fields	63
Field dimensions	33x26mm
Number of dies per field	4
w	32nm
s	32nm
t	60.8nm*
H	60.8nm
L	100μm
3σ overlay	6.4nm

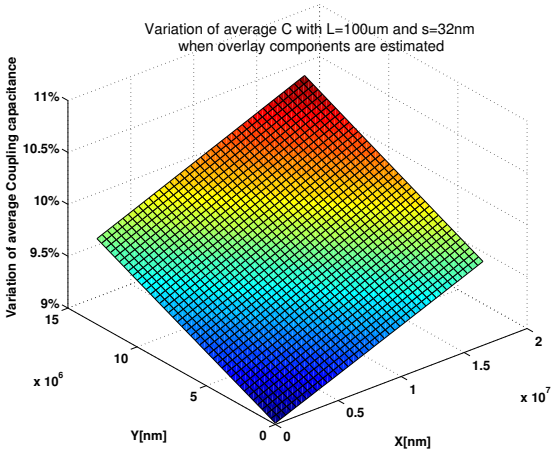

Figure 3. Average C variation for 2-line structure as a function of its location in the design when overlay components are estimated.

3.2 Measurement Methodology

Overlay impact on the electrical characteristics of test structures was measured at discrete locations of the structures in the design and for each copy of the design across the entire wafer. We evaluate absolute worst case impact as well as average impact over all design copies. For the case of average impact, minimum and maximum impacts for the different locations of the structures in the design are presented. In positive-tone DPL experiments, the change of C_{LL} and C are reported for worst and average cases. Similarly, in negative-tone DPL experiments, the change of RC_{LL} and RC are reported for the two cases.

3.3 Results

The first set of experiments is for structures formed with positive-tone DPL. Figure 3 plots average C variation for 2-line structure as a function of its location in the design when overlay components are estimated. This figure indicates that ΔC varies on average from 9% to 10.6% depending on the structure location in the design (all possible locations). Minimum variation occurs when the structure is located at the origin of the design, which is the center of the field in our experiments, and maximum variation occurs when the structure is located at the edge of the design, which is to the center of the field. This experiment is repeated for all other decomposition cases for 2-line and 3-line structures and worst and average impacts are reported. Results for positive-tone DPL experiments are summarized in Table 3.

Table 3. Results of capacitance variation for 2 and 3-line structures in positive-tone DPL.

	2-line structure				**3-line structure**			
	Avg variation		**Worst variation**		**Avg variation**		**Worst variation**	
	ΔC_{LL}	ΔC	ΔC_{LL}	ΔC	ΔC_{LL}	ΔC	ΔC_{LL}	ΔC
Estimated components	11.5-13.6%	9-10.6%	21.2%	16.6%	1.5-1.6%	1.4%	3.2%	2.8%
Translation extreme	25%	19.6%	25%	19.6%	4.2%	3.7%	4.2%	3.7%
Mag extreme	7.9-14.8%	6.2-11.6%	24.9%	19.5%	1.5-2%	1.3-1.7%	4.1%	3.6%
Rotation extreme	8.6-14%	6.75-11%	23%	18%	1.4-1.8%	1.2-1.6%	3.6%	3.2%
Wafer extreme	15-15.9%	11.8-12.4%	21.8%	17.1%	1.8-1.9%	1.6-1.7%	3.3%	2.9%
Field extreme	11.6-19.6%	9.1-15.3%	23.9%	18.7%	1.4-2.4%	1.2-2.1%	3.9%	3.4%

Similarly for negative-tone DPL, experiments for all decomposition cases are performed. However, RC product variation rather than C variation is reported. Table 4 summarizes the results of negative-tone process experiments.

3.4 Observations

Experimental results are interpreted and important observations are brought forward in this section.

*Based on ITRS prediction of aspect ratio

Table 4. Results of RC product variation for 2 and 3-line structures in negative-tone DPL.

	2-line structure				**3-line structure**			
	Avg variation		**Worst variation**		**Avg variation**		**Worst variation**	
	ΔRC_{LL}	ΔRC	ΔRC_{LL}	ΔRC	ΔRC_{LL}	ΔRC	ΔRC_{LL}	ΔRC
Estimated components	12.5-12.7%	9.8-10%	13.9%	10.9%	12-13.2%	10.6-11.6%	17.5%	15.4%
Translation extreme	25%	19.6%	25%	19.6%	25%	22%	25%	22%
Mag extreme	11.2-11.9%	8.8-9.3%	13.6%	10.7%	9.6-13.3%	8.4-11.7%	19.3%	16.9%
Rotation extreme	11.1-11.7%	8.7-9.2%	13.1%	10.3%	9.9-12.8%	8.7-11.3%	18.1%	15.9%
Wafer extreme	15.4-15.6%	12.1-12.2%	16.5%	12.9%	15.2-15.7%	13.4-13.8%	19.2%	16.8%
Field extreme	15.1-16.2%	11.8-12.7%	16.9%	13.3%	13.4-17.9%	11.7-15.7%	20.4%	17.9%

3.4.1 Relative importance of different overlay sources

Relative importance of different overlay sources can be inferred from results shown in Tables 3 and 4. For positive-tone DPL, translation extreme experiment leads to 19.6% ΔC; magnification extreme experiment leads to 6.2-11.6% average ΔC and 19.5% worst-case ΔC; and rotation extreme leads to 6.75-11% average ΔC and 18% worst-case ΔC. Translation impact on average ΔC is much more important than magnification and rotation impact. This difference is because magnification and rotation overlay vectors can have opposite directions and their effects are canceled out when averaging over entire wafer; whereas, translation is actually fairly uniform across the wafer[†]. However, for worst-case ΔC, translation, magnification, and rotation are almost equally important. For negative-tone DPL, translation extreme experiment leads to 19.6% ΔRC; magnification extreme experiment leads to 8.8-9.3% average ΔRC and 10.7% worst-case ΔRC; and rotation extreme leads to 8.7-9.2% average ΔRC and 10.3% worst-case ΔRC. Translation impact on both average and worst-case ΔRC is much more important than magnification and rotation impacts. For average ΔRC, translation impact is the largest for the same reason as in the case of positive-tone DPL. As for worst-case ΔRC, translation impact is the largest because it has no effect on C_{LL} whereas magnification and rotation change R and C_{LL} in opposite directions reducing overall ΔRC. Another observation is that magnification and rotation have very similar electrical impacts in both negative and positive tone DPL.

Results also show that field overlay has same electrical impact as wafer overlay, but field overlay is more dependent on location in the design plane, which is marked by a larger difference between minimum and maximum average variation in Tables 3 and 4. In practice, however, the amount of field overlay is much smaller than the amount of wafer overlay [14].

An important feature of negative-tone DPL is that the electrical impact is virtually independent of location in the design plane (very small difference between minimum and maximum variation in Table 4); consequently, overlay-induced variability is smaller in the case of negative-tone DPL than in the case of positive-tone DPL.

3.4.2 Effect of congestion

Table 3 results for positive-tone DPL show that ΔC is much less in case of 3-line structure (1.4% on average and 2.8% worst variation) than in case of 2-line structure ($9-10.6\%$ on average and 16.6% worst variation). This huge ΔC reduction is because line-to-line capacitance between middle wire and its left and right neighbors change in opposite directions. As a result, the total capacitance is not significantly affected (illustrated in Figure 4).

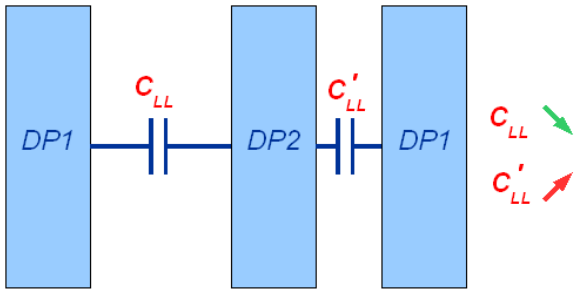

Figure 4. Illustration of cancellation effect between line-to-line capacitances in 3-line structures.

[†]In the experiments, translation vector is assumed to have a uniform direction across wafer.

In case of negative-tone DPL, Table 4 show that ΔRC is larger in case of 3-line structure ($10.6-11.6\%$ on average and 15.4% worst variation) than in case of 2-line structure ($9.8-10\%$ on average and 10.9% worst variation). C and R varies in opposite directions. For 3-line structure, the additional C_{LL} term with the third line is unaffected by overlay resulting in the reduction of overall ΔC. This explains why ΔRC is larger in case of 3-line structure than in case of 2-line structure.

These important features, especially the cancellation effect between line-to-line capacitances in positive-tone DPL, give motivation for considering congestion in electrical evaluation of overlay impact. Given layout's average congestion G, we estimate the probability of 2-line and 3-line structures in the layout. This is done by considering 3 channels that are filled by a wire with probability equal to G. The probability of 3-line structures, P_{3l}, is G^3 and the probability of 2-line structures at minimum spacing, P_{2l}, is $G^2 \times (1-G) \times 2$[‡]. Other possible structures do not induce capacitance variation since they do not involve two or more wires at minimum spacing and therefore can be formed using only one exposure. Hence, the average capacitance variation in the layout is

$$\begin{aligned} \Delta C_{avg} &= \Delta C_{2l} \times P_{2l} + \Delta C_{3l} \times P_{3l} \\ &= \Delta C_{2l} \times G^2 \times (1-G) \times 2 + \Delta C_{3l} \times G^3. \end{aligned} \tag{12}$$

Using Equation (12) and ΔC_{2l} and ΔC_{3l} (average variation) values for the case of estimated overlay components in Table 3, we plot in Figure 5 ΔC_{avg} as a function of congestion for the case of positive-tone process only since it is more favorable for lithography than negative-tone process [3,4]. This plot show that ΔC_{avg} is at most 3.4% (for $G = 72\%$) and can be as low as 2.5% for highly congested layouts (90% and more).

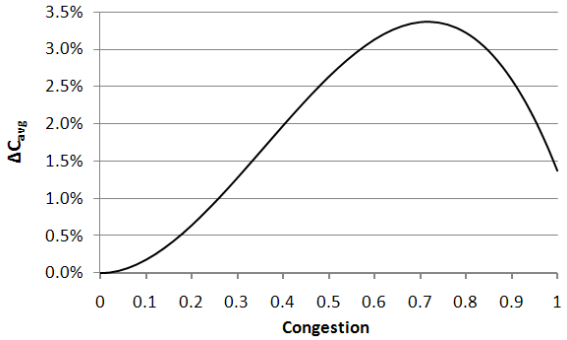

Figure 5. Plot of average coupling capacitance variation in positive-tone DPL as a function of congestion.

3.4.3 Effects of design parameters

Effects of wire length (L) and spacing (s) are evaluated by running the experiment for the case of 2-line structure in positive-tone DPL and estimated overlay components with different values of L and s. Average and worst-case C variations are reported in Tables 5 and 6 respectively. These results show that the effect of L on overlay electrical impact is negligible for $L < 1000\mu$m, which is close to maximum wire length in local interconnect levels where DPL is likely to be implemented. On the other hand, results show a large effect of s on overlay electrical impact; e.g. with 20% increase of s, C is reduced by 21.9% on average and 22.8% for worst case. The effect of s is even larger for smaller dimension of the half-pitch; e.g. for 25.6nm half-pitch, C is reduced by 26% on average and 27.5% for worst case with 20% increase of s.

Table 5. Average ΔC over wafer for different values of wire length (L) and spacing (s) in case of 2-line structure with positive-tone DPL.

	s = **25.6nm**	s = **32nm**	s = **38.4nm**
L = 10μm	13.28%	9.82%	7.67%
L = 100μm	13.28%	9.82%	7.67%
L = 1000μm	13.28%	9.82%	7.67%

[‡]multiplication by 2 accounts for the two possible locations of 2-line structures: occupying either first two channels or last two channels.

Table 6. Worst case ΔC in wafer for different values of wire length (L) and spacing (s) in case of 2-line structure with positive-tone DPL.

	s = **25.6nm**	s = **32nm**	s = **38.4nm**
L = 10μm	22.91%	16.60%	12.81%
L = 100μm	22.90%	16.60%	12.81%
L = 1000μm	22.86%	16.57%	12.78%

Table 7. Average ΔRC over wafer for different values of wire length (L), width (w), and spacing (s) in case of 2-line structure with negative-tone DPL.

	w = **25.6nm**			w = **32nm**			w = **38.4nm**		
	s = **25.6nm**	**32nm**	**38.4nm**	s = **25.6nm**	**32nm**	**38.4nm**	s = **25.6nm**	**32nm**	**38.4nm**
L = 10μm	13.91%	13.37%	12.89%	10.38%	9.90%	9.47%	8.18%	7.74%	7.36%
L = 100μm	13.91%	13.37%	12.89%	10.38%	9.90%	9.47%	8.18%	7.74%	7.36%
L = 1000μm	13.91%	13.37%	12.89%	10.38%	9.90%	9.47%	8.18%	7.74%	7.36%

Similar experiments are run for negative-tone DPL. Effects of wire length (L), width (w), and spacing (s) are evaluated by running the experiment for the case of 2-line structure and estimated overlay components with different values of L, w, and s. Average and worst-case RC variations are reported in Tables 7 and 8 respectively. Results show that the effect of L on overlay electrical impact is also negligible for negative-tone DPL and $L < 1000\mu$m. On the other hand, results show a large effect of w and a minor effect of s on overlay electrical impact; e.g. with 20% increase of w, RC is reduced by 21.8% on average and 22.9% for worst case and with 20% increase of s, RC is reduced by 4.3% on average. The effect of w is even larger for smaller dimension of the half-pitch; e.g. for 25.6nm half-pitch, RC is reduced by 26% on average and 34.4% in worst case with 20% increase of w.

Significant effect of s and w in layouts fabricated with positive and negative-tone DPL manifests the importance of using Design For Manufacturability (DFM) techniques like *wire spreading* and *widening*, which consist of increasing wire separation and width whenever space is available and are currently adopted as recommended layout policies. However, the use of these methods is limited since they cannot be implemented in congested regions of the layout.

Referring to the equations describing electrical characteristics of wires, i.e. Equations (4- 9), overlay in y direction (x for horizontal metallization) only affects L term; therefore, electrical impact in this direction is negligible same as the impact of L. Hence, preferred routing directions should be taken into account in overlay sampling and alignment strategies.

3.4.4 Estimation of overlay requirement

Reducing overlay budget is very challenging and costly. A large reduction might necessitate the replacement of scanners by newer ones with more accurate alignment. A small reduction requires enhanced overlay control that decreases throughput. As a result, determining how much overlay is "really" required can avoid unnecessary tight and costly overlay budget.

Even though overlay error translates into CD variation in DPL, our conjecture is that overlay-induced electrical variation is smaller than overlay-induced CD variation; consequently, overlay requirement should be determined based on overlay electrical impact, which leads to a relaxed overlay budget, rather than CD variation, which leads to excessively constricted budget as in [15].

In Figure 6, average and worst case electrical variation and CD tolerances are plotted for positive-tone DPL, the most favorable process [3,4], in 72% congestion (congestion leading to worst ΔC). Overlay requirement determined by electrical variation tolerance is significantly smaller than overlay requirement determined by same CD variation tolerance; e.g. in positive-DPL, 10% electrical variation tolerance (worst case ΔC) requires overlay $<$ 4.2nm, while the same CD tolerance requires overlay $<$ 3.7nm; this consists of a 13.2% reduction of overlay requirement. Besides, determining overlay budget

Table 8. Worst case ΔRC in wafer for different values of wire length (L), width (w), and spacing (s) in case of 2-line structure with negative-tone DPL.

	w = **25.6nm**			w = **32nm**			w = **38.4nm**		
	s = **25.6nm**	**32nm**	**38.4nm**	s = **25.6nm**	**32nm**	**38.4nm**	s = **25.6nm**	**32nm**	**38.4nm**
L = 10μm	15.69%	16.58%	16.97%	11.48%	10.87%	11.29%	10.35%	8.38%	7.94%
L = 100μm	15.68%	16.58%	16.96%	11.48%	10.87%	11.29%	10.35%	8.38%	7.94%
L = 1000μm	15.67%	16.56%	16.94%	11.47%	10.86%	11.28%	10.34%	8.37%	7.94%

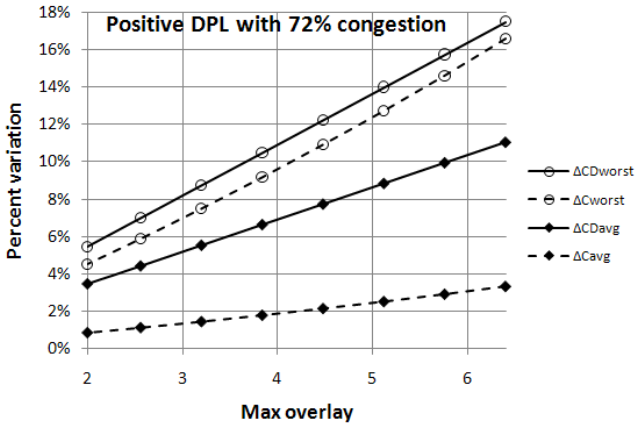

Figure 6. Plots of average and worst case CD and C variations versus requirement of maximum overlay with 72% congestion for positive-tone DPL.

requirement should also take into consideration layout information such as congestion as well as average and worst-case s and w after wire spreading and widening are performed.

4. CONCLUSIONS AND FUTURE WORK

In this paper, we electrically evaluate overlay electrical impact in positive and negative-tone DPL. Experimental results show that overlay electrical impact in positive-tone process, which is more favorable for lithography than negative-tone process [3, 4], is not severe when congestion is considered and wire spreading is performed. On the other hand, overlay electrical impact in negative-tone DPL remains a serious problem. Electrical impact is less than CD variation and, therefore, it should be the base for determining overlay requirement to possibly relax it. Our study of the relative importance of different overlay sources reveals that translation overlay has the largest electrical impact among all other sources. In addition, overlay in y direction (x for horizontal metallization) has negligible electrical impact. Therefore, preferred routing direction should be taken into account for overlay sampling and alignment strategies. In future work, we will extend the results to cover FEOL layers and try to relax overlay requirements by developing DPL-specific and design-aware alignment strategies.

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